TUNNEL TRANSISTOR MODELING

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Abstract

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Tunneling field effect transistors (TFETs) have recently attracted considerable interest because of their potential use in low power logic applications. The major advantage of tunnel transistors is the possibility to achieve less than 60 mV/decade sub-threshold swing, which is the thermionic limit in conventional MOSFETs. In this work, simulation of III-V semiconductor based tunnel transistors has been explored using both commercially available simulator (Synopsys TCAD) and novel analytical compact models.

Synopsys TCAD was used to simulate InAs homo-junction TFET. For the purpose of obtaining higher device performance, the use of AlGaSb/InAs heterostructures was then explored. Contrary to expectations, it was observed that the simulation predicts dramatic changes in device performance as a function of AlGaSb composition.

In order to gain more physical insight, also to reduce computer simulation time, a compact model was built to simulate the tunnel transistors. Analytical expressions for the electrical potential in single-gate (SG), double-gate (DG) and gate-all-around (GAA) tunnel transistors have been derived. The model predicts that the GAA geometry is not always the best geometry when quantum confinement is included in the model.
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CHAPTER 1: INTRODUCTION

Driven by increasing demand for high speed and dense integrated circuits, complementary metal-oxide-semiconductor technology (CMOS) has been continuously scaled down for more than 40 years, following Moore’s law. Assuming the technology scaling continues follow the trend in Fig. 1.1, one can expect the planar MOSFET limit to be approached within the decade.

![Figure 1.1 CMOS technology node and transistor feature size versus calendar year [1].](image)

As seen from Fig. 1.2, the leakage power already accounts for a large part of the total power (close to 50% in 2010), so CMOS technology is essentially already power constrained. To continue to advance electronics beyond the limits of conventional
CMOS, a technology to deliver high performance at low power must be developed. As theoretically analyzed by Zhang et al [2], the tunneling field effect transistor is a promising candidate to exceed the fundamental limits of CMOS in the future. Because tunnel FETs are based on Zener tunneling, a review of the relevant physics is presented, followed by a detailed discussion of the numerical simulation and analytical calculations of TFET performance in subsequent chapters.

Figure 1.2. Trends of System-on-Chip (SOC) Consumer stationary power consumption from ITRS [3]. Total chip power was decomposed into switching power and leakage power, across logic and memory.

1.1 Zener tunneling theory

At the heart of the TFET device design is a gate-modulated band-to-band (Zener) tunnel diode. The simplest way to realize a Zennertunnel diode is a heavily-doped P+/N+ homojunction. As shown in Fig. 1.3(a), the depletion region is very thin (less than 10 nm)
and the field inside the junction is very high (larger than 1 MV/cm). Consequently, under reverse bias, electrons in the valence band of the anode can tunnel through the forbidden region into the conduction band of the cathode as illustrated in Fig 1.3 (b).

The tunneling probability can be estimated by the WKB (Wentzel-Kramers-Brillouin) approximation as:

\[
T_{WKB} = \exp\left(-2 \int_{x_1}^{x_2} |k(x)| dx \right)
\]  

(1.1)

where \(k(x)\) is the imaginary wave vector inside the tunnel barrier. Approximating this through the use of a constant field \(F\) inside the tunnel barrier as shown in Fig. 1.3(b), one can obtain [4]:

\[
T_{WKB} = \exp\left(- \frac{4\sqrt{2m^*E_g^{3/2}}}{3qhf} \right)
\]  

(1.2)

where \(m^*\) is the reduced effective mass, \(m^* = (1/m_e^* + 1/m_h^*)^{-1}\). From 1.2, the Zener tunneling current can be written as:

\[
I_t = \frac{2q}{h} v \int_{E_{cm}}^{E_{m}} [f_c(E) - f_v(E)] \times T_{WKB}(E)dE
\]  

(1.3)

where 2 is from spin, \(v\) is the valley degeneracy, \(f_c\) and \(f_v\) are the Fermi distribution
functions. The limits of integration are from $E_{cn}$, the n-type conduction band edge, to $E_{vp}$, the p-type valence band edge.

From (1.3) one can see that increased tunneling probability can directly lead to a large tunneling current. In order to achieve high current for high-performance devices, small band gap and effective mass are preferred as can be inferred in (1.3). In addition, a large electric field at the tunneling junction will also increase the Zenner tunneling probability.

1.2 Tunnel transistor material choice

To compete with conventional CMOS technology, besides the advantage that tunnel transistors can potentially obtain less than 60 mV/decade sub-threshold swing, a comparable on-state current is also necessary [5]. As previously discussed, tunneling probability and thus current will benefit from the use of materials with smaller band gap and effective mass. In this work, InAs homojunction TFETs are explored. In addition, the use of heterojunctions to increase performance has also been evaluated, using the AlGaSb/InAs material system.
CHAPTER 2: MODELING TFET WITH SYNOPTYS TCAD

In this chapter, performance of p⁺/n⁺ tunnel transistors is explored using Synopsys TCAD, which is a commercially available device simulation tool. The device structure is shown schematically in fig. 2.1. A heavily doped lateral p⁺/n⁺ tunnel junction sits on top of the semi-insulating substrate, and is gated by a high κ oxide and metal gate. The thin channel is designed to be normally depleted by the gate for the purpose of building an enhancement mode device. Both InAs-based homojunction and AlGaSb/InAs based hetero junction tunnel transistors are investigated by simulation.

Figure 2.1 Structure of a gated p⁺/n⁺ singal gate lateral Tunnel FET.

2.1 Tunneling model used in Synopsys TCAD

The computation of tunneling probability in TCAD is based on the WKB approximation. The inter-band tunneling probability between two positions \(x_1\) and \(x_2\) (\(x_2>x_1\)) for a particle with energy \(E\) can be written as [6]:

\[
\text{TunProb} = \sqrt{\frac{2m}{\hbar^2}} \int_{x_1}^{x_2} e^{-\frac{\hbar}{2m} \left(\frac{2\pi}{\hbar} \sqrt{\frac{2m}{\hbar^2}}\right)^2} \left(\frac{2\pi}{\hbar} \sqrt{\frac{2m}{\hbar^2}}\right)^2 dx
\]
\[ T(x_1, x_2, E) = T_{CC}(x_1, E) \times T_{VV}(x_2, E) \times \exp\left[-2\left|\int_{x_1}^{x_2} \kappa(x, E) \, dx\right|\right] \]  

(2.1)

where \(T_{CC}(x_1, E)\) and \(T_{VV}(x_2, E)\) are the interface transmission coefficients at \(x_1\) at \(x_2\). To simplify the problem, both \(T_{CC}\) and \(T_{VV}\) are set to one in this work; this allows us to project the upper limit of drive current performance. \(\kappa(x, E)\) is calculated from Kane’s two-band dispersion relation:

\[ \kappa = \frac{\kappa_C \kappa_V}{\sqrt{\kappa_C^2 + \kappa_V^2}} \]  

(2.2)

Figure 2.2 Comparison of InAs two-band and single-band dispersion. Parabolic dispersion is used, effective mass for electron and hole are 0.023 and 0.026\(m_e\).

Here parabolic dispersion is used. \(\kappa_c\) and \(\kappa_v\) are imaginary wave vectors solved from the parabolic dispersion using \(m_c\) and \(m_v\). Near the conduction and valence band edge, the two-band dispersion and single-band dispersion are close to each other. However, as illustrated in Figure 2.2, for InAs, the two-band model gives a smoother transition from valence band to conduction band. The single band model overestimates
the imaginary wave vector, and that will result in a smaller tunneling probability compared with the two-band model.

2.2 Homojunction tunnel transistor

In this chapter, InAs homojunction TFETs are self-consistently simulated by coupling Poisson’s equation with the continuity equation for electrons and holes. The principal material parameters used in the simulation are listed in table 2.1.

<table>
<thead>
<tr>
<th>MATERIAL PARAMETERS USED IN SIMULATION</th>
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<tbody>
<tr>
<td>parameters</td>
</tr>
<tr>
<td>( E_g ) (eV)</td>
</tr>
<tr>
<td>( m_e (m_e) )</td>
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<tr>
<td>( m_v (m_e) )</td>
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<tr>
<td>Affinity (eV)</td>
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Figure 2.3 shows a simulated transfer curve for a \( p^+ / n^+ \) InAs TFET with body thickness of 4 nm and gate length of 200 nm. 1 nm of Al\(_2\)O\(_3\) layer is used as the gate oxide, with a dielectric constant of 9. The gate metal is ideal, with a work function of 5 eV. The P type doping is \( 5 \times 10^{19} \) cm\(^{-3} \), and the N type doping is \( 1 \times 10^{18} \) cm\(^{-3} \). The drain is biased at 0.4 V.

As seen from the transfer curve in Fig. 2.3, the maximum drain current is about 50 \( \mu A/\mu m \) at \( V_G=0.2 \) V. However, the threshold voltage of this device is considerably lower than zero. In order to achieve a more desirable positive \( V_T \), one can tune the metal work
function. As seen from figure 2.3, a 0.4 V voltage window is used (the $V_{DD}$) to select working region. The best sub-threshold swing can be obtained as marked on the curve.

Figure 2.3 Transfer curve of InAs tunnel FET, the drain side is biased at 0.4V. p+ doping is $5 \times 10^{19}$ cm$^{-3}$, and n+ doping is $1 \times 10^{18}$ cm$^{-3}$.

The simulated results of InAs tunnel FET by TCAD are not too far from what predicted by Luisier et al [7] using atomistic full-band Schrodinger-Poisson simulation. In our work, the on-state current (at the most positive $V_G$ in the working window) is about 20 $\mu$A/µm, while the off-state current is about 0.01 $\mu$A/µm. So the on/off ratio is about $2 \times 10^3$, which is acceptable if compared with the CMOS technology. However, the 130 mV/decade sub-threshold swing is much larger than the thermionic limit. Furthermore, if compared with the high performance MOSFETs with an on-state current of more than 1000 $\mu$A/µm, the current level of InAs tunnel FET is far too low to be competitive. In a homojunction, electrons from the valence band have to tunnel through
the whole band gap into the conduction band. The large barrier limits the tunneling probability under low bias condition, thus lead to a small tunneling current. In order to achieve higher on-state currents and still maintain similar off-state thermionic leakage, one possible way is using the heterostructure to build the tunnel transistor.

2.3 Heterojunction tunnel FET

As discussed in the previous section, a representative InAs homojunction tunnel FET has been studied but the device performance was not satisfying in terms of being a suitable replacement for CMOS because of its low drain current density. To further improve the on-state current level, one important issue is to reduce the tunnel barrier. The band gap of InAs is 0.37 eV, so reducing the barrier by choosing a lower bandgap channel material will result in the off-state thermionic current increasing dramatically due to room temperature thermal generation. In order to increase the on-current while still maintaining similar off-state current, a heterojunction can be used in which the effective tunnel barrier is the band overlap between the two materials.

AlGaSb/InAs is a nearly lattice-matched material system that allows for tuning of the band overlap by adjusting the ternary composition. InAs has a lattice constant of 6.06 Å, while GaSb and AlAs’s lattice constant are 6.10 Å and 6.14 Å, respectively. So the maximum lattice mismatch in this material system is about 1.3%. As show on figure 2.4, AlSb/InAs has a staggered band alignment, and GaSb/InAs has a broken band alignment. The ternary AlGaSb can be used to tune the band alignment to InAs.
2.3.1 Impact of aluminum mole fraction

In this work, a series of simulations of AlGaSb/InAs TFETs with different aluminum mole fraction have been done. Figure 2.5 shows the transfer curve dependency on aluminum composition. The same device structure is used as in figure 2.1 with a $5 \times 10^{19}$ cm$^{-3}$ p+ doped AlGaSb source, and a $2 \times 10^{17}$ cm$^{-3}$ n+ doped InAs drain. With 0.14 aluminum content, the band is broken with a gap of 10 meV, and when the Al mole fraction is 0.15, the band is overlapped by about 5 meV. We see the on-state current is very high for these devices, around 1 mA/µm. This is because the effective tunnel barrier is very low, in fact, for the broken gap case, there is effectively no tunneling barrier at all. Consequently, a very high on-state current can be achieved. However, the device can still be turned off by moving the bands under the gate to turn off the tunneling window.
Figure 2.5 Comparison of transfer curves of AlGaSb/InAs TFETs with different aluminum compositions. The gate length is 20 nm. Drain is biased at 0.3 V.

As shown in figure 2.6, the choice of aluminum composition has a strong influence on current. From aluminum content of 0.1 to 0.2, the current decreases from about 2000 to about 1400 µA/µm. Even this lower current, however, is still much higher than the homojunction TFET, and even higher than current high performance MOSFETs.

One might already see the n-type doping in heterostructure TFET ($2 \times 10^{17}$ cm$^{-3}$) is 5X lower than in the homojunction TFET ($1 \times 10^{18}$ cm$^{-3}$), but the performance was improved. This is because the effective tunnel barrier height is much lower in the heterostructure, so in order to keep the barrier thickness similar, a lower charge density is needed. This is a big advantage of heterojunction TFET, because with a lower doping density, the channel can be depleted much easier, and thus it is expected to be easier to build an enhancement mode device.
2.3.2 Influence of gate position

In experimental realization of TFETs, it is impossible to perfectly align the gate and the tunnel junction as shown in figure 2.1. The gate edge might be located to the left or the right of the tunnel junction. To investigate the impact of this gate misalignment, simulations with displaced gates were performed. From the simulation results showed in figure 2.7, the transfer curve was not changed too much when the gate was mis-aligned to the tunnel junction. The on-state current slightly changed, from 226 µA/µm (well aligned) to 147 µA/µm (gate left shifted 5 nm) at 0.2 V gate bias. The sub-threshold swing changed by a small amount, and the threshold voltage shifted only a little, by 9 mV for the worst case.
2.3.3 Interface trap assisted tunneling

The impact of interface traps is often a significant issue when dealing with tunneling devices, because the interface traps can provide extra energy states for tunneling, and thus can significantly alter the tunneling probability. In this section, the impact of interface states at the heterojunction on TFET performance is explored. In Synopsys TCAD, one cannot directly couple interface traps into the tunneling model. However, a spatially distributed trap can be used in the tunneling calculation. In all the simulations, the interface traps were modeled as being spatially distributed over a region extending from 1 nm left of the junction to 1 nm right of the epitaxial tunnel junction. Since the energy distribution of traps at the InAs/AlGaSb interface is not well established, simulations for several trap energy distributions were performed. The energy distributions were assumed to be uniform, but with states distributed over different
energy ranges from 1eV to 0.1 eV. For the trap energy distribution, the reference energy is the conduction band of InAs.

Figure 2.8 Impact of trap assisted tunneling on TFET performance when working as a forward biased tunnel diode.

Figure 2.9 Impact of trap assisted tunneling on TFET transfer curve, trap density is $10^{12} \text{ cm}^{-2}$, distributed in a 0.1 eV energy window around the InAs conduction band.

To explore the impact of traps on the device, the TFET was operated like a forward-biased tunnel diode. An ideal tunnel diode has a peak current that is dominated
by tunneling current, while the valley current is dominated by thermionic current. Figure 2.8 shows a TFET at a gate bias of 0.2 V, operating in a tunnel diode mode, as a function of trap density and distribution. As described earlier, all interface traps are located within a 2 nm region surrounding the tunnel junction. The traps cause the electronic field at the junction to be redistributed, lowering the peak current. In addition, one can see that the devices with $10^{12}$ cm$^{-2}$ trap density has a larger valley current than devices with $10^{11}$ cm$^{-2}$ trap density or no traps, clearly indicating that the trap-assisted tunneling increases the off-state current level above the thermionic limit (the trap-free case). Figure 2.8 shows transfer curves for TFETs with and without interface traps at tunnel junction. As can be seen, the one with trap-assisted tunneling has a much higher off-state current and lower on-state current. Thus when experimentally building TFET, the interface trap density must be carefully considered, since the traps at interface can significantly degrade the sub-threshold swing, even for a device that is otherwise perfectly designed and processed.

2.4 Conclusion

Performance of InAs homojunction and AlGaSb/InAs heterojunction TFETs has been explored using Synopsys TCAD in this chapter. The heterostructure TFET has been shown to have a much higher on-state current and steeper sub-threshold swing, and is a more promising candidate to succeed beyond the limits of conventional CMOS.

It should be noted that the simulations presented here do not include the effects of quantum confinement. It is also unclear whether TCAD can include quantization effects into the calculating of tunneling current. Thus in order to flexibly add more physical models into the simulation and gain more physical insight, as well as to save some
computation time, a physics-based compact model was developed in the next chapter to simulate TFET performance.
There are two major approaches to experimentally build TFETs; one is the previously mentioned p’n’ TFET, another is the PIN diode (p’/intrinsic/n’) based TFET [7]. In p’n’ type TFET, the tunnel barrier thickness highly depends on the doping in the channel. However in the PIN structure, the tunnel barrier thickness is mainly influenced by the gate electrostatic control. In this chapter, first of all, an analytical Poisson solution will be derived for PIN based TFET, and then a tunneling model without quantum confinement is established. Finally the quantum confinement effect is incorporated into the model.

In CMOS technology, the aggressive scaling of gate length has led to a significant short channel effect and increase in the leakage current level. In order to estimate the short channel effect, the concept of natural scale length, $\lambda$, has been used, which gives an approximation to the potential close to source side as $A \times \exp\left[-\frac{x}{\lambda}\right]$. To achieve good electric control and suppress short channel effect, the gate length $L_g$ should fulfill $LL_g > 4.6\lambda$ [9]. Structures with inherently better gate electrostatic control like fully depleted SOI, Fin-FET and nanowire transistors have been proposed to achieve better electrostatic control [10]. Because good control of the potential profile in the channel is also very important for TFETs, these advanced gate geometries can also be employed to build TFETs.
As shown in figure 3.1, TFETs with different geometries are explored in this chapter. Single-gate (SG) is a SOI structure in which the TFET sits on top of a thick body oxide. Double-gate (DG) is like a Fin-FET, the top and bottom gates are symmetric, with the same gate metal, oxide and bias voltage. The Gate-all-around (GAA) geometry is just a nanowire wrapped by an oxide and metal stack. Device performance of TFETs based on SG, DG and GAA structures will be compared in this chapter.

![Device structures of single gate, double gate and gate all around TFET.](image)

Figure 3.1 Device structures of single gate, double gate and gate all around TFET.

The x-y coordinate is used in SG and DG, r-z coordinate in GAA.

3.1 Electrostatic Comparison

3.1.1 Analytical solution of Poisson’s equation

The potential profile inside SG, DG and GAA TFETs can be obtained by solving Poisson’s equation, \( \Delta \varphi = -\rho/\varepsilon \). Because the source and drain are always metallically doped, to simplify the problem we assume there is no band bending inside the source and
drain. One way to analytically solve the potential in these devices is using the parabolic assumption [11], using the coordinate system described in figure 3.1, which can be written as follows:

\[ \varphi(x, y) = a \times y^2 + b \times y + c \]  

(3.1)

However as mentioned in [10], the parabolic assumption only gives a reasonable estimation for \( \lambda \) along the center of the channel. A more rigorous approach to solve Poisson’s equation is to use the superposition of potential; in this approach Poisson’s equation can be written as:

\[ \varphi(x, y) = u(x, y) + v(y). \]  

\[ \Delta v(y) = -\rho/\varepsilon \]  

(3.2)

\[ \Delta u(x, y) = 0 \]  

(3.3)

The boundary conditions can be written as:

\[ \varphi|_{x=0} = \varphi_s, \varphi|_{x=L_g} = \varphi_d, \varphi|_{gate} = \varphi_g \]  

(3.4)

Here the boundaries depend on material parameters and the doping in source and drain regions. The boundary condition (3.4) can be decomposed into:

\[ v(y = gate) = \varphi_g \]  

(3.5)

\[ u|_{y=gate} = 0, u|_{x=0} = \varphi_s, u|_{x=L_g} = \varphi_d \]  

(3.6)

The function \( v(y) \) is the long channel solution, which depends only on the coordinate normal to the channel. \( v(y) \) can be easily solved using (3.2) and (3.5). Eq. (3.3) can be solved by expanding the boundary conditions described in (3.6) using Fourier series. The solution inside the semiconductor can then be written as:

\[ SG : U = \sum_{n=1}^{\infty} \cos(y / \lambda_n) \times \left[ A_n \frac{\sinh(x / \lambda_n)}{\sinh(L_g / \lambda_n)} + B_n \frac{\sinh((L_g - x) / \lambda_n)}{\sinh(L_g / \lambda_n)} \right] \]  

(3.7)
Here prefactors $A_n$ and $B_n$ can be derived from the boundary conditions (3.6). If the dielectric constants of the oxide and semiconductor are the same, then the basis functions used to expand (3.6) for SG and DG cases are cosine functions, and the basis functions for the GAA geometry are Bessel functions. However, if the oxide and semiconductor have different dielectric constants, then a new function set has to be constructed to serve as the basis [12]. In this work, a new function set was created and the Poisson’s equation was solved for SG, DG and GAA TFETs. More details on this solution are provided in Appendix I. Here we list the Eigen functions which were obtained from the continuous dielectric constant assumption since this can be done in closed form:

**SG:** \[ \tan\left(\frac{t_{ox}}{\lambda_n}\right) \times \tan\left(\frac{t_s}{\lambda_n}\right) = \varepsilon_{ox}/\varepsilon_s \] \hspace{1cm} (3.10)

**DG:** \[ \tan\left(\frac{t_{ox}}{\lambda_n}\right) \times \tan\left(\frac{\bar{t}_s}{2\lambda_n}\right) = \varepsilon_{ox}/\varepsilon_s \] \hspace{1cm} (3.11)

**GAA:** \[ \varepsilon_s \frac{J_1(R)}{J_0(R)} = \varepsilon_{ox} \frac{J_1(R/\lambda)N_0(R_i/\lambda) - N_1(R/\lambda)J_0(R_i/\lambda)}{J_0(R/\lambda)N_0(R_i/\lambda) - N_0(R/\lambda)J_0(R_i/\lambda)} \] \hspace{1cm} (3.12)

In these expressions, $t_{ox}$ is the thickness of oxide, $t_s$ is the thickness of semiconductor layer, $R$ is the radius of cylindrical semiconductor, and $R_i$ is the radius of semiconductor and oxide.
3.1.2 Comparison of SG, DG, GAA gate control

Using the models derived in the previous section, the potential inside the intrinsic semiconductor region can be solved. First we compare our model with Synopsys TCAD. As shown in figure 3.2, except right at the drain end, the potential from our model matches the TCAD result for an InAs PIN TFET very well. The source and drain side are doped to a degeneracy energy of 0.05 eV. However, the doping in the n+ drain side was not very high ($5 \times 10^{17}$ cm$^{-3}$) due to the low $m_e^*$, so there is still some band bending in that region. This leads to the discrepancy observed in figure 3.2. However, for TFET operation, the tunneling current is primarily determined by the source tunnel junction, so our model gives a very good approximation in that critical region.

Figure 3.2 Band profile comparison of results from analytical model and from Synopsys TCAD device simulator, for an InAs PIN TFET. Band diagram is plotted along the center of SG TFET with $V_{gs}=0.1$ and $V_{ds}=0.3$ V, $t_s=10$ nm, $L_g=100$ nm, EOT=1 nm.
As shown in figure 3.3, when SG, DG and GAA TFET provides the same geometrical parameters and the same bias conditions, the GAA structure has best gate control (as shown by the degree of source-side band bending), and thinnest tunnel barrier at the source tunnel junction. The DG TFET is the second best, and SG is the least favorable. So from the point of view of electronstatic control of the channel, GAA is clearly the best geometry. In this comparison, all three devices are using gate length of 100 nm, and as one can see the band diagram is flat at the middle of the channel. That means the source junction is almost not affected by the drain side bias. However, if the device was scaled aggressively, the source and drain will be very close to each other and the drain induced barrier thinning (DIBT) effect will become important. This causes leakage tunnel current. From the band diagram, we can see the GAA is the best geometry to avoid the deleterious effects of DIBT.

Figure 3.3 Band profile comparison SG, DG and GAA TFET with $V_{gs}=0.3$ V and $V_{ds}=0.3$ V, $t_s=10$ nm, $L_g=100$ nm, EOT=1 nm.
As mentioned earlier, the potential near the source region can be approximated by using the natural scale length $\lambda$. From the simulated band diagram, an effective scale length was extracted by fitting the band bending near the source. The influences of oxide thickness, oxide dielectric constant and channel layer thickness on effective scale length are compared in figure 3.4. As one might expect, scaling of the oxide and channel thickness improves the electrostatic control, as does the use of high-$\kappa$ gate oxide material. However, from the comparison, one can see that the influence of oxide dielectric constant is not as obvious as oxide and channel thickness. And the effective scale length tends to saturate as $\varepsilon_r$ approaches to 20. So high-$\kappa$ material with $\kappa$ beyond 20 may not be very effective to improve the gate control further. Reductions in the channel and oxide thickness are needed to effectively improve the electrostatic control.

Figure 3.4 Effective scale length comparisons of SG, DG and GAA TFETs. Dielectric constant used for upper 3 figures is 15. Lower figures show impact of unequal
oxide/semiconductor dielectric constant for 10 nm channel thickness and 1 nm physical oxide thickness.

3.1.3 Approximation of natural scale length $\lambda$

As discussed above, we know that the scale length gives a good estimation of the potential at the source end of the channel, which provides a guide for how much one can scale the device gate length before the onset of short channel effects. Consequently, a method to quickly approximate the scale length from the device geometry and material parameters would be valuable. As mentioned in [13], the first solution from the Eigen functions (3.10)-(3.12) can be used as a quick estimation of scale length $\lambda$. From figure

![Figure 3.5](image)

Figure 3.5 (a)-(c) Pre-factors and scale length of different mode in SG, DG, and GAA TFET. bnR and bnL are pre-factors in the series solutions (Eqn. 3.7 – 3.9). (d) - (f) Simulated band diagram and 1st-order $\lambda$ approximated band diagram.
3.5, one can see the simulated band diagram and the band diagram approximated using the 1st-order $\lambda$ matches very well. The value of $\lambda_n$ decays very fast as the mode number $n$ increases, and the pre-factor decays even faster. This is the reason why the 1st-order $\lambda$ can give a good approximation of the band diagram.

3.2 Tunneling model and performance comparison

InAs TFETs in geometries of SG, DG and GAA have been simulated by Luisier et al. [6] using tight binding simulation. The sp$^3$d$^5$s$^*$ model was used for ultra thin body (UTB) SG and DG, and sp$^3$s$^*$ for GAA. This helps to reduce the complexity of simulation and reduce computation time, because the complexity of tight binding simulation depends on the number of atoms in the device and the number of orbits used for each atom. So devices with large size (like nanowire with diameters larger than 10 nm) are prohibitively time-consuming to simulate even on a large computer cluster. Furthermore, the results of tight binding simulation all come out together. One cannot easily separate physical effects to gain more physical insight. To address this shortcoming, a tunneling calculation based on WKB and Flietner’s two-band model has been developed, and results comparable to full tight binding model calculations are obtained.

3.2.1 Flietner’s two-band model

Very similar to what has been done in Synopsys TCAD, in our compact model, we use WKB to estimate the tunneling probably through the energy barrier. In our simulation, Flietner’s two-band model is used instead of Kane’s two-band model, which has been used in TCAD. As discussed by Mukasa et al in [13], Kane’s two-band model
works well when conduction and valence band effective mass are the same, but when
they differ significantly, it becomes less accurate. However, Flietner’s two-band model is
still valid when \( m^*_c \) and \( m^*_v \) are different. Flietner’s two-band model can be described as
follows:

\[
\frac{\hbar^2 k^2}{2m^*_c} = \frac{E(E/E_g-1)}{(1-\alpha)+E/E_g}
\]

where \( \alpha = 1 - \sqrt{m^*_c/m^*_v} \). When \( m^*_c = m^*_v \), Flietner’s model reduces to Kane’s two band
model.

To calculate the tunneling probability without consideration of the transverse
momentum, the 1-D probability \( T_{1D} \) can be numerically derived using Flietner’s model
and WKB integration. However, when the transverse momentum is included, the 3-D
tunneling probability should be written as:

\[
T_{3D} = \frac{1}{L_x L_y} \sum_{k_x, k_y} T_{1D} \times \exp\left[-2 \frac{E^c_T + E^v_T}{\bar{E}} \right]
\]

where \( E^c_T \) and \( E^v_T \) are the transverse energies of electrons and holes. Because only carriers
with small transverse energy can tunnel through the barrier (larger transverse energy
means increase of the effective band gap, and thus reduces the tunneling probability
significantly), we can use the parabolic band dispersion along the transverse direction.

Then the transverse energy can be written as:

\[
E^c_T = \frac{\hbar^2 k_x^2}{2m^*_c} + \frac{\hbar^2 k_y^2}{2m^*_v}
\]

\[
E^v_T = \frac{\hbar^2 k_x^2}{2m^*_v} + \frac{\hbar^2 k_y^2}{2m^*_c}
\]
Substituting (3.15) and (3.16) into (3.14), replacing the summation with integration, and under the assumption of constant field inside the tunnel barrier, results in the following expression for the 3-D tunneling probability:

\[ T_{3D} = \left( m_{rx}^* m_{ry}^* \right)^{1/2} \frac{E}{4\pi \hbar^2} \times T_{1D} \]  

(3.17)

One can see there is only a pre-factor difference for 3-D and 1-D tunneling probability. However, a constant field inside the tunneling barrier was assumed in this derivation, and for a PIN structure TFET, the field is clearly not constant. It can be shown that the tunneling probability of 3-D is still a pre-factor difference from \( T_{1D} \). The 3-D tunneling probability for non-constant field can be written as:

\[ T_{3D} = \left( m_{rx}^* m_{ry}^* \right)^{1/2} \frac{\bar{E}}{4\pi \hbar^2} \times T_{1D} \]  

(3.18)

with

\[ \bar{E} = \frac{4q\hbar[1+(m_{cz}^*/m_{cz})^{1/4}]^2}{3\pi (2m_{cz}^* E_0)^{3/2}} F_{eff} \]  

(3.19)

We know tunneling is enabled by the presence of a strong electric field inside the junction, and the maximum tunneling probability should happen along the field direction. But in our model, angled tunneling was not included, only tunneling along the channel direction is calculated. However, as shown in figure 3.6, the electric field inside the TFET at on-state is almost parallel to the channel direction, suggesting that the use of this simplified tunneling model in the simulation should be reasonably accurate.
3.2.2 Simulation results and comparison

Using Flietner’s two-band model, non-constant field 3-D tunneling probability, and WKB integration, the tunneling current is calculated. The transfer curve of SG, DG and GAA TFETs are compared in figure 3.7. Obviously the GAA has the highest on-state current and DG is the second highest. The reason is that GAA TFET has the smallest scale length $\lambda$, which means the thinnest tunneling barrier at the source tunnel junction. However the off-state current level also increases with on-state current, because there is a large tunnel current at the drain side when the gate was turned off due to the symmetric property of PIN structure TFETs.
Figure 3.7 Transfer curves of SG, DG and GAA TFET with $t_s$ of 5, 10, 15, 20 nm.

t$_{ox}$=1 nm, $\varepsilon_{ox}$=15 $\varepsilon_0$, $L_g$=100 nm.

From figure 3.7, the on-state current for GAA TFET with $t_s$=5 nm is about 700 $\mu$A/µm, and it is much higher compared to the value from tight binding simulation [6] of 110 $\mu$A/µm. An important reason why our simulated current is higher than theirs is that the quantum confinement was not accounted for in this simulation. When quantum effects are considered, the band gap and the effective mass will increase significantly for thin channel devices, and result in a smaller tunneling current. In addition, for the same device structure, different body thickness or diameter gives quite different transfer curves, because the scale length also depends on the thickness of semiconductor layer.

3.3 Impact of quantum confinement

Thus far, no quantum effects (except for tunneling) have been included in the model. However, we know the quantum confinement enlarged band gap and effective mass will reduce the tunneling current. In order to achieve a better estimation of device performance for thin channels, this effect must be included. In this work, the values of band gap and effective mass for UTB SG and DG are from tight-binding simulation.
(Courtesy of Steve Koester, IBM). The effective mass for nanowire GAA TFET is from [14], which also comes from tight binding simulation.

![Figure 3.8 Wave vector and energy relationship for InAs nanowire along <110> direction with \(d=2.5\) nm, courtesy of Steve Koester, IBM.](image)

From the tight binding results, the wave vectors inside the band gap are very symmetric in the conduction and valence band. So in all the simulations, same effective mass for electrons and holes has been used. The dependency of effective mass and band gap on UTB thickness and nanowire diameter is shown in figure 3.9. Clearly, the nanowire GAA geometry has more quantum confinement than UTB SG and DG geometries. As expected, for larger thickness/diameter devices, the quantum confinement effects are weaker, and the parameters converge on their bulk values.
As shown in figure 3.10, the tunneling current is much lower when quantum confinement is considered. Due to larger quantum confinement, devices with 2.5 nm InAs thickness have much smaller current than those with thick channels. This is an especially strong effect for the GAA geometry, because nanowires are confined in two transverse dimensions. For example, when the diameter is 2.5 nm, the band gap is about 1.5 eV and effective mass is close to 0.15 $m_0$. Compared with the bulk value of 0.37 eV and 0.021 $m_0$, the band gap is 4X larger and the effective mass is 7X larger. Obviously one can see the GAA structure is most sensitive to the adverse effects of quantum confinement. However, we already know the GAA TFET has the best electrostatic control, so there might be an optimized case for $t_s$ that can benefit from the better gate control of GAA geometry, while avoiding excessive quantum confinement effects.
Figure 3.10 Comparison of transfer curves of SG, DG and GAA with $t_{ox}=2$ nm, $\varepsilon_{ox}=20\varepsilon_0$, $L_g=100$ nm. The top row does not include quantum confinement, while the bottom row includes quantum confinement effects.

Figure 3.11 Comparison of on-state current density versus off-state current of SG, DG and GAA with $t_{ox}=2$ nm, $\varepsilon_{ox}=20\varepsilon_0$, $L_g=100$ nm. The top row does not include quantum confinement, while the bottom row has quantum confinement effect included.
In order to find the optimal design, we compared on-state current density versus off-state current in figure 3.11. For a fixed off current, we look at which geometry provides the best injection efficiency, which can be estimated from the on-state current density. The on-state and off-state are defined from the transfer curve by a voltage window of 0.3 V, which was the $V_{dd}$ in all the simulations. As shown in figure 3.11, when quantum confinement was not included, better electrostatic control always leads to higher injection efficiency. However, when quantum confinement induced band gap and effective mass enlargement was considered, the injection efficiency first increases as $t_s$ becomes larger, and then reaches a maximum point and turns back. For GAA, the optimized case is between 7.5 and 10 nm in diameter, while for DG the optimum is between 5 and 7.5 nm body thickness.

3.4 Impact of short channel

In our previous simulation, the gate length used is 100 nm, which is more than 5X larger than the natural scale length $\lambda$. But smaller gate length is always preferred for high speed switching, which was the major driver for MOSFET scaling. In order to evaluate the scaling property SG, DG and GAA InAs TFETs, a comparison has been done between TFETs with 100 nm and 20 nm gate lengths. As shown in figure 3.12, devices with gate lengths of 20 nm have much higher leakage current. From the band diagrams of GAA for $L_g=20$ and 100 nm respectively in figure 3.13, the source side potential was obviously affected by the drain bias for $L_g=20$ nm. When biased in the off-state, the tunneling length is more than 80 nm for $L_g=100$ nm. However, in the 20 nm channel, the off-state tunnel path is only about 18 nm long, and this leads to severe leakage current.
As mentioned by Plummer et al. [8], $L_g$ should be larger than $4.6\lambda$ to achieve good gate control and avoid short channel effects. So for a 20 nm gate length, the scale length $\lambda$ should be less than 4 nm, and that requires exceptional electrostatic control of the channel.

![Transfer curves of SG, DG and GAA TFETs for $L_g=100$ nm (upper) and $L_g=20$ nm (lower). With $t_s=2$ nm, $\varepsilon_{ox}=20 \varepsilon_0$.](image1)

Figure 3.12 Transfer curves of SG, DG and GAA TFETs for $L_g=100$ nm (upper) and $L_g=20$ nm (lower). With $t_s=2$ nm, $\varepsilon_{ox}=20 \varepsilon_0$.

![Band diagrams of short channel and long channel GAA TFETs at off-state bias with $V_g=-0.2$ and $V_d=0.3$ V.](image2)

Figure 3.13 Band diagrams of short channel and long channel GAA TFETs at off-state bias with $V_g=-0.2$ and $V_d=0.3$ V.
CHAPTER 4: FUTURE STUDY AND CONCLUSION

4.1 Conclusion

Analytical Poisson and tunneling models were developed for single gate, double gate and gate-all-around TFETs. The Poisson model is robust, and compares well with the commercial software Synopsys TCAD. The tunneling model also gives reasonable results compared to results from tight banding simulation. Device performance of SG, DG and GAA TFET has been compared. The GAA geometry is shown to provide the best electrostatic control of the channel, which will help suppress short channel effects and reduce off-state leakage. However, due to the thin body thickness, the quantum confinement effects in these devices are very strong. Quantum confinement increases $m^*$ and $E_g$, and thus degrades TFET performance. Because the GAA structure is confined in two directions and the SG and DG are only confined in one transverse direction, the quantum confinement effect has more impact on the GAA geometry.

4.2 Recommendations for future study

In this work, only compact models for homojunction TFETs are developed. But from the simulation results of chapter 2, one might see there is a big performance boost by changing from homojunction to heterojunction TFET. The on-state current is 10X larger and the sub-threshold swing is much steeper. Also as shown in chapter 3, quantum
confinement will hurt the device performance by increasing the band gap and effective mass. However, in heterojunction TFETs, the tunneling barrier is not determined by the band gap, but by the effective barrier height, and that can be controlled by the band alignment. So in heterojunction TFETs, one can still benefit from the best electrostatic control from GAA, while managing the quantum confinement-induced enlarged band gap by tuning the band alignment to compensate.

Another improvement that could be done is to include the tunneling model for 1-D and 2-D. In the current model, the tunneling model used is all 3-D tunneling, only the quantum induced band gap and effective mass change are included. But for small semiconductor thickness, SG and DG are actually 2-D structures and GAA is actually 1-D. So when calculating the tunneling probability by summing over the transverse momentum space, the quantum confinement of momentum should be considered.

Last but not least is the implementation of a fully self-consistent model. In conventional MOSFETs, when the device is in the on-state, there is an inversion charge at the channel surface, and this should be the same situation for large size TFET. However, TFETs that are of interest have very small size. In these situations, the charge distributions are different from traditional MOSFET as shown in [15]. The charges are distributed in a Sine-like distribution for SG and DG TFET, and are Bessel-like function in GAA TFET. One would improve the model by first calculating the total injected charge, and then using the distribution function to find the density and iteratively substitute back into Poisson’s equation.
APPENDIX A

The coordinate system was chosen as shown above. The complete function set $g_n$ derived as Fourier expansion basis:

Single gate:

$$g_n = \begin{cases} \frac{\sin(t_s/\lambda_n)}{\cos(t_{ox}/\lambda_n)} \sin[(x + t_{ox})/\lambda_n], & -t_{ox} < x < 0 \\ \cos[(x - t_s)/\lambda_n], & 0 < x < t_s \end{cases}$$

Double gate:

$$g_n = \begin{cases} \frac{\sin(t_s/2\lambda_n)}{\cos(t_{ox}/\lambda_n)} \sin \left[ x + t_{ox} + \frac{t_s}{2}/\lambda_n \right], & -t_{ox} - \frac{t_s}{2} < x < \frac{t_s}{2} \\ \cos(x/\lambda_n), & -\frac{t_s}{2} < x < \frac{t_s}{2} \\ -\frac{\sin(t_s/2\lambda_n)}{\cos(t_{ox}/\lambda_n)} \sin \left[ x - t_{ox} - \frac{t_s}{2}/\lambda_n \right], & \frac{t_s}{2} < x < \frac{t_s}{2} + t_{ox} \end{cases}$$

Gate-all-around:

$$g_n = \begin{cases} \frac{J_0(r/\lambda_n)}{J_1(r_s/\lambda_n)}, & 0 < r < r_s \\ \frac{J_0(r/\lambda_n)N_0(r_0/\lambda_n) - N_0(r/\lambda_n)J_0(r_0/\lambda_n)}{J_1(r_s/\lambda_n)N_0(r_0/\lambda_n) - N_1(r_s/\lambda_n)J_0(r_0/\lambda_n)}, & r_s < r < r_0 \end{cases}$$
Here $r_s$ is the radius of semiconductor, $r_0$ is the total radius.

From (3.7)-(3.9), if we take a short-hand notation of $U(x,y)$ as $U(x,y)=\sum_n f_n$, then the above function set will be orthogonal to $f_n$ as $\int f_m \times g_n = \delta_{mn}$, when the integration goes over the whole semiconductor and oxide region. Then the pre-factor $A_n$ and $B_n$ can be written as:

$$A_n = \frac{\int \varphi_s \times g_n}{\int f_n \times g_n}$$

$$B_n = \frac{\int \varphi_d \times g_n}{\int f_n \times g_n}$$
REFERENCES


