FABRICATION OF METALLIC SINGLE ELECTRON TRANSISTORS

FEATURING PLASMA ENHANCED ATOMIC LAYER DEPOSITION

OF TUNNEL BARRIERS

A Dissertation

Submitted to the Graduate School
of the University of Notre Dame
in Partial Fulfillment of the Requirements
for the Degree of

Doctor of Philosophy

by

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Notre Dame, Indiana
December 2015
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Abstract
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The continuing increase of the device density in integrated circuits (ICs) gives rise to the high level of power that is dissipated per unit area and consequently a high temperature in the circuits. Since temperature affects the performance and reliability of the circuits, minimization of the energy consumption in logic devices is now the center of attention. According to the International Technology Roadmaps for Semiconductors (ITRS), single electron transistors (SETs) hold the promise of achieving the lowest power of any known logic device, as low as $1 \times 10^{-18}$ J per switching event. Moreover, SETs are the most sensitive electrometers to date, and are capable of detecting a fraction of an electron charge. Despite their low power consumption and high sensitivity for charge detection, room temperature operation of these devices is quite challenging mainly due to lithographical constraints in fabricating structures with the required dimensions of less than 10 nm. Silicon based SETs have been reported to operate at room temperature.
However, they all suffer from significant variation in batch-to-batch performance, low fabrication yield, and temperature-dependent tunnel barrier height.

In this project, we explored the fabrication of SETs featuring metal-insulator-metal (MIM) tunnel junctions. While Si-based SETs suffer from undesirable effect of dopants that result in irregularities in the device behavior, in metal-based SETs the device components (tunnel barrier, island, and the leads) are well-defined. Therefore, metal SETs are potentially more predictable in behavior, making them easier to incorporate into circuits, and easier to check against theoretical models.¹

Here, the proposed fabrication method takes advantage of unique properties of chemical mechanical polishing (CMP) and plasma enhanced atomic layer deposition (PEALD). Chemical mechanical polishing provides a path for tuning the dimensions of the tunnel junctions, surpassing the limits imposed by electron beam lithography and lift-off, while atomic layer deposition provides precise control over the thickness of the tunnel barrier and significantly increases the choices for barrier materials.

As described below in detail, the fabrication of ultra-thin (~1nm) tunnel transparent barriers with PEALD is in fact challenging; we demonstrate that in fabrication of SETs with PEALD to form the barrier in the Ni-insulator-Ni tunnel junctions, additional NiO layers are parasitically formed in the Ni layers that form the top and bottom electrodes of the tunnel junctions. The NiO on the bottom electrode is formed due to oxidizing effect of the O₂ plasma used in the PEALD process, while the NiO on the bottom of the top electrode is believed to form during the metal deposition due to oxygen-containing contaminants on the surface of the deposited tunnel barrier. We also
show that due to the presence of these surface parasitic layers of NiO, the resistance of Ni-insulator-Ni tunnel junctions is drastically increased. Moreover, the transport mechanism is changed from quantum tunneling through the dielectric barrier to one consistent with the tunnel barrier in series with compound layers of NiO and possibly, NiSi$_x$O$_y$. The parasitic component in the tunnel junctions results in conduction freeze-out at low temperatures, deviation of junction parameters from ideal model, and excessive noise in the device. The reduction of NiO to Ni is therefore necessary to restore the metal-insulator-metal structure of the junctions. We have studied forming gas anneal as well as H$_2$ plasma treatment as techniques to reduce the NiO layers that are parasitically formed in the junctions. Using either of these two techniques, we reduced the NiO formed on the island after being covered with the PEALD dielectric and before defining the top source and drain. Later, the NiO formed on the bottom of the source/drain is reduced during a second reducing step after the source/drain are formed on the tunnel barrier. Electrical characterization of SETs that are made with the proposed reducing treatments enable us to study the effect of each reducing process on the properties of the constituent tunnel junctions. In comparison to the junctions annealed twice in forming gas at 400°C, we consistently observed a $\sim 10 \times$ higher conductance in devices treated twice with H$_2$ plasma at 300°C. The possible damage to the barrier during the plasma treatment and thermally induced film deformation during the anneal which respectively, is believed to increase and lower the conductance are among the possible cause of this difference. Although both types of treatments were effective in alleviating the effect of the activated components in the junctions, all the devices that were treated by two anneal steps or by two H$_2$ plasma steps (for reducing the top and bottom NiO) show deviations
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ACKNOWLEDGEMENTS

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This research was impossible without the technical support of the Notre Dame Nanofabrication Facility (NDNF) staff who do their best to keep the lab running. Therefore, I would like to express my gratitude to Michael Thomas, Michael Young, Keith Darr, David Heemstra, and Mark Richmond.

Finally, I would like to thank my group members and friends in electrical engineering department at Notre Dame who taught me many useful tips and helped me whenever I needed it.
1.1 Structure of a single electron transistor

As shown in Figure 1-1, a single electron transistor is composed of a nanometer-scale island that is coupled to source and drain through tunnel junctions that are made with ultrathin (≈ 1nm) tunnel transparent barriers. The island is also capacitively coupled to a third electrode called the gate. Although electrons can tunnel from source and drain to the island, no charge transport is possible between the island and the gate.

![Figure 1-1 Schematic of a single electron transistor](image)

Nano-gap fabrication\(^2\), oxidation of the island metal\(^3\), applying electrostatic potential to a Si-based structure\(^4\), and pattern-dependent oxidation (PADOX) of a Si rib\(^5\) are among the methods that have been reported for formation of the tunnel junctions with tunnel transparent barriers in SET devices.
The ultra-thin tunnel barriers (<1.5nm) allow direct tunneling of electrons from source and drain to the island. Tunnel junctions, as depicted in Figure 1-2, can be considered leaky capacitors that are modeled by an ideal (non-leaky) capacitance in parallel with a resistance, \( R = \frac{V}{I} \), where \( V \) is the applied potential across the junction and \( I \) is the measured tunneling current through the junction.

![Figure 1-2 Schematic of a tunnel junction](image)

Electron tunneling through the tunnel junctions allows discrete number of electrons to accumulate on the island. However, the addition of electrons to the island requires a certain amount of energy that is a function of the island total capacitance:

\[
V = \frac{(Ne + q)}{C}
\]

\[
E = \int Vdq = Ne\frac{e^2}{C} + \frac{e^2}{2C} = E_c(2N + 1)
\]

\[
E_c = \frac{e^2}{2C}
\]

Where \( q \) is the charge that is being added to the island, \( V \) is the island potential as a function of the island total capacitance (\( C \)) and number of extra electrons already added.
to the island (N). $E_c$ that is referred to as the charging energy is the required energy to add the first electron to the island (i.e. $N=0$). From the equation above it is clear that although the energy to add the first electron on the island is $E_c$, the second electron ($N=1$) requires $3E_c$ of energy to be added to the island, and the energy for adding the third electron is $5E_c$ ($N=2$).

If the energy of electrons is smaller than the charging energy, no electron can be added or removed from the island and therefore the conductance between the source-drain leads through the island is suppressed. The suppression of conductance through the SET due to the charging energy of the island is called Coulomb blockade in SETs. In other words, in order to observe the Coulomb blockade in SETs, the energy of electron should be restricted below the charging energy.

1.2 The requirements to observe single electron effects in an SET

1.2.1 Maximum temperature for operating SETs

In order to observe the single electron charging of the island, the thermal fluctuation in the energy of electrons must be smaller than the charging energy. This ensures that the thermal fluctuations do not smear the energy barrier and electrons do not enter or leave the island when it is not electrostatically favorable. As a result, the maximum temperature for operation of an SET is set as follows:

$$E_c >> k_B T \Rightarrow T << \frac{E_c}{k_B}$$

(2)
Where $T$ is the absolute temperature of operation and $k_B$ is the Boltzmann constant. The condition of $T < E_c/3k_B$ is practically sufficient for operation of an SET and experimental observation of single electron charging, since at this temperature, the peak/valley ratio in the oscillating conductance modulation by $V_g$ is ≈ 2^6.

1.2.2 Minimum resistance for tunneling junctions

One of the conditions that must be met for single electron effect observation is the suppression of quantum fluctuations. That is, the electrons must be localized on the island and the fluctuation in the number of electrons over the timescale of measurement must be suppressed. This sets a lower limit on the tunneling resistance of the barriers, which can be calculated using the Heisenberg uncertainty principle. Based on the Heisenberg uncertainty principle, the product of the quantum energy fluctuation of an electron and the lifetime of the charge on the capacitor plate has a minimum as shown in Eq. 3:

$$\Delta E \times \Delta t \geq \hbar / 2 \quad (3)$$

The lifetime of the charge on the capacitor plate can be approximated by the charge relaxation time, $R_tC$ time constant, where $R_t$ is the tunneling resistance and $C$ is the capacitance of the junction. Since the quantum energy fluctuation must be smaller than the charging energy, the minimum value for the resistance is calculated as follows:

$$\Delta E \times \Delta t \geq \frac{\hbar}{2} \Rightarrow \Delta t \geq \frac{\hbar}{2\Delta E} \Rightarrow R_tC \geq \frac{\hbar}{2 \frac{e^2}{4C}} \Rightarrow R_t \geq \frac{2\hbar}{e^2} \approx 8.2k\Omega \quad (4)$$

This minimum value of tunnel junction resistance ensures that the electron on the island has a localized wave function, which does not extend to the leads and therefore the quantum fluctuations do not lead to uncontrolled charge transport through the island.
1.2.3 Orthodox theory

Kulik and Shektar have developed a set of global rules, called the Orthodox theory, to study single electron devices. According to the Orthodox theory, tunneling events will take place randomly and independently on each junction at a rate that exponentially depends on the change of the free electrostatic energy of the system as a result of the tunneling. The tunneling rate is expressed by the formula below:

$$\Gamma(\Delta W) = \left[ \frac{I(\Delta W)}{e} \right][1 - \exp(-\frac{\Delta W}{k_B T})]^{-1}$$

(5)

where $I(\Delta W)$ is the DC current of the tunnel barrier in the absence of single-electron charging effects, and $\Delta W$ is the change in the free electrostatic energy due to the tunneling event. The statement above is the main result of the three major assumptions in the Orthodox theory:

1) The electron energy quantization inside the conductors is ignored: this assumption is valid in the experimental devices with metallic conductors due to the small Fermi wavelength of electrons ($\lambda_F$) compared to the dimensions of the metallic conductors.

2) Electron tunneling time through the tunnel barrier is negligible in comparison with the time scale of any other event, including the time interval between two consecutive tunneling events. The tunneling time of $\approx 1$ fs is much smaller than that corresponding to any operational frequency of interest.
3) Simultaneous tunneling events (cotunneling) are ignored. This assumption is valid if the value for each tunneling resistance is much higher than $R_Q$, quantum resistance.

After introducing the conditions needed for observing Coulomb blockade and single electron charging, a more detailed and quantitative description of Coulomb blockade is necessary:

The available energy states for extra electrons in the island with respect to the chemical potential of the source and drain leads are shown in Figure 1-3.
Figure 1-3 Energy states of the added electron to the island when no bias is applied to gate and the conduction through the source and drain is suppressed. (b) When $V_g = e/2C_g$ and the lowest unfilled state is aligned with the source and drain Fermi level, Coulomb blockade is lifted and an electron is added to the island. (c) When $V_g = -e/2C_g$ and the highest filled state is aligned with the source and drain Fermi level, Coulomb blockade is lifted and an electron leaves the island.

At $T \approx 0$ K, all the energy levels under the island Fermi level are filled and all the ones above the Fermi level are empty, and if we assume a zero flat-band voltage, the Fermi level of the island lies in the middle of the energy gap ($2E_c$) between the lowest empty state and the highest filled state. Consequently, since no energy states are available at the island Fermi level, there is no conduction path between the source and drain (i.e. Coulomb blockade).
Figure 1-4 shows the equivalent capacitance circuit of an SET structure. The self-capacitance of the island, $C_o$, is much smaller than the other capacitance values and therefore is not considered in our future calculations. Since the island is coupled to the gate, source, and drain, the potential of the island can be modulated by these terminals.

Assuming that the source is grounded, the island potential as a function of the bias applied to the drain and gate is as follows:

If the island potential is adjusted by the gate bias so that one of the available energy states of the island is aligned with the source and drain Fermi level (Figure 1-5 (a)) the Coulomb blockade is lifted and a conduction path forms between the source-drain through the island which allows the tunneling of one electron in and out of the island at a time. However, the conduction path is again blocked once the gate potential goes beyond that point (Figure 1-5 (b)) but reforms again as the next available energy state is aligned to drain-source Fermi level (Figure 1-5 (c)). As a result, the applied potential of the gate can periodically modulate the conductance through the device. This periodic modulation of conductance with $V_g$ is called the Coulomb blockade oscillation (CBO).
Figure 1-5 Alignment of available energy states of the island as a function of the gate potential. (a) When $V_g = e/2C_g$ and the lowest unfilled state is aligned with the source and drain Fermi level, Coulomb blockade is lifted and an electron is added to the island. (b) When $e/2C_g < V_g < 3e/2C_g$ and no island available energy state is aligned to the drain-source Fermi levels. (c) When $V_g = 3e/2C_g$ and the second lowest unfilled state is aligned with the source and drain Fermi level, Coulomb blockade is lifted and an electron is added to the island.

1.3 Quantitative analysis of Coulomb blockade oscillations and Coulomb diamonds

In order to explain the characteristics of an SET, the free electrostatic energy of a single electron transistor as a function of the applied gate bias and the number of electrons on the island is mathematically calculated. For this, let us assume no DC bias is applied to the source and drain terminals (Figure 1-6 (a)). Here, the source and drain are
grounded and the total capacitance between the island and the grounded leads is the sum of $C_d$ and $C_s$ (Figure 1-6 (b)).

Figure 1-6 (a) Equivalent capacitance circuit of an SET structure when source and drain are grounded (b) The total capacitance between the island and ground is the sum of source and drain capacitance. $q_1 - q_2$ is the total charge on the island.

As discussed before, the number of excess electrons added to the island is an integer number and is the sum of the charges at the plates of the two capacitors, i.e. $-eN = q_1 - q_2$, where $C_g$ is the gate capacitance and $C_s + C_d$ is the sum of all the capacitances with one grounded end: the source and drain, respectively. As explained before, the self-capacitance of the island is negligible compared to the source and drain junction capacitance and is not considered in our calculations.
The free (available) electrostatic energy of the system is the energy accumulated in the capacitors minus the energy by the voltage source to provide the charge $q_2$ on the gate electrode. The total free electrostatic energy is derived in Eq. 7:

$$E_{el} = \frac{1}{2} (C_g V_2^2 + (C_s + C_d)V_1^2) - q_2 V_g = \frac{1}{2} \left( \frac{q_2^2}{C_g} + \frac{q_1^2}{C_s + C_d} \right) - C_g V_2 V_g$$

(7)

$$q_2 = C_g \times V_2, \quad q_1 = (C_s + C_d) \times V_1$$

Where $V_1$ is the potential across $C_s+C_d$ and $V_2$ is the potential across the $C_g$.

Next, we define a new parameter $q_g = -C_g \times V_g$. Note that this parameter is continuous and it is different from the total number of extra electrons on the island, which must be an integer. We then write $q_1$, $q_2$, and thus $E_{el}$ in terms of $q_g$ and $eN$ as follows:

$$\frac{q_2}{C_g} + \frac{q_1}{C_d + C_s} = V_g \Rightarrow q_2 = \frac{q_1 + eN}{C_g} \cdot \frac{1}{C_d + C_s} + q_g \Rightarrow q_2 = \frac{(eN - q_g)}{(1 + \frac{C_d + C_s}{C_g})} + q_g$$

$$\frac{q_2}{C_g} + \frac{q_1}{C_d + C_s} = V_g \Rightarrow q_1 = \frac{q_1 + eN}{C_g} \cdot \frac{1}{C_d + C_s} = V_g \Rightarrow q_1 = \frac{-(eN - q_g)}{(1 + \frac{C_d + C_s}{C_g})}$$

(8)

$$E_{el} = \frac{e^2}{2(C_g + C_d + C_s)} \left( N - \frac{q_g}{e} \right)^2 \frac{q_2^2}{2C_g}, E_c = \frac{e^2}{2(C_g + C_d + C_s)}$$

$$\Rightarrow E_{el} = E_c (N - \frac{q_g}{e})^2 \frac{q_2^2}{2C_g}$$

Since the last term in $E_{el}$ does not depend on $N$, it will not be taken into account as we investigate the change in the free electrostatic energy with different numbers of added electrons. As shown in Figure 1-7, the electrostatic energy of the system is
proportional to $q_g^2$ and different numbers of added electrons on the island (N) just shifts the parabola along the x-axis.

Figure 1-7 Electrostatic energy of the system as a function of gate induced charge. Adjacent parabolas show how the electrostatic energy changes when a certain number of electrons, written above the parabola, are added to the island.

As shown in the figure above and also in Figure 1-3, when no bias is applied and $V_g=0$, the energy needed to add the first electron to the island or remove the first electron from the island is $E_c$ (i.e. the energy difference between the red and green parabolas and the blue parabola at $V_g=0$).

The points at which the two adjacent parabolas cross are where the states that are different by one electron on the island and have the same electrostatic energy. Since the free electrostatic energy of the device is proportional to difference between the island charge and $q_g$, these points can simply be calculated as follows:
The derivation above provides us with the bias points at which the addition of an extra added electron to the island does not change the electrostatic energy of the system. For instance, consider the blue parabola with no added electron to the island (N=0). By increasing the $V_g$ bias, the electrostatic energy of the system is increased and at $V_g = e/2C_g$ it becomes equal to the energy of a system with one extra electrons. This point is equivalent to the energy states shown in Figure 1-5 (a), where the first available energy state on the island is aligned with source and drain Fermi levels. As a result, one electron can tunnel though the tunnel junctions and be added to the island. It should be mentioned that above $V_g = e/2C_g$, the energy of the system with one added electron to the island is lower than that with an empty island (the red curve of N=1 is lower than blue curve of N=0 beyond $V_g = e/2C_g$), and hence the tunneling of an extra electron to the island is energetically favorable at $V_g = e/2C_g$. By the same token, at all bias points of $V_g = (2N+1)e/2C_g$, where two adjacent parabolas cross, the one island energy state is aligned with source and drain Fermi level and transport of one electron to the island through the junctions is energetically favorable. These points represent peaks of Coulomb blockade oscillations. In contrast, in the $V_g$ range between the intersection points, there is no energy level of the island that is aligned with source/drain Fermi level. There is an energy barrier against the addition of any extra electrons, since it increases the electrostatic energy of the system and is not energetically favored. For instance, if $-e/2C_g < V_g < e/2C_g$, adding an electron to the island raises the energy from the blue curve (for N=0) to the red curve (for N=1) which has a higher energy. Therefore, the conduction between the source and drain in blockaded for that region. The Coulomb
blockade oscillations (CBO) for a simulated device with $C_d=C_s=10$ aF, $C_g=2$ aF, and $R_s=R_d=200$ kΩ at 300mK is shown in Figure 1-8.

![Coulomb blockade oscillation](image)

Figure 1-8 Coulomb blockade oscillation of an SET device with $C_d=C_s=10$ aF, $C_g=2$ aF, $R_s=R_d=200$ kΩ

As it is clear for the simulated device with $R_s=R_d=200$ kΩ, the peak of CBO ($G=12.5$ µS) is half of the conductance through the device ($G_0=25$ µS), since in the peak of CBO, only one energy state on the island is aligned with source/drain Fermi level and enables the conduction through the device. When the island is populated with one extra electron and the energy state is filled, the conductance through the tunnel barriers is restricted, and since the island is populated with one electron 50% of the time, the conductance through the barriers is suppressed 50% of the time. As a result, the conductance in the peaks of CBOs is half of the high temperature ($T>>E_c/k_B$) value ($G_0$) in which the Coulomb blockade is suppressed by thermal fluctuations.
In an SET, the drain terminal is not grounded and therefore the bias that is applied to the drain can also change the electrostatic energy of the SET and hence control the tunneling of electrons through the tunnel junctions. The charging diagram which displays the so-called “Coulomb diamonds” of an SET is an instrumental plot that shows the conductance variations as a function of $V_{ds}$ and $V_g$. Figure 1-9 shows the charging diagram of a single electron transistor with $C_d=C_s=10\,\text{aF}$, $C_g=2\,\text{aF}$, and $R_s=R_d=200\,\text{k}\Omega$ at 300mK that was simulated based on orthodox Coulomb blockade theory for a metal dot, using code developed by M. Pierre\textsuperscript{10}. The model used here does not take higher order events, e.g. co-tunneling, into account and is valid for junction resistance greater than.

Figure 1-9 The charging diagram, showing “Coulomb diamonds” of the simulated SET with $C_d=C_s=10\,\text{aF}$, $C_g=2\,\text{aF}$, and $R_s=R_d=200\,\text{k}\Omega$ at 300 mK
In Figure 1-9, the black diamonds in the middle row correspond to the Coulomb blockade in a range of drain and gate voltages where there is no available energy states in the island placed between the source and drain Fermi levels, and hence the conductance is strongly suppressed by a factor of $\sim \exp(\Delta E_c/k_B T)$, and the number of electrons on the island is constant. In this region, there is an energy barrier (with max value of $E_c$) for tunneling of electrons since it is energetically unfavorable. The points on $V_g$ axis where the diamonds meet correspond to the bias values where the electron tunneling is energetically favorable and therefore one electron is either added to or removed from the island. Therefore, the number of electrons that are on the island is different by one electron in the adjacent diamonds. The diamonds in the first row from the center (both above and below) represent a range in the bias where Coulomb blockade is lifted and one electron at a time tunnels from one lead to the island and then leaves the island towards the other lead. Since in this range only one island state is aligned between the source and drain Fermi level (Figure 1-10 (a)), the added electron to island must leave the island before the next electron can enter the island, and as discussed above, the conductance is half of $G_0$. The second row away from the center (Figure 1-10 (b)) represent a range at which two electrons at a time can tunnel to the island since two available states on the island are aligned between the source and drain. The farther rows represent a higher number of electrons that can enter the island at once.
Figure 1-10 (a) The alignment of energy levels for the diamond of the first row below the Coulomb blockade diamonds. For these diamonds, one available energy level on the island lies between the source and drain Fermi levels. (b) The alignment of energy levels for the diamond of the second row below the Coulomb blockade diamonds. For these diamonds, two available energy levels on the island lie between the source and drain Fermi levels.
Figure 1-11 shows the Coulomb diamond that is located at the origin where no electron is added to the island (N=0). From the shape of the diamonds in the charging diagram, different parameters of the device: $C_g$, $C_d$, $C_s$, and $E_c$, can be easily extracted.

![Figure 1-11 Coulomb diamond of an SET located at the origin of $V_{ds}$-$V_{gs}$ axes](image)

The alignment of energy levels at point a, b, and c of the Figure 1-11 is depicted in Figure 1-12; While (a) represents no applied bias to the device, (b) and (c) represent a $V_{ds}$ bias at which the drain (source) is aligned to the lowest unfilled available energy on the island, and source (drain) is aligned to highest filled energy state on the island.
Figure 1-12 The alignment of energy levels at point a, b, and c of the Figure 1-11; (a) represents no applied bias to the device, (b) represents a $V_{ds}$ bias at which the drain is aligned to the lowest unfilled available energy on the island, and source is aligned to highest filled energy state on the island, (c) represents a $V_{ds}$ bias at which the source is aligned to the lowest unfilled available energy on the island, and drain is aligned to highest filled energy state on the island.

To derive the positive and negative slopes of the diamond, let us first write the potential of the island with respect to source and drain, separately.

$$V_{is} = \frac{C_g}{C_t} V_{gs} + \frac{C_d}{C_t} V_{ds}$$

$$C_t = C_g + C_d + C_d = C_g + 2C_d$$

$$V_{di} = V_{ds} - V_{is} = V_{ds} (1 - \frac{C_d}{C_t}) = V_{ds} \left( \frac{C_s + C_g}{C_t} \right) - \frac{C_g}{C_t} V_{gs}$$
Where $V_{is}$ is the potential of the island with respect to the source and $V_{gs}$, $V_{ds}$ are the applied gate-source and drain-source bias, respectively. $C_t$ is the sum of gate, drain, and source capacitances: $C_t = C_g + C_d + C_s$.

In Figure 1-12 (b), two available energy states of the island are aligned to source and drain Fermi levels. By applying a positive $V_{gs}$ bias, the island potential is lowered and the highest filled state on the island is no longer contributing to the conduction since it is lower than both source and drain Fermi levels. The lowest unfilled state, however, will be placed between the Fermi level of the drain and source. The positive slope of the blockade diamond corresponds to a bias range at which drain Fermi level is kept aligned with the lowest unfilled state, so that no available energy state is placed between source and drain Fermi levels and the conduction is kept blockaded. As a result, the positive slope of the diamonds originates from keeping the island states aligned with the drain Fermi level.

$$V_{di} = V_{ds} \left( \frac{C_g + C_s}{C_t} \right) - \frac{C_s}{C_t} V_{gs} = 0 \Rightarrow \frac{V_{ds}}{V_{gs}} = \frac{C_g}{C_s + C_g}$$ (11)

In Figure 1-12 (c), two available energy states of the island are aligned to source and drain Fermi levels. By applying a positive $V_{gs}$ bias, the island potential is lowered and the highest filled state on the island is no longer contributing to the conduction since it is lower than both source and drain Fermi levels. The lowest unfilled state, however, will be placed between the Fermi level of the drain and source. To maintain the blockade in the diamond, the lowest unfilled state should be kept aligned with the island Fermi level so that no available energy state is present between source and drain Fermi levels.
As a result, the negative slope of the diamonds originates from keeping the island states aligned with the source Fermi level.

\[ V_{is} = \frac{C_s}{C_i} V_{gs} + \frac{C_s}{C_t} V_{ds} = 0 \Rightarrow \frac{V_{ds}}{V_g} = -\frac{C_s}{C_d} \tag{12} \]

As explained before, for \( V_{ds}=0 \) on \( V_g \) axis, the diamonds meet at the bias points where an island energy state is aligned with source and drain Fermi levels and there is a conduction path between the source and drain. Since the energy difference between the available states is \( 2E_c \), the period in \( V_g \) between two points of conduction (the period of the charging diagram) can be calculated as follows:

\[ V_{ds} = 0 \Rightarrow V_{is} = \frac{C_s}{C_i} V_g = \frac{2E_c}{e} = \frac{e}{C_t} \Rightarrow V_g = \frac{e}{C_g} \tag{13} \]

Knowing the positive and negative slope as well as the period of the diamonds, one can easily calculate that the height of the diamonds by calculating the point where the diamond crosses the \( V_{ds} \) axis:

\[
\text{negative slope: } \frac{V_{ds}}{V_g} = -\frac{C_s}{C_d} \Rightarrow V_{ds} = \frac{C_s}{C_d} \times \frac{e}{2C_g} = \frac{e}{2C_d} \tag{14}
\]

\[ \Rightarrow \text{Height of the diamonds} = 2V_{ds} = \frac{e}{C_d} = \frac{4E_c}{e} \]
1.4 Charge sensitivity of a single electron transistors

Charge sensitivity, $\delta Q_g$, in a SET as an electrometer is defined as follows\textsuperscript{11}:

$$\delta Q_g = \frac{\sqrt{\Delta F \ast S(0)}}{g_m}$$  \hspace{1cm} (15)

where $\Delta F$ is the equivalent noise bandwidth, $S(0)$ is the zero-frequency shot noise, and $g_m$ is the transconductance of the SET defined by $\delta I/\delta Q_g$.

As clear from the formula, to decrease $\delta Q_g$ for increased sensitivity, one can adjust the noise, bandwidth, and transconductance. The measurement bandwidth is changed by the time constant of the acquisition apparatus\textsuperscript{12}. Transconductance of the device depends on the $E_c/k_BT$ ratio and hence for certain charge sensitivity, a smaller SET can be operated at a higher temperature. Asymmetry in the tunneling resistance of the junctions also has been shown to increase the $\delta I/\delta Q_g$ due to the formation of Coulomb staircase in the SET current\textsuperscript{11}. As explained, both the measurement bandwidth and the transconductance of the device can the adjusted for improved sensitivity, but most importantly, the relatively small value of the noise energy for SETs has made these devices most sensitive electrometers to date\textsuperscript{13-15}. At SET operating temperatures, thermal noise is negligible, while $1/f$ noise and shot noise are the main noise sources. Flicker ($1/f$) noise represents the stochastic occupation of traps in the vicinity of the device, and can in principle be eliminated with improvement in the fabrication technology\textsuperscript{14, 16}. Therefore, the theoretical noise floor is set by the shot noise, which is reported to be suppressed below the classical Poisson shot noise (for a single tunnel junction) \textsuperscript{17}. Single electron
transistors are capable of detecting a fraction of elementary electron charge, as small as \( \approx 10^{-6} \, \text{e/\sqrt{Hz}} \). This characteristic of SETs has made them naturally suitable for detecting nanometer scale displacement, sensing single gas molecules, and readout sensors in atomic level computing architectures such as Quantum Cellular Automata (QCA).
CHAPTER 2:
DEVICE FABRICATION

2.1 Substrate preparation and marker fabrication

The first step in device fabrication is substrate preparation. Some of the requirements for a desired substrate include: smoothness, thermal and chemical stability at processing temperatures, no chemical reaction with materials from which the device is made, and good adhesion to the device materials. Different deposition methods for forming the insulation SiO₂ substrate have been studied.

Figure 2-1 A SiO₂ layer deposited on a Si wafer using plasma enhanced chemical vapor deposition
Figure 2-1 shows a SiO$_2$ layer deposited on a Si wafer using plasma enhanced chemical vapor deposition (PECVD) with 80 standard cubic centimeter per minute (sccm) of SiH$_4$ and 900 sccm of N$_2$O at 900 mTorr with plasma power of 25W at 250°C substrate temperature and 60°C heat exchange temperature. The roughness of the deposited SiO$_2$ increases the resistance of devices that have a thickness in the range of the SiO$_2$ surface roughness, and can even lead to breaks in these devices.

Based on our observations, the adhesion to the SiO$_2$ layer deposited using low-pressure chemical vapor deposition (LPCVD) is very poor, resulting in delamination of the deposited Ni layer during the chemical mechanical polishing (CMP) step. Thermally grown SiO$_2$, however, proved to be a smooth underlying layer for device fabrication that also provides satisfactory adhesion to the device. As a result, 350 nm of thermally grown SiO$_2$ on the Si wafer was used as the substrate for fabricating SET devices and all other test structures.

Since different components of the device must be aligned to one another, alignment markers that can survive all the processing steps are of great importance. Markers that are etched deep in the oxide and the underlying silicon wafer proved to be reliable and robust. These markers are easily detected by automated marker detection in 100 keV Vistec EBPG 5200 electron beam lithography (EBL) system.

In the EBL machine, the electrons backscattered from the markers are converted to light via florescence plates (scintillators). The light is then converted back to an electrical signal via photomultiplier tubes$^{21}$. In order to locate the markers, the signal (video level) reflected from the substrate and the markers have to be distinguishable, and
this imposes some important factors in designing the markers. Markers with higher and lower backscattered electron yield than the substrate are referred to positive and negative markers, respectively. Positive markers with 50 nm of high atomic number metals like Pt and Au can be located with auto marker detection. However, since the processing steps for SET fabrication includes high temperature (400°C) treatment and CMP, these markers are damaged during the fabrication and cannot be re-used for the next alignment. We therefore designed and successfully made 4×4 |m^2 negative markers. For this purpose, photolithography and subsequent etching steps were used to transfer the marker pattern into the substrate as shown in Figure 2-2.

![Figure 2-2 Schematic of the steps for fabricating alignment markers](image)

First, SPR 700-1.2 positive-tone photoresist, with a nominal required dose of 130 mJ/cm^2, is spun on the substrate at 4000 revolutions per minute (rpm) for 60 seconds and baked at 90°C for 60 seconds, giving a resist thickness of \( \approx 2 \) μm. Exposure of the pattern was performed in an RTS AutoStep 200 i-Line wafer stepper with a 0.26 sec exposure time at each step. The resist was then developed in MIF-917 for 45 seconds upon exposure (Figure 2-2 (a)). After the marker pattern was developed in the resist, SPR 700 was used as a mask to etch the pattern into the oxide and the Si layer under the SiO\(_2\). A
Plasmalab System 100 inductively coupled plasma - reactive ion etcher (ICP-RIE), from Oxford Instruments is used to transfer the marker pattern from the photoresist into the 350 nm of SiO$_2$ during a 70 sec etch step using a fluorine-based chemistry at 8 mTorr composed of 20 sccm Ar, 5 sccm C$_4$F$_8$, 15 sccm CHF$_3$, and 20 sccm CF$_4$. The RIE power of 150 W and the ICP power of 1000W result in a DC bias of 290V and a SiO$_2$ etch rate of 360 nm/min (Figure 2-2 (b)). Following the oxide etch and revealing the top surface of the Si wafer, the sample is dipped in buffered hydrofluoric acid (BHF) for two seconds to remove any native oxide formed on the Si surface by exposure to atmosphere after the oxide etch. Next, Memstar XeF$_2$ etcher is used to etch the underlying Si. XeF$_2$ is used to isotropically etch Si (Figure 2-2 (c)) with great selectivity with respect to photoresist, and silicon dioxide (around 1000:1). Etching the underlying Si in 200 sccm of XeF$_2$ added to 300 sccm of N$_2$ results in $\approx$4 µm deep trenches under the alignment marks within 30 seconds. Our experiments have confirmed that this method for making deep trenches in Si provides enough contrast for auto-marker detection.

It should be mentioned that since the devices are bonded to a chip carrier for final characterization, bond pads must be deposited on the sample to provide electrical access to the fabricated structures. These pads are defined in a photolithography step, which is the last step in the fabrication process. As a result, alignment marks for this photolithography step are also formed along with the EBL marks.

After the etched alignment marks are fabricated in the substrate, the wafer is diced into 15×15 mm$^2$ chips for individual processing. Only 15×15 mm$^2$ and 10×10 mm$^2$ chips fit in the wafer carrier of the Logitech Orbis CMP system, so the larger chip size was chosen to process more devices at a time and to increase the throughput.
2.2 SET fabrication

As explained in detail in chapter 1, one of the most important components of SETs is the tunnel barrier. The electrical properties of the dielectric barrier like band gap, electron affinity, dielectric constant as well as its thickness are among the main parameters determining the junction capacitance and resistance. Previously, only native metal oxides (e.g. Al, Cr, Ti, and Ni) formed the tunnel barriers in metal-based SETs, yielding a higher tunnel junction capacitance due to their high dielectric constants\textsuperscript{22-26}. However, our group is among the pioneers in using atomic layer deposition (ALD) to form $\text{Al}_2\text{O}_3$ tunnel barrier on Pt for metallic SETs\textsuperscript{27}. The cyclic deposition of ALD, with one monolayer of the desired material deposited in each cycle, makes it a controllable and precise method to form ultrathin tunnel barriers. Moreover, the use of ALD enables formation of low-k $\text{SiO}_2$ for example, that is not a metal native oxide, on a metal substrate.

The main goal of this research project is to use plasma enhanced ALD (PEALD) to form a tunnel transparent barrier in metallic SETs. PEALD has gained significant attention in the past few years due to a more efficient nucleation, lower required processing temperature, wider range of available materials for deposition, and higher film qualities compared to thermal ALD\textsuperscript{28}. Moreover, the metallic components of the SET, which form the electrodes in the tunnel junctions, were chosen to be made from Ni for the following reasons. First, since the fabrication of SETs includes CMP of the chosen metal, it must provide satisfactory adhesion to the substrate. We have shown that Ni can be easily polished during a CMP step, while the planarization of noble metals is quite challenging due to their chemical inertness and poor adhesion\textsuperscript{29}. Second, PEALD or ALD
of thin dielectric barriers are difficult on noble metals, whereas the hydroxyl groups on the oxidized surface of more reactive metals is believed to promote film nucleation in the PEALD process\textsuperscript{30-33}. Finally, although Ni is known to be more reactive than noble metals\textsuperscript{34}, it is more resistant to oxidation compared to Ti and Al. Moreover, the oxide formed on the surface of the Ni has been reported to reduce in H\textsubscript{2} containing ambient\textsuperscript{35, 36}. 

Here, I discuss the fabrication of Ni based SETs in form of crosstie structures and rib structures. The former has relatively easy processing steps, which results in a higher yield and enables us to characterize the fabricated metal-insulator-metal (MIM) tunnel junctions faster. Despite their challenging fabrication process, rib SETs provide a path for scaling down the SET devices beyond the constraints that are imposed by electron beam lithography, as will be explained in detail. Rib SETs are suitable for ultra-thin tunnel junctions, which lead to a higher temperature of SET operation.

2.2.1 Crosstie structures fabricated with liftoff

For electrical characterization of tunnel junctions with PEALD SiO\textsubscript{2} tunnel barrier, cross-tie test structures (Figure 2-3) with two tunnel junctions in series were fabricated as follows: Prior to starting the process, the diced chips are cleaned in acetone with ultrasonic agitation, and then rinsed in isopropyl alcohol (IPA), followed by a 10 min O\textsubscript{2} plasma cleaning in DryTek asher to completely remove any organic residue. Polymethyl methacrylate (PMMA) C2 from MicroChem is then spun on the substrate at 10000 rpm and is subsequently baked at 180°C for 3 minutes. Next, polymethylglutarimide (PMGI SF5) from MicroChem is spun on the substrate at 10000 rpm and baked at 180°C for 5 minutes to give a ~100 nm film. Later, in a Vistec EBPG 5200 EBL system, a 40 nm wide island (vertical line in Figure 2-3) with exposure dose of
6.5 mC/cm² was patterned on the resist stack with an electron beam current of 5 nA. PMMA-PMGI are then developed in Xylenes for 8 minutes while being ultrasonically agitated. The island pattern is then formed on the thermal SiO₂ with a 20 nm blanket Ni evaporation at < 8×10⁻⁷ Torr and liftoff in 80°C MR-Rem 400 resist stripper from Micro Resist Technology. Following the island fabrication, FlexAl PEALD system from Oxford instrument is used to form a dielectric barrier covering the island. The PEALD process parameters for SiO₂ deposition, with a nominal growth rate of 0.09 nm/cycle, are as follows. First, Bis(diethylamino)silane precursor (BDEAS) is introduced in the Oxford FlexAl chamber at 80 mTorr for 125 ms. After the first precursor is purged out of the chamber, 3 seconds of oxygen plasma (pressure of 15 mTorr and power of 300 W) replaces the ligands of the deposited BDEAS monolayer with oxygen. Following PEALD, 20 nm wide, 30 nm thick source and drain wires were defined by a second EBL, metal deposition, and liftoff. The relatively easy fabrication of these structures enables characterization of the PEALD tunnel barrier faster and leads to acquiring more data for a shorter processing time.
2.2.2 Crosstie SETs with an island inlaid in the oxide

These devices are similar to the structure explained above with a difference that the island is fabricated inlaid in the thermal SiO$_2$ substrate using a damascene process, as shown in Figure 2-4.
The use of chemical mechanical polishing in this process provides a path to achieve line widths smaller than those made with simple liftoff. Since the island is formed in a trench that is etched in the substrate, the profile of the trench determines the size of the island. Therefore, if the bottom of the trench is narrower than its top, CMP can be tuned to thin down the island and produce a narrower line. A narrower island leads to smaller junction capacitance between the island and the source and drain leads, \( C_d \) and \( C_s \). Moreover, the damascene island fabrication reduces the island area accessible to the source and drain from three sides of the island to just the top of the island, and can thus further decrease the junctions capacitance.
To fabricate the inlaid island devices, the following steps were performed: PMGI SF5 is spun on the chip at 2000 rpm, and then baked at 180°C for 5 min to form a ~250 nm layer of PMGI electron beam resist. The pattern of the island is exposed in PMGI during an EBL with a dose of 8500 µC/cm². PMGI is then developed in Xylenes for 10 minutes while being ultrasonically agitated. Based on our experiments, PMGI can be used as a mask for SiO₂ etch due to its better etch-resistance than PMMA. The Plasmalab ICP-RIE System 100 is used to transfer the island pattern from PMGI to the SiO₂ substrate in a 10 sec etch step using the fluorine-based chemistry explained above. The island is then filled with a 60 nm blanket Ni e-beam evaporation at base pressure of $7 \times 10^{-6}$ Torr. Following the evaporation, the evaporated Ni along with the underlying PMGI on the substrate is dissolved in MR-Rem 400 that is heated to 70°C. Next, 9 seconds of chemical mechanical polishing is used to remove the residual Ni left on the oxide, while leaving the island trench filled with Ni. Ultra Sol A19, alumina based slurry from Eminess at pH=4, diluted 50% with DI water is used as the polishing slurry. Platen and carrier head rotation speed of 60 rpm, slurry-dispensing rate of 125 ml/min, and 0.7-pound force per square inch (psi) of applied pressure on the wafer carrier result in a 360 nm/min Ni polish rate in the Orbis CMP system from Logitech. FlexAl PEALD system then used to form a dielectric barrier covering the island using the same recipe explained for liftoff structures. In addition to SiO₂, Al₂O₃ can also be deposited in FlexAl PEALD system using trimethylaluminum (TMA) and oxygen plasma. During TMA introduction in the first step of PEALD, chamber pressure is held at 15 mTorr for 40 msec, while the pressure is held at 15 mTorr for 2 sec during the 250 W plasma step of 40 sccm Ar + 60
sccm O₂. The described PEALD recipe has a nominal Al₂O₃ deposition rate of 0.11 nm/cycle.

After the dielectric barrier is formed, the source, drain, and gate terminals of the SET are formed on the substrate. A second EBL step exposes the patterns of these terminals, with the same dose as for the island, on a 100 nm PMGI layer that was spun on the substrate at 10,000 rpm, and baked as previously explained. Following the 5 minute-developing in Xylenes, 30 nm of Ni is evaporated as previously described, and then the metal evaporated on the e-beam resist is lifted off the substrate when PMGI is dissolved in MR-Rem 400 at 70°C. The micrograph of the device using high-resolution transmission electron microscopy (HRTEM), courtesy of Dr. Sergei Rouvimov, is shown in Figure 2-5.
Figure 2-5 HRTEM image of the crosstie SET with an inlaid island. (a) The whole fabricated device. (b) Tunnel junction on the left. (c) Tunnel junction on the right.
2.2.3 Damascene rib SETs

Figure 2-6 shows the schematic of rib SET fabrication steps. The proposed self-aligned process enables fabrication of ultra-small tunnel junctions, down to a few nm in each dimension, and thus using this process, an operating temperature of the SET up to 70K should be possible.

Figure 2-6 Schematic of nanodamascene SET fabrication steps: (a) Island pattern is exposed on PMGI during an EBL. (b) The developed PMGI is used as a mask to transfer the island pattern in the underlying oxide with an ICP etch step. (c) PMGI is removed from the sample, and a blanket Ni evaporation is performed on the sample (d) In a CMP step, metal overburden is polished off the sample leaving the island trench filled with Ni, as shown in the image taken with scanning electron microscopy (SEM). (e) During a second EBL and ICP etch, the pattern of the source and drain is transferred to the thermal SiO$_2$ substrate. (f) PEALD is used to form the dielectric barrier on the island. (g) Blanket Ni evaporation fills the source and drain trenches. (h) Ni overburden on the thermal SiO$_2$ field is polished away during a second CMP, the SEM image shows the junction between the island, source, and drain.
First, PMGI SF5 is spun on the substrate at 2000 rpm and is subsequently baked at 180°C for 5 minutes to give a 250 nm film. The pattern of the 30 nm wide island is exposed in PMGI during an EBL step with an area dose of 6.5 mC/cm². Following the exposure, the PMGI is developed in Xylenes for 12 minutes using ultrasonic agitation (Figure 2-6 (a)). Using the same recipe for the ICP-RIE plasma step, the pattern of the island is transferred from PMGI to the SiO₂ substrate during a 15 sec etch step (Figure 2-6 (b)). MR-Rem 400 heated to 70°C, is used to strip the PMGI mask. Next, the etched island trench is filled with Ni in a blanket 100 nm Ni evaporation (Figure 2-6 (c)). A Ni CMP step similar to that previously described removes the Ni in the field, leaving only the Ni in the island trench (Figure 2-6 (d)). After polishing away the metal overburden on the oxide, a perpendicular line to the island is written in PMGI during the second EBL to form the pattern of the source and drain. A similar ICP-RIE etch recipe is used to transfer the pattern into the SiO₂ (Figure 2-6 (e)). It is worth mentioning that the plasma etch recipe is designed to leave vertical sidewalls in the oxide. A re-entrant profile in the island (where the angle between the sidewalls and the bottom of the trench is more than 90°) results in an undercut in the adjacent source and drain trench, which is challenging to refill with metal evaporation. The resulting unfilled voids lower the fabrication yield. Next, MR-Rem 400 followed by a 10 sec ashing step in DryTek plasma asher strips PMGI from the substrate, and tunnel barrier is formed on the island with a PEALD process (Figure 2-6 (f)). Following the PEALD, the residual carbon on the deposited tunnel barrier must be cleared with a 10 sec ashing step in Drytek plasma asher. Based on our observations, the two ashing steps mentioned above play an important role in the adhesion of Ni to the dielectric and can significantly affect Ni CMP results since poor
adhesion of the metal to the substrate leads to metal delamination during the CMP step. Next, 200 nm blanket Ni is deposited by e-beam evaporation (Figure 2-6 (g)), and in a 25-sec CMP step, with the similar conditions as mentioned above, the Ni on the field is removed, leaving the trenches filled with metal (Figure 2-6 (h)). By controlling the depth of the final CMP polishing step, the depth and hence the cross-sectional area of the device can be reduced, which can give a higher charging energy.

Figure 2-7 shows a rib SET that is imaged with a scanning electron microscope (SEM). The 500×500 nm² pad is attached to the island to make it visible in the optical microscope. In a subsequent batch of devices, this pad has been detached from the island to further reduce its capacitance.

Figure 2-7 SEM image of a nanodamascene rib SET device
The final step following the fabrication of the nanostructures is forming the bonding pads that are connected to the devices and are necessary for performing the electrical measurements. Pattern of the pads is first exposed on a 2 \( \mu \)m-thick nLOF 2020, a negative tone photoresist, which is spun on the substrate at 4000 rpm for 45 seconds and then baked for 60 seconds at 90°C. Pattern exposure is performed in the RTS AutoStep 200 i-Line wafer stepper with a 0.17 sec exposure time in each step. Following the exposure, the resist should be baked for 1 min at 100°C and then developed in MIF-917 caustic developer for 45 seconds. Prior to metal evaporation, a 10 second descum in the DryTek plasma asher is performed to remove the residual organic contaminants on the surface and enhance the adhesion of the metal to the substrate. Finally, a 100 nm blanket Ni evaporation forms the bond pads on the substrate. Figure 2-8 shows the optical micrograph of a die that includes SET devices connected to bond pads so they can be measured on a probe-station or bonded to a chip carrier for detailed analysis and measurement.
Figure 2-8 An optical micrograph of a die with fabricated SETs that are accessible for measurement with the bond pads that are connected to these devices.
CHAPTER 3:
EXPERIMENTAL RESULTS

After fabrication, the differential conductance of the devices, \( \frac{dI_{ds}}{dV_{ds}} \), is measured at room temperature using lock-in techniques on a probe-station. Depending on the conductance range, a 1 or 10 mV RMS AC signal (higher AC signal is required to improve SNR in devices with \( G < 1 \text{ nS} \)) is applied between the source and the drain of the device at 10-50 Hz. Devices with conductance in the range of 10 nS-20 \( \mu \text{S} \) are selected for further measurements at low-temperatures. However, before measuring the devices at low temperatures, the sample must be cleaved into smaller \((\leq 10 \times 15 \text{ mm}^2)\) pieces to fit into a chip carrier. Smaller pieces are then wire bonded to the ceramic chip carrier with 24 pins (Figure 3-1), and then depending on the desired measurement temperature, are placed in either \(^3\text{He} \) Janis or \(^4\text{He} \) ARS closed cycle cryocoolers.

Figure 3-1 A ceramic 24-pin chip carrier to which the cleaved sample is glued and the bond pads are wire-bonded

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ARS cryocooler is capable of cooling the device down to 3.5K, while the Janis $^3$He refrigerator has a base temperature of $\approx$300mK. The sample temperature is monitored by a thermometer glued directly to the chip carrier. To measure the differential conductance through the devices at low temperatures, up to 4 Stanford Research 830 lock-in amplifiers (LIA) are used in parallel. To improve the signal to noise ratio, the devices under test (DUT) are connected to a trans-impedance battery-powered four-channel preamplifier located at the top plate of the cryostats as shown in Figure 3-2. The excitation voltage is chosen to avoid significant smearing of the device characteristics at a given temperature: $v_{ac} \times e \approx k_B T$. The use of higher frequency for AC probing signal enables the use of a lower time constant, and therefore faster data acquisition is possible at higher frequencies. However, for the devices studied here, the values of conductance are typically below 0.1 $\mu$S, and since in our acquisition setup the wires used to connect the source and the drain are unshielded, there is a significant parasitic capacitance between these wires (at least 100pF). As a result at frequencies $>200$ Hz, the out of phase displacement current exceeds the current through the device, and compromises the measurement accuracy. Therefore, the frequency used for the excitation signal was kept $<200$ Hz in all measurements.
We start the report of the electrical measurements with the first fabricated device in which the PEALD of Al$_2$O$_3$ formed the tunnel barrier in the nanodamascene rib SET. No treatments for reducing the parasitic NiO were performed on this device. However, observing the deviation of the performance of this batch from that expected based on MIM SET led us to pay a closer attention to junction formation and PEALD interaction with the substrate.

3.1 Nanodamascene SET with Al$_2$O$_3$ tunnel barrier

Electrical measurement of the nanodamascene SET that is fabricated using the process flow described in chapter 2 with 9 cycles of Al$_2$O$_3$ PEALD as the tunnel barrier is performed with a 0.3 mV excitation voltage at 38 Hz. The wire-bonded sample is attached to the $^3$He pot of a closed cycle refrigerator.
The Coulomb blockade oscillations of the differential drain-source conductance, \( G_{ds} \), as a function of gate voltage, at \( V_{ds}=0 \) and \( T \approx 0.46 \)K are shown in Figure 3-3.

![Coulomb blockade oscillations](image)

Figure 3-3 Coulomb blockade oscillations of the device measured at 0.46 K

The very large noise, clearly visible in Figure 3-3, is far greater than thermal and shot noise expected at the temperature of measurements for a given device conductance. If measured versus time, conductance of the device randomly switches between peaks and the valleys of CBOs and in that sense peaks and valleys can only be “probabilistically” defined, meaning that the probability of measuring a large value of conductance (CBO peak value) is higher around \( V_g = -7.5 \) mV than near \( V_g = -5 \)mV. Likewise, the low value of conductance near \( V_g = -5 \) occurs with higher probability than the high value of conductance. This type of behavior is indicative of the “random telegraph signal” (RTS) noise. RTS noise in SETs has already been studied and is attributed to stochastic electron entrapment and release by the single traps in the
proximity of the island (the tunnel barrier, nano particles positioned near the island, etc.) \textsuperscript{39-41}. Since in the fabricated devices, the traps are most likely in the dielectric tunnel barrier or in the dielectric-metal interface of the junctions, they can change the potential of the island and result in abrupt change in SET conductance on the order of the CBO magnitude. The observed noise is significantly different from that in SET devices fabricated by Dolan bridge technique in which the tunnel barrier was formed by in-site oxidation of metal layers that formed the island\textsuperscript{3}. We show below that by employing appropriate treatments, it is possible to alleviate the noise in fabricated MIM junctions.

The Coulomb diamond plot of the device is shown in Figure 3-4 (a). For comparison, we performed simulations of the charging diagram, Figure 3-4 (b), based on orthodox Coulomb blockade theory for an MIM SET with $C_d=C_s=145 \text{ aF}$, $G_d=G_s=150 \text{ nS}$, and $C_g=21 \text{ aF}$ at 0.46K, using code developed by Pierre et al. \textsuperscript{10}.
Figure 3-4 (a) Coulomb diamonds of the fabricated nanodamascene SET measured at 0.46K, (b) Simulated Coulomb diamonds with $C_{d}=C_{s}=145$ aF and $C_{g}=21$ aF
The value of gate capacitance is chosen to replicate the period of Coulomb blockade oscillations while the values of junction capacitances are chosen based on the sample geometry: assuming a parallel-plate capacitor model, a 45 nm wide, 40 nm deep rib is expected to result in junction capacitance of $C_d=C_s=\varepsilon_c \varepsilon A/d=143$ aF, where $\varepsilon_c$ and $\varepsilon = 9$ are respectively the vacuum permittivity and the dielectric constant of Al₂O₃, A is the junction area, and $d\sim1$nm is the thickness of 9 cycles Al₂O₃ tunnel barrier, based on the 0.11 nm/cycle nominal growth rate. The expected charging energy based on geometry is 0.27 meV. Although Coulomb diamonds in the blockaded regions of Figure 3-4 (a) are distinguishable and the height of the diamonds in $V_{ds}$ is similar to the simulations, there is a noticeable discrepancy between theoretical predictions and the experimental observations outside the central diamonds.

First, there is a significant discrepancy between the expected peak value of CBO considering the room temperature conductance $G_\text{o}=1$ µS, and the experimental result $G_\text{p}=18$ nS. Based on theory explained in chapter 1, the peak of CBO is half of the high-T conductance ($G_\text{o}$). However, for the fabricated device measured at 0.46K, the differential conductance at peaks of CBOs is by more than an order of magnitude smaller than the room temperature value.

Figure 3-5 (a) shows an experimental $G_{ds}(V_{ds})$ dependence measured at a peak of CBO at $V_g=8$ mV (solid curve), along with the $G_{ds}(V_{ds})$ for the simulated device (dashed curve). To get a comparable scale in the $y$-axis, the conductance of both devices is normalized. Clearly, in the simulations, $G_{\text{norm}}$ changes from 0.5 at $V_{ds}=0$ to $\approx1$ at $V_{ds}=3$ mV, whereas in experiment, $G_{\text{norm}}$ decreases well below 0.5 at $V_{ds}=0$. There is also a noticeable asymmetry in the experimental curve, which will be discussed below.
Due to the suppression of conductance at 0.36 K by approximately one order of magnitude below the room temperature value for $|V_{ds}| >> E_c/q$ as well as significant discrepancy between the expected Coulomb dip magnitude and experimental results, it is therefore reasonable to assume that there must be a parasitic thermally activated resistive component in series with the tunnel junctions, as schematically illustrated in Figure 3-5 (b), that results in the observed deviations from the simulated MIM SET characteristics. The most probable origin for the parasitic layer is the formation of NiO during the oxygen plasma steps in the PEALD process. The oxidizing effect of the O$_2$ plasma during the PEALD has already been studied for different metallic substrates$^{42, 43}$, and later discussions here also confirm the formation of parasitic NiO layers during the PEALD process.

We also believe that the noticeable asymmetry in the experimental data of Figure 3-5 (a) can be attributed to a random non-uniformity in the parasitic oxide layer in the junctions that results in one less favorable current direction. This type of deviation from linearity is fairly common phenomenon in mesoscopic samples$^{44}$. 
Figure 3-5 (a) Differential conductance of the fabricated and simulated devices vs. DC bias applied across source and drain ($V_{ds}$) for $V_g=8$ mV, where $G(V_g)$ is at maximum. In the simulations, the conductance is normalized by the $G_0$ (i.e. $G(V_{ds} >> E_C/e)$ and in the experimental data, the $G(V_{ds}=3mV)$ is used for normalization ($V_{ds}=3mV >> E_C/e$).

Schematic diagram of the parasitic NiO formed in the drain-island and source-island junction as the island is subjected to the O$_2$ plasma step in PEALD of Al$_2$O$_3$. The top surface of the island is also oxidized but is most probably polished away during the second CMP step.
In order to confirm the non-ideal behavior in the tunnel junctions, several batches were fabricated and consistently showed the presence of a thermally activated component in the device. Figure 3-6 shows the SEM image of the fabricated nanodamascene SET device in which the dimensions of the tunnel junctions were intentionally made relatively large to increase the junction capacitance and thus reduce the associated charging energy. Therefore, the suppression of conductance at low temperatures due to the activated transport will dominate the Coulomb blockade effect. $G_{ds}(V_{ds})$ as a function of temperature for the nanodamascene device with 12 cycles of PEALD SiO$_2$ as the tunnel barrier is shown in Figure 3-7. No additional treatments were performed on the tunnel junctions of the SET after fabrication.

Figure 3-6 SEM image of an SET with 110 nm wide- 60 nm deep tunnel junctions, intentionally fabricated to diminish the charging energy and Coulomb blockade
Figure 3-7 $G(V_{ds})$ as a function of $T$ for a nanodamascene device with 12 cycles of PEALD SiO$_2$ as the tunnel barrier and with no treatments on the junctions following the fabrication.

Clearly, the conductance shows nonlinearity for high bias values as opposed to that expected from the Coulomb blockade. Moreover, the suppression of conductance by a factor of 100 at 4.8K is not expected to originate from Coulomb blockade of an island with a 0.3 meV charging energy. As a result, it is reasonable to believe that the parasitic component present in the tunnel junctions plays the dominant role in determining the conductance.

To summarize, the presence of the parasitic layer, which is most likely the NiO formed during the PEALD, has been observed to significantly modify the behavior of the fabricated SETs and, therefore several techniques have been employed in this project to reduce the parasitic NiO to a metallic Ni and restore the MIM characteristics of the
junctons. Below, we describe a set of experiments performed to study the formation of the parasitic NiO and the approaches taken to reduce the NiO layers in order to make the behavior of the SET devices as close to the one with ideal MIM junctions as possible.

3.2 Investigating the NiO formed during the PEALD of SiO$_2$

To investigate plasma interaction with Ni nanostructures during the barrier formation and to determine the optimal number of PEALD cycles needed to form the dielectric barrier with the desired thickness, two types of test structures were fabricated on a Si wafer covered with 300 nm thermally grown SiO$_2$: (1) a cross-tie device structure, forming two Ni-SiO$_2$-Ni tunnel junctions in series (the fabrication steps for these structures are explained in chapter 2), and (2) single layer nanowires covered with PEALD SiO$_2$.

For cross-tie devices, reference (Ni-Ni) structures, where the PEALD and therefore the associated oxygen plasma exposure was omitted, were first fabricated and exhibited conductance of $G\approx 0.4$ mS between the terminals, which is comparable with the conductance of a nanowire with similar dimensions. However, in devices with only 2 SiO$_2$ PEALD cycles ($\approx 0.2$ nm of expected thickness of SiO$_2$ tunnel barrier) the conductance dropped below $G\approx 5$ nS. This value is about 4 orders of magnitude smaller than the expected value of $G\approx 50$ $\mu$S, calculated from Simmons approximation for 0.2 nm of uniform SiO$_2$ dielectric barrier in the tunnel junctions$^{45}$. We have found that after annealing at 400°C for 2 min in 5% H$_2$-95% Ar ambient, the fabricated structures with 2 PEALD cycles of SiO$_2$ exhibit a drastic increase in conductance from $G \approx 5$ nS to $G > 600$ $\mu$S.
The lower than expected conductance in the untreated devices with 2 PEALD cycles likely results from NiO layers that are parasitically formed in series with the tunnel barrier during the PEALD process. Note that for the cross-tie structures, the contribution of in series parasitic layer to the total conductance can dominate if its conductance is lower than that of the PEALD barrier: \( G_{\text{total}} = G_{\text{TJ}} \times G_{\text{parasitic}} / (G_{\text{TJ}} + G_{\text{parasitic}}) \approx G_{\text{parasitic}} \) if \( G_{\text{parasitic}} \ll G_{\text{TJ}} \).

NiO has been shown to be reduced to Ni by annealing the oxidized film in hydrogen at temperatures above 300°C, and therefore the increase in conductance by 5 orders of magnitude upon annealing the structures in forming gas at 400°C is consistent with hydrogen promoted reduction of the parasitic NiO to Ni. The resulting conductance (\( G > 600 \mu S \)) is much greater than \( G \approx 50 \mu S \), expected for a uniform, pinhole-free 0.2 nm of oxide barrier. This is most likely due to non-uniformities in the deposited two monolayers of SiO\(_2\), which lead to “pinholes” where the top and bottom Ni electrodes are shorted. Moreover, as discussed below, the increase in Ni grain size caused by the anneal results in reduced electron scattering though the devices, and therefore a higher conductance than that of reference (Ni-Ni) structure is observed.

The thickness of the NiO layer formed during the PEALD step was estimated based on the conductance change of the 20 nm-thick Ni nanowires (Figure 3-8) after being covered with 10 cycles of SiO\(_2\).
Figure 3-8 Ni nanowires fabricated with EBL and liftoff. The conductance of the wires were measured before and after being covered with PEALD SiO\(_2\) barrier, and the thickness of the NiO was calculated based on the observed change in resistance.

After the PEALD process, the Ni nanowires exhibited a decrease in conductance from 1.3 mS to \(\approx\)1 mS (the series resistance of the access probes, \(\approx\) 100 \(\Omega\), is taken into account in these estimates). The decrease of conductance in the nanowires can be interpreted as a decrease in their conducting cross-sectional area by formation of \(\approx\) 2 nm NiO on the surface of the wires. Based on our observations, after annealing at 400°C for 30 min in 5% H\(_2\)-95% Ar ambient, the PEALD SiO\(_2\) coated Ni nanowires exhibit an increase in conductance to a level about 30% above that of the as-deposited metal. This result can be interpreted as a cumulative effect of two phenomena: a) reduction of NiO, and b) reduced electron scattering along the wire as a result of the grain size increase caused by the anneal, which results in a higher conductance\(^{48}\).
3.2.1 Reducing the parasitic oxide with rapid thermal anneal (RTA)

Using the proposed anneal step to reduce the parasitic NiO formed during PEALD on the Ni SET island, we fabricated cross-tie structures in which the island was treated in 5% H$_2$-95% Ar ambient at 400°C for 30 min after being covered with the PEALD tunnel barrier and prior to formation of the source/drain on top of the barrier. Our experiments show more than a 10× increase (from <0.15 nS to 2 nS) in conductance through the structures with 5 cycles of SiO$_2$ barrier. The 2 nS conductance through the device with 5 cycles of SiO$_2$ tunnel barrier and annealed island, however, is still far smaller than that expected based on the Simmons approximation (~1 µS). As a result, we conclude that in addition to the NiO formed on the bottom Ni electrode, there must be another parasitic layer in the tunnel junctions, which results in a lower than expected conductance. To further investigate this assumption, we studied the interface between the top Ni electrode and the PEALD SiO$_2$ using high-resolution transmission electron microscopy (HRTEM).

Figure 3-9 (a) shows an HRTEM image of 40 cycles of PEALD SiO$_2$ between two Ni films. A relatively thick SiO$_2$ is deposited to improve the identification of NiO at the top interface. Figure 3-9 (b) shows the elemental composition and concentration in 0.1 nm spaced data points along the red arrow in Figure 3-9 (a) extracted from energy dispersive X-ray spectroscopy (EDX). The points 2-6 denote the area near the top Ni-SiO$_2$ interface where the presence of NiO can be inferred from the pronounced oxygen content in the vicinity of the top Ni electrode that is more than twice the Si concentration, for a stoichiometric SiO$_2$. It should be mentioned that the maximum 20% concentration of Ni is due to the dominating presence of copper (~80%) resulting from the copper grid that is supporting the sample in the TEM system.
Figure 3-9 (a) The TEM image of a Ni-SiO$_2$-Ni structure fabricated with 40 cycles of PEALD SiO$_2$. (b) Elemental composition along the red arrow in (b): at the top Ni-SiO$_2$ interface, oxygen concentration is more pronounced than Si, suggesting the presence of NiO. Technical help of Dr. Sergei Rouvimov in acquiring the TEM and EDX data is highly appreciated.
The main cause of oxidation in the top Ni layer remains to be determined, but the oxidation of metals when deposited on SiO₂ has been reported for Cu, Mo, and W and has been attributed to the oxygen containing contaminants, such as water, on the oxide⁴⁹, ⁵⁰. Based on our experiments explained below, the top NiO can be reduced to Ni during a second anneal for 10 min at 400°C in 5% H₂ -95% Ar. Figure 3-10 shows the process schematic of Ni-SiO₂-Ni tunnel junction fabrication, illustrating where the parasitic NiO layers are formed and then reduced during the tunnel junction fabrication.
Figure 3-10 Schematic of parasitic NiO formation during Ni-SiO$_2$-Ni tunnel junctions. a) The Ni bottom electrode is evaporated on the substrate. b) The PEALD of SiO$_2$ forms the tunnel barrier on the bottom Ni electrode. Additionally, NiO is also formed on the surface of the bottom Ni due to the oxidizing effect of the O$_2$ plasma steps in PEALD of SiO$_2$. c) The underlying NiO is reduced when the SiO$_2$ covered Ni is annealed in H$_2$ containing environment at 400 °C for 30 minutes, while the SiO$_2$ layer remains intact. d) Ni top electrode is evaporated atop the SiO$_2$. The bottom of the top Ni electrode is oxidized due to residual oxygen containing contaminants on the SiO$_2$. e) The parasitic NiO on the top layer is reduced when the fabricated structure is annealed in H$_2$ containing environment at 400 °C for 10 minutes.
Based on our observations, all of the crosstie devices with 2, 5, 8, and 10 cycles of PEALD SiO$_2$ as the barrier exhibit a conductance greater than 400 $\mu$S when prior to formation of the source/drain on the PEALD SiO$_2$ covered island, the NiO layer formed on the island is reduced for 30 min at 400°C in 5% H$_2$-95% Ar and the top NiO, formed on the bottom of the source/drain, is reduced in the same conditions for 10 min after the source/drain are defined. In contrast, after the two reducing treatments, the average conductance for devices with 12 or 13 cycles of SiO$_2$ as the tunnel barrier is 0.1 $\mu$S, which is consistent within an order of magnitude of the expected tunneling conductance through a $\approx$1.1 nm of SiO$_2$ barrier$^{45}$. We attribute these results to non-uniformities in the PEALD films that are more detrimental for thinner dielectrics, and lead to a high conductance after the parasitic NiO layers in the junctions are reduced.

From the fabrication of crosstie devices it was concluded that 12-13 PEALD cycles of SiO$_2$ is suitable for Ni-SiO$_2$-Ni tunnel junctions in SET devices since the resulting conductance is sufficiently below the quantum conductance, $G_q \approx 40$ $\mu$S, required for suppression of quantum fluctuations in single electron transistors$^{9,8}$, yet high enough (>10 nS) to avoid signal-to noise ratio degradations due to excess Johnson noise.
3.2.2 Single electron transistors made with double RTA

3.2.2.1 SiO$_2$ tunnel barrier

Using the proposed annealing steps to reduce the top and bottom parasitic NiO that are formed in the junctions, we fabricated crosstie structures with inlaid island. The NiO formed on the inlaid island during the PEALD is reduced during a 25-min anneal at 400°C in 5% H$_2$ -95% Ar and the top NiO formed on the bottom of source and drain is reduced in the same conditions for 10 min after the source and drain are deposited on the island. Figure 3-11 shows an SET device that is fabricated using the two-step reduction of NiO with reducing RTA.

Figure 3-11 SEM image of a crosstie SET with inlaid island and reduced NiO in the junction
Electrical measurement of the device is performed with a 100 µV excitation voltage at 38 Hz and at the temperature of 0.34K. Figure 3-12 (a) is the measured charging diagram of the shown device. For comparison, we performed simulations of the charging diagram, Figure 3-12 (b), based on orthodox Coulomb blockade theory for a metal dot using $C_s=40.1$ aF, $G_s=0.25$ µS and $C_d=68.4$ aF, $G_d=0.15$ µS and $C_g=1.3$ aF, where the values of the junction capacitances are extracted from the slopes of the experimentally measured diamonds, $\gamma^+=C_g/(C_g+C_s)$, $\gamma^-=C_g/C_d$, and the island-gate capacitance, $C_g$, can be calculated from the period of the diamonds: $C_g=e/\Delta V_g=1.3$ aF where $\Delta V_g$ is the period of Coulomb blockade oscillations.

A good correlation between the theory and experiment is observed. This confirms the formation of well-defined MIM tunnel junctions in the fabricated device and demonstrates the effectiveness of the anneal steps in eliminating the NiO parasitic layers by means of reduction.
Figure 3-12 a) Charging diagram (Coulomb diamonds) of the fabricated device with 12 cycles of PEALD SiO$_2$ as the tunnel barrier and two reducing anneal step to reduce the parasitic NiO formed in the junctions. b) A simulated charging diagram of a metallic SET with $C_s=40.1$ aF, $G_s=0.25$ $\mu$S and $C_d=68.4$ aF, $G_d=0.15$ $\mu$S, and $C_g=1.3$ aF
Figure 3-13 shows the differential conductance between the source and drain ($G_{ds}$) as a function of the applied bias ($V_{ds}$) at 6K, for a device with untreated NiO layer (purple curve) and for the fabricated device explained above (solid black curve) in which the bottom NiO layer, formed on the island the PEALD, is reduced for 25 min at 400°C in 5% H$_2$ -95% Ar before the top source/drain are defined on the barrier. Additionally, the top NiO, formed at the bottom of the source/drain, is reduced in the same conditions for 10 min. For comparison, $G_{ds}(V_{ds})$ of the simulated device with parameters mentioned above is also shown (red line). The room temperature conductance of both treated and untreated devices was 11 nS.

Figure 3-13 The effect of the reducing anneal step in alleviating the activated conductance in cross-bar structures which is shown to be caused by the parasitic NiO formed in the tunnel junctions
As noticed by comparing the charging diagrams, the behavior of the device with reduced NiO layers is similar to the ideal. In contrast, as expected from the presence of NiO in the junctions, the device with untreated NiO exhibits a conductance that is exponentially suppressed at $V_{ds}=0$. Furthermore, as the bias is increased, the conductance gradually increases with $V_{ds}$, and even at $V_{ds}=40$ mV, is less than the room temperature value (11 nS). This confirms that the parasitic NiO is most likely responsible for the activation-based conduction mechanism in the device structure, and shows that the proposed reducing steps in 5%H$_2$-95% Ar at 400°C are effective in reducing the NiO parasitic layers that are formed in the tunnel junctions, and therefore can be used to reduce the effect of thermal activation in the junctions.
3.2.3 Damage induced by thermal anneal: agglomeration of Ni thin films

Although the 400°C anneal step is necessary for reducing the NiO in the junctions, this high temperature treatment has an adverse effect on the thin Ni film that forms the island, source, and drain. We have observed that upon annealing the devices and nanowires, the resistance first decreases due to both NiO reduction and the increased size of the metal grains, which decreases the scattering along the wire. However, prolonged thermal anneal results in an increase in resistance and eventually an open. We attribute this to grain agglomeration and film deformation that is induced by high temperature. Based on our experiments, the grains of the Ni film grow during high temperature anneal and begin to cause agglomeration and deformation in the film, as shown in Figure 3-14.

Figure 3-14 Thermal induced grain agglomeration and film deformation as a result of 30 min anneal at 400°C
It has been reported that agglomeration in thin films starts with grain boundary grooving driven by reduction of the free energy at grain boundaries\(^5\). As the annealing step progresses, the grooves at the grain boundaries get deeper until they result in a discontinuity in the film and therefore an open. Boragno et al. have also reported time evolution of Ni films during high temperature treatment \(^5\). For many metals, a temperature of a few hundred °C, well below their melting point, is claimed sufficient to cause the rupture of the film by providing the activation energy that is needed for the film to turn into clusters (droplets). Figure 3-15 shows this phenomenon in a fabricated nanodamascene SET.

Figure 3-15 Nanodamascene SET structure with agglomerated island due to the thermal anneal
Although agglomeration degrades the performance of the SETs fabricated in different structures (crosstie, inlaid island, nanodamascene), it has the most severe effect on nanodamascene SETs. In fact, since the lateral contact between the leads and the island forms the tunnel junctions, a small deformation in the leads results in an open in the junctions, as shown in Figure 3-16 below:

![Figure 3-16 Nanodamascene SET structure after the reducing anneal steps that result in deformation of Ni layer in the leads and consequently an open](image)

Due to the detrimental side-effects of the anneal steps for NiO reduction (especially the second anneal), the two alternative approaches that we tried are as follows: First, we tried to use a noble metal like Pd as the top electrode. Pd has a satisfactory adhesion to SiO$_2$, and due to its chemical inertness, is not expected to oxidize when evaporated on SiO$_2$. Second, NiO reduction was performed with H$_2$ plasma that is
reported to reduce the NiO at a lower temperature range than that for annealing\textsuperscript{36}. The second approach uses a H\textsubscript{2} plasma in the Oxford FlexAL PEALD system at 200-300°C, which is expected to slow down the process of grain agglomeration and film deformation due to a lower processing temperature.

3.2.3.1 Inlaid crosstie SETs with Ni island and Pd source-drain and stacked layers of SiO\textsubscript{2}:Al\textsubscript{2}O\textsubscript{3} as the tunnel barrier

As discussed before, in order to eliminate the second reducing anneal that resulted in open nanodamascene devices, we tried Pd, a noble metal which is not expected to be oxidized when evaporated on the SiO\textsubscript{2} PEALD, as the top electrode so that no second reducing anneal is necessary. In addition to the SiO\textsubscript{2} tunnel barrier, Al\textsubscript{2}O\textsubscript{3} and SiO\textsubscript{2}-Al\textsubscript{2}O\textsubscript{3} were also studied. Al\textsubscript{2}O\textsubscript{3} was studied since it has a standard enthalpy of formation almost twice as SiO\textsubscript{2} (-1669.8 vs. -859.4 kJ/mol, respectively), and therefore is believed to have a low interaction (intermixing) with the top electrode, and thus might prevent the top surface oxide from forming. Since the dielectric constant of bulk Al\textsubscript{2}O\textsubscript{3} is almost twice as that of SiO\textsubscript{2} (9 vs. 4, respectively), to fabricate junctions with smaller capacitance, we have also tried a stack of SiO\textsubscript{2}-Al\textsubscript{2}O\textsubscript{3} to take advantage of smaller SiO\textsubscript{2} dielectric constant as well as a more stable Al\textsubscript{2}O\textsubscript{3} dielectric, and thus less reaction with the top electrode. For this purpose, SET structures with Ni-insulator-Ni and Ni-insulator-Pd tunnel junctions were made and different tunnel barrier dielectrics, Al\textsubscript{2}O\textsubscript{3}, SiO\textsubscript{2}, and SiO\textsubscript{2}-Al\textsubscript{2}O\textsubscript{3}, were studied in these two structures.

The covered inlaid Ni islands in all of the fabricated devices were treated under the same condition in 5\% H\textsubscript{2}-95\% Ar for 25 minutes at 400 °C. Surprisingly, no significant difference resulting from replacing the top Ni electrode with Pd was observed.
In fact, prior to the second treatment, both type of devices exhibited a resistance greater than 20 GΩ (conductance lower than G< 0.05 nS) for all types of barriers.

Table 3-1 is the summary of the outcome from annealing the fabricated structures.

**TABLE 3-1:**

**THE SUMMARY OF THE OUTCOME FROM ANNEALING THE FABRICATED STRUCTURES WITH 40×40 NM² TUNNEL JUNCTIONS MADE WITH NI OR PD TOP ELECTRODES, NI INLAID ISLAND, Al₂O₃, SiO₂, OR SiO₂-Al₂O₃ TUNNEL BARRIER**

<table>
<thead>
<tr>
<th></th>
<th>As deposited</th>
<th>5 min anneal at 400°C</th>
<th>Resistance after 60 hours</th>
<th>15 min anneal at 400°C after 60 hours</th>
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</thead>
<tbody>
<tr>
<td></td>
<td>Ni</td>
<td>Pd</td>
<td>Ni</td>
<td>Pd</td>
</tr>
<tr>
<td>12 cycles SiO₂</td>
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<td>&gt;20 GΩ</td>
<td>30 MΩ</td>
<td>70 MΩ</td>
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<tr>
<td></td>
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<td>Pd</td>
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</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>13 MΩ</td>
<td>20 MΩ</td>
</tr>
<tr>
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<td>&gt;20 GΩ</td>
<td>30 MΩ</td>
<td>No Data</td>
</tr>
<tr>
<td></td>
<td>Ni</td>
<td>Pd</td>
<td>No Data</td>
<td>No Data</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>No Change</td>
<td>16 MΩ</td>
</tr>
<tr>
<td>6:4 cycles SiO₂: Al₂O₃</td>
<td>&gt;20 GΩ</td>
<td>&gt;20 GΩ</td>
<td>1 MΩ</td>
<td>1 MΩ</td>
</tr>
</tbody>
</table>
Figure 3-17 (a) shows the charging diagram of an SET device with 40×40 nm² tunnel junctions in which the Ni island is treated with 25 minutes in 5% H₂-95% Ar ambient at 400°C after deposition of 6 SiO₂ and 4 Al₂O₃ PEALD cycles as the tunnel barrier, while the Pd source and drain are treated in the same ambient at 375°C for 5 minutes. For comparison, the charging diagram of a simulated device with C_d=110 aF, G_d=70 nS, C_s=80 aF, G_s=50 nS, and C_g=0.8 aF, at 400mK is shown in Figure 3-17 (b).
Figure 3-17 (a) The charging diagram of an SET device with 40×40 nm² tunnel junctions in which the island is Ni, treated with 25 minutes in 5% H₂-95% Ar ambient at 400°C after deposition of 6 SiO₂ and 4 Al₂O₃ PEALD cycles as the tunnel barrier, while the Pd source and drain are treated in the same ambient at 375°C for 5 minutes. (b) The charging diagram of a simulated device with $C_d=110$ aF, $C_s=80$ aF, $C_g=0.8$ aF, $R_s=8$ MΩ, and $R_d=8$ MΩ at 400mK
Although the height of the experimental diamonds (charging energy) reasonably matches the simulated results, there is a discrepancy in the regions where two diamonds meet at $V_{ds}=0$. As discussed before, these regions correspond to the peak of the Coulomb blockade oscillations and for an ideal MIM SET must be $G_o/2$.

$G(V_{ds})$ at the peak of Coulomb blockade oscillations ($V_g=92$ mV) was plotted and compared to simulations; Figure 3-18 shows an experimental $G_{ds}(V_{ds})$ dependence measured at a peak of CBO (black curve), while red curve is the results of $G_{ds}(V_{ds})$ at the peak of CBO for the simulated device with ideal MIM tunnel junctions and junction parameters as explained above.

![Graph](image.png)

Figure 3-18 (Black curve) An experimental $G_{ds}(V_{ds})$ dependence measured at a peak of CBO at $V_g=35$ mV. (Red curve) The simulation results of $G_{ds}(V_{ds})$ for a device with ideal MIM tunnel junctions.
Clearly, at the peak of the Coulomb blockade oscillations, $G(V_{ds}=0)$ is smaller than $G_0/2$. To verify that the additional suppression of $G_{ds}$ ($V_{ds}=0$) is related to the remaining NiO in the junctions, additional anneal treatment in 5% H$_2$-95% Ar ambient at 400°C was performed for 15 minutes in order to reduce the residual parasitic NiO to metallic Ni.

Figure (a) shows the Coulomb diamonds of a Ni-SiO$_2$-Pd device that after the first anneal (in 5% H$_2$-95% Ar ambient at 375°C for 5 min) had a resistance of 32MΩ, which increased to 260 MΩ over the course of 60 hours after the treatment. The resistance of the device decreased to 10 MΩ after the second anneal (in 5% H$_2$-95% Ar ambient at 400°C for 15 min), but later again increased to 40 MΩ in 24 hours. We believe that the initial resistance drop after the anneal is due to reduction of the surface metal oxide at the metal-dielectric interface. However, the reduced metal is re-oxidized slightly due to reacting with oxygen either from the ambient or from the residual contaminants on the barrier surface. For comparison, the charging diagram of a simulated device with $C_d=148$ aF, $G_s=23$ nS, $C_s=48$ aF, $G_d=47$ nS, and $C_g=0.012$ aF, at 400 mK is shown in Figure 3-19 (b).
Figure 3-19 a) Charging diagram (Coulomb diamonds) of the fabricated device with 12 SiO$_2$ PEALD cycles as the tunnel barrier and two reducing anneal steps on the top Pd source and drain electrodes (at 375°C for 5 min and at 400°C for 15 min. b) Simulated SET device with ideal MIM tunnel junctions with $C_d=148$ aF, $G_s=23$ nS, $C_s=48$ aF, $G_d=47$ nS, and $C_g=0.012$ aF at 400 mK. The small $C_g$ is due to the use of a gate that was located >100µm away from the SET structure.
In comparison to the devices annealed for 5 minutes, it seems that the extra anneal step results in increased asymmetry in junction parameters which can be inferred from the skewed diamonds in the charging diagram. Dissimilar junction parameters can result from the interaction between the metal and dielectric, non-uniformities in the deposited tunnel barrier, and diffusion of metal in the dielectric that takes place at elevated temperatures. This phenomenon can randomly change the dielectric properties and result in dissimilar barriers in the junctions. Indeed, high-temperature driven inter-diffusion of metals in SiO$_2$ as well as Pd$_3$Si formation from Pd and SiO$_2$ at H$_2$ ambient has been reported.$^53$ Since the tunnel junctions in SETs are fabricated with $\approx$1 nm of tunnel barrier and critically depend on the quality of the barrier as well as metal-barrier interface, slight change in the tunnel junction can drastically change the performance of the fabricated devices.
It is clear that although the experimental charging diagram matches the simulations quite reasonably, the fabricated device measurements suffer from a significant RTS noise level, which considerably compromises the S/N ratio. In Figure 3-20 that shows the Coulomb blockade oscillations of the device, the noise effect is highly noticeable.

Figure 3-20 Coulomb blockade oscillations of the fabricated device with 12 SiO$_2$ PEALD cycles as the tunnel barrier and two reducing anneal steps on the top Pd source and drain electrodes. There is a clear effect of noise that compromises S/N.

We believe that as discussed before, the electron entrapment and release by the traps in close proximity of the island, most likely in the dielectric tunnel barrier or in the dielectric-metal interface of the junctions$^{54}$, is responsible for the observed RTS noise.
since it can change the potential of the island and result in abrupt change in SET conductance on the order of the CBO magnitude.

Figure 3-21 shows the $G_{ds}(V_{ds})$ plotted for the device at a peak of CBO at $V_g=-7\text{V}$ (black curve). At this bias point, any suppression of the conductance at $V_{ds}=0$ below half of the room temperature value is not part of the Coulomb blockade and results from a residual parasitic component in the junctions. For comparison, $G_{ds}(V_{ds})$ is also plotted at the peak of CBO (red curve) for the simulated device, with ideal MIM tunnel junctions and junction parameters as explained above. In addition to an extra $G$ suppression at $V_{ds}=0$, the effect of RTS noise is clearly visible.

Figure 3-21 (Black curve) An experimental $G_{ds}(V_{ds})$ dependence measured at a peak of CBO at $V_g=-7\text{V}$. (Red curve) The simulation results of $G_{ds}(V_{ds})$ for a device with ideal MIM tunnel junctions
In addition to the stacked barriers composed of 6 cycles of SiO$_2$ and 4 cycles of Al$_2$O$_3$, tunnel barriers from 10 cycles of SiO$_2$ and 2 cycles of Al$_2$O$_3$ (Figure 3-22) were also fabricated to increase the charging energy by lowering the overall dielectric constant.

![Figure 3-22 The stacked Al$_2$O$_3$-SiO$_2$ tunnel barrier formed by PEALD in the SET tunnel junctions](image)

Based on our experiments, compared to 12 cycles of SiO$_2$ PEALD tunnel barrier, the average resistance of the devices with stacked layers of SiO$_2$/Al$_2$O$_3$ with the same total number of PEALD cycles was lower. That is, after the covered island was annealed for 25 min at 400°C in 5% H$_2$-95% Ar and the NiO on the bottom of source/drain leads was annealed for 10 min at 370°C in 5% H$_2$-95% Ar, the average resistance of SETs with 10 SiO$_2$+2 Al$_2$O$_3$ tunnel barrier was 1.3 MΩ, while the SET devices with 12 cycles of SiO$_2$ tunnel barrier exhibited 5.3 MΩ of resistance through the device. This can be attributed to a thinner barrier in stacked SiO$_2$+Al$_2$O$_3$ as a result of the non-uniformities in the two monolayers of the deposited Al$_2$O$_3$ Figure 3-23 (a) shows the charging diagram of an SET device with 10+2 SiO$_2$+Al$_2$O$_3$ tunnel barrier. For comparison, the charging diagram of a simulated device with $C_d$=65 aF, $G_d$=263 nS, $C_s$=50 aF, $G_s$=18 nS, $C_g$=16 aF, at 0.4 K is shown in Figure 3-23 (b).
Figure 3-23 a) Charging diagram (Coulomb diamonds) of the fabricated device with 10 SiO$_2$ cycles +2 Al$_2$O$_3$ cycles of PEALD as the tunnel barrier and two reducing anneal step to reduce the parasitic NiO formed in the junctions. b) Simulated SET device with ideal MIM tunnel junctions with $C_d=65$ aF, $G_d=263$ nS, $C_s=50$ aF, $G_s=18$ nS, $C_g=16$ aF at 400 mK
The experimental charging diagram suffers from significant RTS noise as also observed for all previously discussed devices.

The experimental $G_{ds}(V_{ds})$ dependence measured at a peak of CBO at $V_g=9$ mV, Figure 3-24 (a), was plotted to validate the $\approx 15\times$ conductance difference in the simulated model (Figure 3-24 (b)). A reasonably good match between the simulation and experimental results confirm the asymmetry in the junction resistance. We believe that a significant ($\approx 15$ times) difference in conductance values in spite of the relatively small ($\approx 1.5$ times) difference in junction capacitance results from random fluctuations in the dielectric thickness, which may be caused by the non-uniformity in the 2 cycles of $\text{Al}_2\text{O}_3$ or from the inter-diffusion of the metal electrodes and the dielectric barrier which can exponentially change the conductance due to “thin spots” in the dielectric without significant change in the average thickness of the barrier.
Figure 3-24 (a) Differential conductance vs. DC bias applied across source and drain ($V_{ds}$) at the peak of CBO ($V_g=9.7$ mV) of the fabricated device with 10 SiO$_2$ cycles +2 Al$_2$O$_3$ cycles of PEALD as the tunnel barrier and two reducing anneal step to reduce the parasitic NiO formed in the junctions. (b) Differential conductance at the peak of CBO of the simulated device with ideal MIM tunnel junctions with $C_d=65$ aF, $C_s=50$ aF, $C_g=16$ aF, $R_s=54$ M$\Omega$, and $R_d=3.6$ M$\Omega$ at 400mK.
3.2.4 Reduction of the parasitic NiO with H$_2$ plasma

3.2.4.1 SET cross-tie structures with RTA reduction for the island and H$_2$ plasma reduction for source and drain

As explained above, to alleviate the thermally induced damage on the Ni films during NiO high-temperature reduction, we studied the reduction of the parasitic NiO layers with H$_2$ plasma. The lower processing temperature as well as a possible shorter processing time makes this approach more desirable than the reducing anneal step.

The first batch of SET devices that were studied for NiO reduction with H$_2$ plasma was prepared as follows. First, 12 SiO$_2$ PEALD cycles and 10:2 SiO$_2$:Al$_2$O$_3$ PEALD cycles formed the tunnel barriers on the islands of two separate batches of devices, and 400°C of anneal in forming gas reduced the underlying NiO in 30 min. Next, the source-drain leads were formed on the barriers and each batch was divided into separate dies that were studied for different treatments of the top NiO. The result of the device with 10:2 SiO$_2$:Al$_2$O$_3$ PEALD cycles as the tunnel barrier in which the top NiO is reduced with a high-T anneal has already been discussed above (Figure 3-23 and 3-24) in which significant RTS noise is observed. However, the devices in which the top NiO is reduced in H$_2$ plasma at 300°C for 5 minutes, in FlexAl PEALD system with 50 sccm H$_2$ at 10 mTorr and plasma power of 100W, exhibited a drastic decrease in the observed RTS noise, as clear from the observed CBO of a fabricated device (Figure 3-25). The reason to this is still under further study, however, we believe that this likely results from a lower H$_2$ plasma processing temperature and a shorter processing time, which minimizes any undesirable metal-dielectric interaction and metal inter-diffusion in the barrier.
Figure 3-25 CBOs of an SET device in which the NiO formed on the island is reduced with rapid thermal annealing and the NiO formed on the bottom of the source and drain is reduced in a H₂ plasma treatment for 5 min.

Based on our experiments, after the fabricated devices with annealed island are subjected to 5 minutes of H₂ plasma, they exhibit an increase of conductance by more than 50× (from ~2 nS to ~125 nS). Figure 3-26 (a) shows the charging diagram of the devices with NiO films reduced with a combination of rapid thermal anneal (RTA) (for the NiO formed on the island) and H₂ plasma (for the NiO formed on the bottom of source and drain). For comparison, the charging diagram of a simulated device with $C_d=62$ aF, $C_s=41$ aF, $C_g=1.21$ aF, and $G_s=G_d=240$ nS at 400 mK is shown in Figure 3-26 (b).
Figure 3-26 The charging diagram of an SET device in which the NiO formed on the island is reduced with rapid thermal annealing and the NiO formed on the bottom of the source and drain is reduced in a H$_2$ plasma treatment for 5 min. The change in the period of the diamonds is due to the charge drift in the substrate due to the sweeps of the gate voltage. (b) charging diagram of a simulated device with $C_d=62$ aF, $C_s=41$ aF, $C_g=1.21$ aF, and $G_s=G_d=240$ nS at 400 mK.
It should be mentioned that no difference in terms of decreased RTS noise is observed for devices with 12 cycles of SiO$_2$ or the ones with 10:2 cycles SiO$_2$:Al$_2$O$_3$ as the barrier.

Clearly, a comparison between experimental results and the simulations indicates a good match. Most importantly, unlike the majority of other devices discussed above, the detailed comparison of the features on the Coulomb diamonds plots reveals a very good quantitative match. For instance, the conductance in the central diamonds is blocked due to the island charging energy, while between the central diamonds at $V_{ds}$=0, where the blockade is lifted, the conductance through the device approaches half of that at room temperature ($G_0/2$). This confirms minimal presence of the activated component in the junctions. Figure 3-27 shows the $G_{ds}(V_{ds})$ at the peak of the Coulomb blockade oscillations ($V_g$=100 mV).
Figure 3-27 Differential conductance vs. DC bias applied across source and drain ($V_{ds}$) at the peak of CBO ($V_{g}$=110 mV) of the fabricated device in which the NiO formed on the island is reduced with rapid thermal annealing and the NiO formed on the bottom of the source and drain is reduced in a H$_2$ plasma treatment for 5 min.

A good match between the experimental result and simulations results from the minimal NiO residue after a high-T anneal+H$_2$ plasma treatment on the device that was intended to reduce the parasitic NiO in the junctions with minimum damage to the dielectric as well as possible passivation of the traps in the barrier due to the H$_2$ plasma.

3.2.4.2 SET crosstie devices with H$_2$ plasma reduction of the bottom NiO and untreated source/drain

After successful H$_2$ plasma reduction of NiO that is formed on the bottom of source and drain (the bottom of the top electrodes in the tunnel junction), a new batch of devices was fabricated to study the H$_2$ plasma reduction of NiO that is formed on the island (the bottom electrode of the tunnel junctions). For that purpose, crosstie SETs with
an inlaid island were fabricated using the process flow described in chapter 2. However, following the formation of the 12-cycle PEALD SiO$_2$ tunnel barrier, the covered islands were subjected to 5 minutes of H$_2$ plasma at 300°C with 50 sccm H$_2$ at 10 mTorr and plasma power of 100W.

Our experiments show that the devices with H$_2$-plasma treated island and untreated source and drain exhibit a conductance that is around three orders of magnitude greater than those with just annealed islands. That is, with no source and drain treatment, the islands that were exposed to H$_2$ plasma led to structures with G=1.7µS through source-drain, while islands subjected to 400°C-anneal reduction resulted in G=2 nS through the device. The characteristics of a fabricated device with a H$_2$-plasma treated island and untreated source-drain with G$_o$=400 nS is reported here. The Coulomb blockade oscillations of the device at 0.4 K are shown in Figure 3-28.
Figure 3-28 Coulomb blockade oscillations of the fabricated crosstie device with inlaid island that is subjected to H$_2$ plasma for reduction of the NiO formed during the PEALD of SiO$_2$. The source and drain are not treated.

As shown above, the peak of the oscillations is less than 20 nS, which is an order of magnitude smaller than the expected peak of the CBO based on the simulations ($G_{\text{peak}}=G_0/2\approx200$ nS). Also, note the significant noise observed in the CBO plot.

The charging diagram of the device at 0.4 K is shown in Figure (a). For comparison, the charging diagram of a simulated device with $C_d=46.3$ aF, $C_s=99$ aF, $C_g=0.51$ aF, and $G_s=G_d=800$ nS at 0.4 K is shown in Figure 3-29 (b). The parameters for the simulated device were chosen based on the positive and negative slopes as well as the period of the charging diagram for the fabricated device.
Figure 3-29 (a) Charging diagram of a device with island exposed to H\textsubscript{2} plasma following the PEALD of SiO\textsubscript{2} barrier. (b) Charging diagram of a simulated device with $C_d=46.3$ aF, $C_s=99$ aF, $C_g=0.51$ aF, and $G_s=G_d=800$ nS at 0.4 K
The skewed diamonds in Figure 3-29 is a result of asymmetric capacitance in source and drain junctions. As discussed before, the variations in junction capacitances are likely to be caused by random fluctuations in the tunnel barrier composition and thickness. This can result from intermixing in the metal and dielectric that can change different properties (e.g. dielectric constant, thickness, uniformity) of the barrier. Although the blockade diamonds in the measured device resemble the simulated data reasonably, there is considerable discrepancy between the experimental data and simulations in conductance outside the blockaded region; for instance, for simulations, the conductance for |Vds|>2E_c/e is 400 nS, which is equal to G_o. In contrast, the value of conductance outside the blockade region is between 100-200 nS for the fabricated device, which approaches the room temperature value at Vds > 7 mV.

Moreover, at V_{ds}=0, the area between the Coulomb diamonds represent the V_g range where the Coulomb blockade is lifted and the conductance is at the peak of Coulomb blockade oscillations and should be equal to G_o/2. Indeed, for the simulated MIM device, the conductance between the Coulomb blockade diamonds at V_{ds}=0 (G=G_o/2≈ 200 nS), while in the experiment it does not exceed 12 nS. For a closer look at the discrepancy between the ideal and fabricated device at the peak of Coulomb blockade oscillations, Figure 3-30 is plotted, which shows an experimental G_{ds}(V_{ds}) dependence measured at a peak of CBO at V_g=72 mV (red curve), along with the G_{ds}(V_{ds}) for the simulated device (black curve).
Figure 3-30 (Red curve) $G_{ds}$ as a function of drain-source bias ($V_{ds}$) at the peak of the oscillations ($V_{gs} = 72$ mV) for a device in which only the island was subjected to H$_2$ plasma (source and drain remained untreated). (Black curve) $G_{ds}(V_{ds})$ for a simulated device with $C_d=46.3$ aF, $C_s=99$ aF, $C_g=0.51$ aF, and $R_s=R_d=1$ MΩ at 400mK. 

Clearly, in the simulations, the conductance changes from 400 nS at $V_{ds}=-300$ mV ($|V_{ds}| >> 2E_c/e$) to 200 nS at $V_{ds}=0$, whereas in experiment, the conductance decreases well below 200 nS at $V_{ds}=0$. Additionally, outside the Coulomb blockade region, the conductance is not a constant value and gradually approaches 400 nS as the drain-source bias is increased. This behavior has been observed previously for the samples with residual untreated NiO films in the tunnel junctions. As a result, we believe that there is still residual NiO, most likely on the bottom of the source and drain leads, left unreduced and this results in a significant activated transport. However, the higher conductance of devices in which the island is treated with H$_2$ plasma compared to the ones in which
island was annealed is believed to be caused by the plasma-induced damage on the barrier or possible chemical reduction of the SiO$_2$ barrier upon exposure to H$_2$ plasma. Additionally, the thermal deformation and grain boundary grooving in the annealed islands can further increase the resistance of the devices compared to the H$_2$ plasma treated samples.

3.2.4.3 SET crosstie devices with two H$_2$ plasma steps for reducing the top and bottom NiO

Due to the evident presence of the parasitic component in devices with H$_2$ plasma treated islands and untreated source/drain, in the next batch of devices, the source and drain electrodes were also treated with H$_2$ plasma for reduction of the parasitic NiO that is believed to be formed on the bottom of these electrodes. Based on our experiments, the average conductance change after the second H$_2$ plasma treatment was approximately 3× (from ~ 0.8 µS to ~ 2.5 µΩ), where more than 50× conductance change was observed after source-drain H$_2$ plasma treatment for the devices in which the island was annealed. This discrepancy is believed to result from the different effect of these two treatments on the barrier and Ni films.

For the measured device reported here, a conductance of 0.3 µS was measured through the device before the final H$_2$ treatment which increased to ≈3 µS after the fabricated structure, with deposited source/drain, was exposed to H$_2$ plasma under the same plasma condition (10 mTorr, 100W) at 300°C for 5 minutes. Figure 3-31 (a) shows the charging diagram of the device. For comparison, an SET with ideal MIM structures was simulated (Figure 3-31(b)) with the following parameters: $C_d=84$ aF, $C_s=60$ aF, $C_g=3.3$ aF, and $G_s=G_d=3.6$ µS.
Figure 3-31 (a) Charging diagram of a device with island exposed to H₂ plasma following the 12 cycles PEALD of SiO₂ barrier, and source-drain leads that are exposed to H₂ plasma for 5 minutes after being deposited on the island. (b) Charging diagram of a simulated device with $C_d = 84$ aF, $C_s = 60$ aF, $C_g = 3.3$ aF, and $G_s = G_d = 3.6$ µS at 400 mK.
The Coulomb blockade diamonds in the center reasonably match the simulations, although there is clear discrepancy for the regions outside the central diamonds. As shown for the simulated result, the conductance between the blockaded diamonds at \( V_{ds} = 0 \) is \( G_0/2 \), but for the fabricated device, the conductance between the central diamonds is approximately \( G_0/4 \). Moreover, as opposed to the simulated SET in which the conductance approaches a constant value above the Coulomb diamonds for \( |V_{ds}| > 5 \) mV, the conductance gradually increases in the fabricated device at \( |V_{ds}| > 5 \) mV. It must also be mentioned that the conductance of the device at room temperature was 3 \( \mu \)S, which decreased to 2 \( \mu \)S as the temperature was lowered to 0.4 K.

Figure 3-32 shows the experimental \( G_{ds}(V_{ds}) \) dependence measured at a peak of CBO at \( V_g = 72 \) mV (red curve), along with the \( G_{ds}(V_{ds}) \) for the simulated device (black curve).

![Figure 3-32](image_url)

**Figure 3-32** Red line: \( G_{ds} \) as a function of drain-source bias \( (V_{ds}) \) at the peak of the oscillations \( (V_{gs} = 7 \) mV) for a device in which both island and the leads are subjected to H\(_2\) plasma for reducing the parasitic NiO. Black line: \( G_{ds}(V_{ds}) \) for a simulated device (with \( C_d = 84 \) aF, \( C_s = 60 \) aF, \( C_g = 3.3 \) aF, and \( G_s = G_d = 3.6 \) \( \mu \)S at 400mK) at the peak of coulomb blockade oscillations.
As discussed before, the clear discrepancy between the experimental and simulated data is the constant conductance in simulations for $|V_{ds}| > 5$ mV compared to the increasing conductance in that region for the fabricated device. Moreover, the conductance at $V_{ds} = 0$ in the fabricated device is suppressed by more than $3\times$ compared to $G_0$, in contrast to $2\times$ lower conductance at $V_{ds} = 0$ in the simulated SET.

Curiously, the noise observed in the devices treated with one or two H$_2$ plasma steps was again very strong, similar to those treated with two high-T anneal steps (Figures 3-17, 3-19, and 3-23).

3.2.4.4 SET crosstie devices with a thicker dielectric barrier, treated with two H$_2$ plasma steps

The last batch of crosstie SET structures discussed here were made with 16 cycles of PEALD SiO$_2$ in the tunnel junctions; after deposition of the SiO$_2$ PEALD, the island was exposed to 5 minutes of H$_2$ plasma for reduction of the NiO formed on the island.

To reduce the residual water adsorbed on the oxide barrier that is believed to result in oxidation of the bottom of source and drain, after H$_2$ plasma treatment of the barrier, the sample was heated at 110°C for one hour at < $8 \times 10^{-7}$ Torr to desorb the water on the oxide desorbs before the source and drain formation on the barrier. Next, without breaking the vacuum, the source and drain metal electrodes were formed by Ni evaporation. Based on our observations, the average conductance through these devices with untreated source and drain leads was ≈0.8 μS. However, based on the Simmons equation, the tunneling conductance for a junction that has 16 cycles of PEALD SiO$_2$ tunnel barrier should be 50× lower than that with 12 cycles of PEALD SiO$_2$ dielectric.
barrier. Indeed, we have not observed a significant decrease in the conductance of the junctions with 16 PEALD SiO$_2$ cycles relative to 12 cycles of the SiO$_2$ PEALD. We attribute this to the damage that is caused by the H$_2$ plasma step on the tunnel barrier, which may result in defects and traps formed in the oxide as well as thinner barrier than one expected based on the nominal PEALD growth.

Figure 3-33 shows the conductance through the device as a function of source-drain bias (V$_{ds}$) at 48 K and 6K. For comparison, an SET was simulated (C$_d$= 64 aF, C$_s$=46 aF) where the capacitance of the junctions were 1.3× smaller than the H$_2$ plasma-treated SET with 12 SiO$_2$ PEALD cycles (C$_d$= 84 aF, C$_s$=60 aF) since the dimensions of the fabricated devices are similar and the dielectric for this batch was nominally 1.3× thicker.
Figure 3-33 $G_{ds}$ as a function of drain-source bias ($V_{ds}$) for a device in which 16 cycles of PEALD SiO$_2$ formed the tunnel barrier on the island and island was treated with 5 min H$_2$ plasma. The sample was heated at 110°C for one hour at $< 8 \times 10^{-7}$ Torr before deposition of source and drain leads. Red line is the measured $G_{ds}(V_{ds})$ for the device at 48K, while green line is the measured $G_{ds}(V_{ds})$ for the device at 6K. Black line: $G_{ds}(V_{ds})$ for a simulated device (with $C_d = 64$ aF, $C_s = 46$ aF, $C_g = 3.3$ aF, and $G_s = G_d = 3.6$ $\mu$S at 48K. Blue line: $G_{ds}(V_{ds})$ for the simulated device 6K.

As described before, the significant deviation from ideal SET at both temperatures results from the parasitic component that is present in the tunnel junctions.

A 7-min H$_2$ plasma treatment (10 mTorr, 100W) was performed on the devices with untreated source and drain leads to reduce the NiO that is formed in the tunnel junctions on the bottom of the source/drain leads. The conductance of the measured device was 0.3 $\mu$S before the final treatment, and increased to 2.5 $\mu$S after the second H$_2$ plasma treatment for 7 minutes. Figure 3-34 (a) shows the charging diagram of a device with 16 cycles of SiO$_2$ PEALD of tunnel barrier in which the island is treated with H$_2$. 

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plasma for 5 min and the source and drain were treated for 7 min with H₂ plasma. For comparison, the charging diagram of a simulated device with $C_d=46$ aF, $C_s=84$ aF, $C_p=5$ aF, and $G_d=0.14$ μS, $G_s=0.27$ μS at 400 mK is shown Figure 3-34 (b). Based on the simulations, there is a clear discrepancy between an ideal SET with MIM tunnel junctions and the experimental results, especially outside the Coulomb diamonds.
Figure 3-34 (a) Charging diagram of a device with island exposed to H\textsubscript{2} plasma following the 16 cycles of PEALD SiO\textsubscript{2} barrier. The sample was heated at 110°C for one hour at < 8\times10\textsuperscript{-7} Torr before deposition of source and drain leads. Following the source and drain formation, the structure is exposed to H\textsubscript{2} plasma for 7 minutes. (b) Charging diagram of a simulated device with \(C_\text{d}=46\ \text{aF}, C_\text{s}=84\ \text{aF}, C_\text{g}=5\ \text{aF},\) and \(G_\text{d}=0.14\ \mu\text{S}, G_\text{s}=0.27\ \mu\text{S}\) at 400 mK.
Figure 3-35 shows an experimental $G_{ds}(V_{ds})$ dependence measured at a peak of CBO at $V_g=-64$ mV (blue curve), along with the $G_{ds}(V_{ds})$ for the simulated device (black curve) at a peak of CBO at $V_g=7.5$ mV.

Figure 3-35 Blue line: $G_{ds}$ as a function of drain-source bias ($V_{ds}$) at the peak of Coulomb blockade oscillations ($V_g=-64$mV) for a device in which 16 cycles of PEALD SiO$_2$ formed the tunnel barrier on the island and island was treated with 5 min H$_2$ plasma. The sample was heated at 110°C for one hour at $<8\times10^{-7}$ Torr before deposition of source and drain leads. Following the source and drain formation, the structure is exposed to H$_2$ plasma for 7 minutes. Black line: Gds(Vds) at the peak of Coulomb blockade oscillations ($V_g=7.5$mV) for a simulated device (with $C_d=84$ aF, $C_s=46$ aF, $C_g=5$ aF, and $G_s=G_d=5.2 \ \mu\text{S}$) at 400 mK

The conductance of experimental data and simulations are normalized by the conductance of the device at room temperature ($G_o=2.6 \ \mu\text{S}$). Based on the simulations, although 7 minutes of H$_2$ plasma on the source and drain further reduces the amount of nonlinearity outside the Coulomb blockade region, compared to 5 minutes, devices using these reduction steps still exhibit deviation from an SET device with ideal MIM tunnel
junctions (i.e. additional suppression below $G_o/2$ at the peak of CBO as well as asymmetry in the $G(V_{ds})$ and nonlinear behavior outside the CB).

3.2.5 $H_2$ plasma induced damage

During our experiments, we have observed bubbles and surface bulging of the bonding pads after being treated with $H_2$ plasma for $\geq 10$ min. These bubbles, that can be as large as the bonding pads, compromise the adhesion of pads to the substrate and make the wire bonding impossible. Figure 3-36 shows an SEM micrograph of a pad with bubbles due to exposure to $H_2$ plasma.

![SEM micrograph of a pad with bubbles due to exposure to $H_2$ plasma.](image)

Figure 3-36 Surface bulging in the bond pads as a result of $H_2$ plasma exposure for 10 minutes
Kuznetsov reported the accumulation of atomic hydrogen at the metal-dielectric interface, which leads to plastic deformation of the metal films due to continuous hydrogen adsorption\textsuperscript{55}.

It is worth mentioning that to prevent the damage that is induced by the H\textsubscript{2} plasma, we studied the effect of H\textsubscript{2} treatment with no plasma power at 300°C in the Oxford FlexAl PEALD chamber. To do so, the crosstie SET structures with an inlaid island and 16 cycles of PEALD SiO\textsubscript{2} were fabricated. Before the source and drain formation, the island was treated with H\textsubscript{2} plasma (10 mTorr, 100W) at 300°C for 5 minutes. After the source/drain were formed on the barrier-covered island, the conductance through the devices was measured and exhibited an average of 170 nS. Next, the structures were treated in FlexAl PEALD chamber with 5 minutes of annealing at 300°C in 50 sccm H\textsubscript{2} ambient at 10 mTorr (the same parameters as for the H\textsubscript{2} plasma treatment but no applied plasma power). Following the treatment, the average conductance of the structures decreased to 85 nS, which is attributed to the dominating effect of thermally-induced electrode deformation and negligible reducing effect of H\textsubscript{2} molecules at 300°C. However, the same batch of devices was exposed to 150 W H\textsubscript{2} plasma for 1 min with the same H\textsubscript{2} flow rate, pressure, and temperature explained above. Based on our observations, the conductance of the devices after the H\textsubscript{2} plasma exposure increased to 400 nS. That is, more than 4× increase in conductance results from NiO reduction during a 1 minute H\textsubscript{2} plasma exposure, whereas H\textsubscript{2} with no applied plasma power does not lead to significant change in the conductance and therefore is believed not be effective in reducing the NiO formed in the junctions at 300 °C. In summary, although H\textsubscript{2} plasma may result in damage to the bonding-pads and make the probing impossible, it
is necessary for reducing the parasitic NiO in the structures at 300°C, and therefore improving the adhesion of the bonding-pads to the substrate is crucial. We have observed that increasing the O₂ plasma descum duration before metal deposition improves the adhesion of the pads to the substrate. However, we have not been able to increase the H₂ plasma exposure time to more than 10 min due to the resulting damage on the bond-pads.
CHAPTER 4:

SUMMARY

We have shown a reliable and reproducible method of fabricating half and full nanodamascene MIM single electron transistors featuring plasma enhanced atomic layer deposition of ultra-thin ($\approx 1$nm) tunnel transparent barriers in the device tunnel junctions.

The use of PMGI as the ebeam resist and Xylenes as the PMGI developer enables repeatable fabrication of $<30$ nm features that can be directly transferred into the oxide due to higher etch resistance of PMGI compared to PMMA. Moreover, by tuning the EBL, etch profile, and the CMP step, repeatable fabrication of $<15$ nm inlaid features in the substrate is possible.

Tunnel barriers of SiO$_2$, Al$_2$O$_3$ and a combination of Al$_2$O$_3$ and SiO$_2$ are used in the fabricated single electron transistors. The formation of the tunnel barriers with PEALD, as opposed to the commonly used Dolan bridge technique that allows in-situ fabrication of the MIM tunnel junctions, results in some challenges that are summarized here. Due to the O$_2$ plasma steps in the cyclic PEALD, the surface of the underlying metal substrate is oxidized during the formation of the tunnel barrier. The thickness of the parasitically formed NiO depends on the number of the PEALD cycles, however, based on our experiments, the parasitic NiO formed on the substrate at the Ni-dielectric interface is approximately 2 nm after deposition of $\approx 1$ nm PEALD SiO$_2$. Moreover, the
Ni layer deposited on top of the dielectric to form the top electrode is also oxidized at the top Ni-dielectric interface. We believe that the adsorbed water vapor and other possible oxygen-containing contaminants on the dielectric, most probably adsorbed on the dielectric when it is exposed to the ambient, result in the oxidation of a thin layer of the Ni deposited atop the dielectric. The parasitically formed NiO layers in the junctions significantly change the behavior of the fabricated SET structures; thin NiO layers on Ni have been reported to exhibit electrical properties consistent with presence of a small (<0.2eV) potential barrier. As a result, the conductance through a few nanometers of NiO is lower than that of Ni by several orders of magnitude at room temperature, and as the device is cooled down, the freeze-out of carriers leads to unmeasurably low conductance. Consequently, the presence of NiO in the tunnel junctions leads to significant performance degradation in the fabricated SETs, and elimination of the formed NiO is therefore necessary to restore the characteristics of MIM SETs.

NiO has been reported to be reduced to Ni (NiO+H₂→Ni+H₂O) by annealing at high temperatures in H₂ ambient as well as by being exposed to H₂ plasma at relatively lower temperatures than one needed for the anneal. Here, we have presented two techniques to reduce the NiO in the junctions: anneal in forming gas ambient (5% H₂-95% Ar) at 400°C in a rapid thermal anneal system and H₂ plasma treatment at 300°C in the same chamber used to deposit the tunnel barrier (Oxford FlexAl PEALD). Since the reduction process of NiO includes diffusion of hydrogen towards the NiO and out-diffusion of H₂O that forms as the by-product, we believe that in crosstie structures where source/drain are formed on top of the tunnel barrier covered island, each parasitic NiO (lower NiO formed on the island and upper NiO formed at the bottom of source/drain)
should be reduced separately. That is, the reduction of NiO layer on the top surface of the island, after the island is covered with the tunnel barrier, is performed before the source/drain fabrication since the presence of the source/drain leads slows down the reduction process by adding extra layer through which the hydrogen and byproducts should diffuse. After the source/drain are deposited on the reduced island, the NiO formed in the upper leads is reduced by subjecting the fabricated SET structure to the reducing ambient.

Several batches of devices have been fabricated using the three following techniques to eliminate the parasitic NiO: 1-Reduction of both NiO layers with anneal in forming gas ambient at T> 370°C (25 min at 400°C for the bottom NiO and 10 min at 370-400°C for the top NiO). This step is referred to as “high-T anneal + high-T anneal”. 2- Reduction of the bottom NiO layer with anneal in forming gas ambient at T=400°C for 25 min, and reduction of the top NiO in H₂ plasma (10 mTorr, 100W at 300°C) for 5 minutes. This step is referred to as “high-T anneal+H₂ plasma”. 3- Reduction of both NiO layers for 5 min in H₂ plasma (10 mTorr, 100W at 300°C). This step has been referred to as “H₂ plasma +H₂ plasma”.

 Typically, between 4 to 8 devices were randomly selected from a processed batch and simultaneously measured at low temperatures. Therefore, the reported devices here are representative of several measurements.

To compare the experimental SET device treated with each technique with the ideal MIM SET, the charging diagram of the measured device was plotted and compared against the simulated Coulomb diamonds. The capacitance values used for the
simulations were extracted from the slopes and period of the Coulomb diamonds, while the resistance of the tunnel junctions was chosen based on the total conduction through the device, and in the case of dissimilar junctions, the ratios between the values were chosen to best match the charging diagram and $G_{ds}(V_{ds})$. For a more detailed investigation, $G_{ds}(V_{ds})$ was also plotted for each fabricated device at the peak of the Coulomb blockade oscillations and compared with expected behavior based on simulations (see Figures 3-3, 3-7, 3-13, 3-18, 3-21, 3-27, 3-30, 3-32, and 3-35).

According to orthodox model of Coulomb blockade, when an MIM SET is cooled to $T \approx E_C/k_B$, the conductance at $V_{ds}=0$ decreases towards $G_0/2$ due to a reduction in the island occupation probability imposed by Coulomb blockade. However, when $|V_{ds}| > 2E_C/e$, the Coulomb blockade is suppressed and SETs exhibit an almost constant differential conductance that approaches the high temperature value. In contrast, based on our observations, in samples with residual NiO, the conductance at the peak of CBOs is strongly suppressed at $V_{dc}=0$, and gradually increases with applied bias. As a result, comparing the experimental conductance through the device, as a function of the applied bias, with simulations enables us to study the properties of the tunnel junctions.

In addition to the described comparison, to quantitatively evaluate the contribution of in series resistive component that is likely caused by non-reduced NiO in the junctions, we present the following procedure. First, the zero-bias conductance expected in the minima of CBOs ($G_{\text{min}}(V_{ds}=0)$) for the MIM SETs at several temperatures is calculated, using the $G_0$ value extracted from room temperature measurements and capacitances extracted from the low temperature measurements of the charging diagram. Next, the experimentally obtained conductance values at $G(V_{ds}=0)$ for the same points in
temperature used in our simulations is plotted. Note that at low temperatures, $T \ll E_c/k$, the conductance in the minima of CBOs $G_{\text{min}}(V_{ds}=0, T)$ follows simple activation law $G=\exp(-E_c/kT)$, so the slope of $\ln(G(1/T)$ dependence can be used to extract the value of charging energy. However, in the temperature range presented in Figure 4-1, the theoretical curve exhibits weaker temperature dependence since the studied temperature range is $T \approx E_c/k_B$, and therefore Coulomb blockade is suppressed by thermal fluctuations and CBOs are not observed.

Figure 4-1 The experimental $\ln(G)$ as a function of $(1/T)$ for devices treated with “high-T anneal+ high-T anneal”, “H$_2$-plasma+H$_2$ plasma”, and “high-T anneal+H$_2$ plasma” plotted vs. the expected $\ln(G)$ as a function of $(1/T)$ at the valley of the CBOs. The junction parameters for the simulation were extracted from room-temperature and low-temperature measurements of the fabricated devices.
It is evident in Figure 4-1 that experimentally observed data strongly deviates from theoretical predictions for MIM SETs indicating in series component that lowers the total conductance. The smallest deviation from the model was observed for high-T anneal+H₂ plasma device, where over the entire temperature range this deviation never exceeds 40%, while the strongest deviation is observed for H₂ plasma+H₂ plasma sample where the measured conductance deviates from the theory by almost an order of magnitude. Also, two distinct ranges of temperature can be seen in Figure 4-1 for “high-T anneal+ high-T anneal” and “H₂ plasma+H₂ plasma” samples: a steep slope at higher temperatures, where ln(G) is roughly proportional to 1/T, and low temperature range, characterized by a much weaker slope. The steepness of the slope gives a qualitative feeling for the dominance of tunneling vs. activation, since the systems with pure tunneling exhibit no temperature dependence. Although these results require further investigation, the working hypothesis suggests that in “high-T anneal+ high-T anneal” and “H₂ plasma+H₂ plasma” samples there is still a significant residual non-metallic component. It can be present in the form of non-reduced layers of NiO, or a mix of NiO and Ni, as well as compounds such as NiSiₓOᵧ that at higher temperature leads to activation (hopping) over the random barriers, which is surpassed by direct tunneling at lower temperatures. Unlike that, the “high-T anneal+ H₂ plasma” sample exhibits a very weak deviation from theory over the entire temperature range which is consistent with very small contribution of parasitic residue.

In addition to the extra conductance suppression in the fabricated SETs, a high level of random telegraph signal (RTS) was observed in the measured devices. We believe that the population/depopulation of the traps that are in close proximity of the
island, most likely in the dielectric barrier and the metal-dielectric interface, changes the potential of the island and leads to random change in the conductance through the device. RTS noise has been observed for composite films of Ag-SiO$_2$ and Au-SiO$_2$ and is attributed to the trap sites at the interface between a metal particle and SiO$_2$.\textsuperscript{54}

In devices with double high-T anneal, during the anneal treatment, the temperature-driven catalytic interaction of Pd, and possibly Ni, with SiO$_2$ that is reported to result in Pd$_3$Si formation in H$_2$ ambient\textsuperscript{53}, as well as inter-diffusion of metal-dielectric at high temperatures can aggravate the SNR due to the resulting RTS noise.

Figure 4-2 shows the $G_{ds}(V_{ds})$ at $T=0.4$ K of a device with 12 PEALD cycles of SiO$_2$ as the tunnel barrier in which the parasitic NiO in the junctions were reduced with two high-T anneal. The $V_{ds}$ increment step is lowered to 10 $\mu$V, and this allows detailed acquisition of conductance. The clear jumps in conductance (RTS noise) within $|V_{ds}|\approx E_c/q$ is attributed to random change in the island potential that can increase the conductance through the device as it gets closer to Coulomb blockade. For high $|V_{ds}|$ values where Coulomb blockade is lifted, the conductance is not significantly affected by the slight change in the island potential.
Based on the performed experiments on devices with double H₂ plasma treatments, we believe that the H₂ plasma on the bare dielectric tunnel barrier (with no source/drain of top) results in physical and chemical⁶² damage to the dielectric, since the fabricated devices with H₂ plasma treatment were consistently more than 10× more conductive than those treated with high-T anneal. Moreover, in devices with H₂ plasma treated islands, no significant change in conductance was observed after the nominal thickness of the deposited oxide increased by 30% (from 12 cycles to 16 cycles), whereas the high-T anneal devices with 15 cycles of SiO₂ PEALD exhibited an unmeasurably low conductance. These observations are consistent with non-uniformities, caused by the
damage to the tunnel barrier, that result in areas with thinner dielectric and can significantly change the average resistance over the whole area of the tunnel junctions. The damage on the dielectric caused by the H\textsubscript{2} plasma is also likely to contribute to the observed RTS noise.

Figure 4-3 shows the $G_{ds}(V_{ds})$, at $T=0.4$ K for $V_{ds}$ increment step of 10 $\mu$V, for a device with 12 PEALD cycles of SiO\textsubscript{2} as the tunnel barrier and two H\textsubscript{2} plasma treatments. The inset of the figure shows the RTS noise at $V_{ds}=18$ mV.

![Figure 4-3 G_{ds}(V_{ds}) of a device with 12 PEALD cycles of SiO_{2} as the tunnel barrier and two H_{2} plasma treatments at T=0.4 K for V_{ds} increment step of 10 \mu V](image)

 Clearly, as opposed to the previously observed RTS which was prominent near the $|V_{ds}|<E_{c}/q$, the RTS noise in double H\textsubscript{2} plasma treated samples with 12 SiO\textsubscript{2} PEALD
cycles is more prominent for higher $V_{ds}$ values outside the Coulomb blockade. At this moment, it is not clear to us how different RTS profiles can be related to traps, which are likely located in different areas in the SET devices based on different treatments. Further study regarding this issue is in progress.

The fabricated SET devices with “high-T anneal+ H$_2$ plasma” seem to result in the lowest RTS level. Figure 4-4 shows the charging diagram of two devices fabricated in one batch, with 2:10 PEALD cycles of Al$_2$O$_3$:SiO$_2$ as the tunnel barrier, with islands annealed at the same time for NiO reduction. However, after the source/drain formation, (a) was annealed again at 370°C for 10 min, and (b) was treated with H$_2$ plasma at 300°C for 5 min.
Figure 4-4 The charging diagram of two devices fabricated in one batch, with 2:10 PEALD cycles of Al$_2$O$_3$:SiO$_2$ as the tunnel barrier, with islands annealed at the same time for NiO reduction. However, after the source/drain formations, the (a) was annealed again at 370°C for 10 min, and (b) was treated with H$_2$ plasma at 300°C for 5 min.
Figure 4-5 shows the $G_{ds}(V_{ds})$ of a fabricated device with 2:10 PEALD cycles of Al$_2$O$_3$:SiO$_2$ as the tunnel barrier, that is treated with the explained “high-T anneal+ H$_2$ plasma” reducing steps.

![Graph showing $G_{ds}(V_{ds})$](image)

Figure 4-5 $G_{ds}(V_{ds})$ of a device with 10:2 PEALD cycles of SiO$_2$: Al$_2$O$_3$ as the tunnel barrier and “high-T anneal+ H$_2$ plasma” treatment

There is a remarkably strong noise reduction observed in devices subjected to a combined high-T anneal+H$_2$ plasma and, to a lesser degree, in devices subjected to H$_2$ plasma+H$_2$ plasma treatments. The reason for this is currently under investigation, yet several observations can be made. First, most of the excess noise (i.e. in addition to Johnson and shot noises) appears to have an RTS nature typically associated with random charge trapping/detrapping. Second, the magnitude of excess noise observed in “high-T anneal+ high-T anneal” structures is equivalent to a gate charge fluctuations as large as 0.5e that correspond to jumps between peaks and valleys of CBOs. Importantly, for the
devices with high level of noise (see Figure 3-17, 3-19, 3-23) the noise does not depend on the voltage applied to the gate electrode and is uniformly occurring at any $V_g$. Considering the geometry of the device, such strong charge fluctuations can only occur due to charge trapping/detrapping either within the junction, or in a very close proximity to it. Unlike that, the appearance of the RTS noise in one of the “high-T anneal+H$_2$ plasma” samples is revealed only in the area defined by a combination of $V_g$ and $V_{ds}$ (bottom right corner in Figure 4-6) suggesting that a combination of biases leads to a trap activation. The fact that this noise exhibits itself along the positively sloped diamond line is a strong indication of a trap situated closer to the drain junction, but also coupled to the gate.

![Figure 4-6 Coulomb diamonds at 0.4 K of a device with 12 PEALD SiO$_2$ cycles as the barrier, where the NiO on the island was reduced during a high-T anneal, and the NiO on the bottom of source/drain was reduced in a H$_2$ plasma step.](image)
To summarize, it seems plausible that observed excess RTS noise is caused by charged defects in the ALD layer or at the metal-dielectric interfaces and strong suppression of this noise in “high-T anneal+H₂ plasma” devices is caused by “healing” the charged defects within the junctions.

Additionally, although the use of chemical mechanical polishing and PMGI as the e-beam resist led to fabrication of inlaid islands and source-drain electrodes that are repeatedly less than 20 nm, the charging energy of the fabricated devices have constantly been lower than the value expected from the junction dimensions and dielectric constant of the tunnel barrier. Moreover, from the skewed diamonds in the charging diagram as well as oscillating conductance (see Figure 3-19 and 3-24) in \( G_{ds}(V_{ds}) \) of the fabricated devices, asymmetry in the junction capacitance and conductance can be inferred. We believe that a thinner than expected dielectric layer, perhaps due to a delay in growth during the first few PEALD cycles that results in an average growth rate slower than the nominal value, non-uniformities of dielectric formation, or intermixing of dielectric and Ni at the interfaces are the most possible causes for the observed outcome. Further study regarding this discrepancy is in progress.
The main goal of this project was to investigate the possibilities for fabricating ultra small MIM SETs by using high-resolution e-beam lithography, nanodamascene process, and PEALD to achieve devices with high charging energy and small dimensions capable of detecting electron switching in molecular complexes. There were a number of challenges discovered over the course of the project. We found out that the use of PEALD for tunnel barrier definition results in formation of thin layers of native oxides on both sides of the dielectric that lead to the exponential decrease of device conductance. We show that by employing Ni as metal for MIM junctions it is possible to alleviate the problem of native oxide formation by utilizing NiO reduction process using hydrogen assisted treatments. Furthermore, several detrimental effects were observed while the conditions for NiO reduction were investigated. First is the thermally induced agglomeration of Ni nanostructures that leads to discontinuity in Ni nanowires. Second is the damage to the PEALD dielectric caused by H\textsubscript{2} plasma which exhibits itself in drastic increase of tunnel barrier leakage presumably caused by chemical reduction of the dielectric material (SiO\textsubscript{2}) and formation of silicates or silicide compounds. Third, the majority of MIM SETs that are subjected to the hydrogen assisted reduction of NiO
exhibit significant level of RTS noise. Despite these obstacles, we show that by choosing an optimal combination of treatments it is possible to fabricate MIM SETs with characteristics that closely match the theoretical predictions. In the optimal devices the level of noise does not exceed that observed in MIM devices fabricated by traditional fabrication techniques that employ in-situ oxidation of metals for tunnel barrier formation.

Since the oxygen in the tunnel barrier is believed to be the main cause in the oxidation of metal electrodes and consequent anomalies in the junctions, one would expect a more convenient process flow if the PEALD process for forming the tunnel barrier does not require O\textsubscript{2} plasma and the tunnel dielectric is not composed of oxide. Si\textsubscript{3}N\textsubscript{4}, which is deposited in PEALD system using BDEAS and N\textsubscript{2} plasma, for instance has a dielectric constant of 7 between the one for SiO\textsubscript{2} (≈4) and Al\textsubscript{2}O\textsubscript{3} (≈9) and therefore is a suitable material to form the dielectric barrier in the junctions.

Additionally, other metals can replace the SET electrodes. Ir for instance is a metal in Pt-group and is more resistant to oxidation compared to Ni. Moreover, it has a better adhesion to SiO\textsubscript{2} compared to Pt.

Since one of the main goals in fabricating the SETs is to increase the charging energy and to reduce the tunnel junction capacitance, the use of CMP in a damascene process can be the ultimate technique to fabricate sub 10×10 nm\textsuperscript{2} tunnel junctions, as schematically shown in Figure 5-1. First, a trench in the dielectric field is defined using electron beam lithography and plasma etching. Next, the trench is partially filled by depositing a dielectric layer with atomic layer deposition. The dimensions of the trench
can be tuned by adjusting the thickness of the deposited dielectric in the trench, and therefore a trench with width×height of less than $10 \times 10$ nm$^2$ is potentially achievable. Metal deposition followed by chemical mechanical polishing is then used to fabricate an inlaid tunnel junction in the designed trench. The dimensions of the trench determine the size of the inlaid feature and as a result, tunnel junctions with less than $10 \times 10$ nm$^2$ area is possible.

![Figure 5-1 Damascene process for fabricating the inlaid tunnel junctions where depositing a dielectric in the trench shrinks the dimensions of the inlaid pattern formed in the trench](image-url)
APPENDIX A:

PROCESS RECIPES

TABLE A-1:

THE SUMMARY OF THE PROCESS PARAMETERS USED IN EACH FABRICATION STEP

<table>
<thead>
<tr>
<th>Process</th>
<th>Parameters</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Alignment Marker Fabrication</strong></td>
<td></td>
</tr>
<tr>
<td>I. 4 µm marker lithography:</td>
<td>SPR 700 spun at 4000rpm-90°C bake for 60 sec RTS AutoStep 200: 0.28 sec exposure MIF 917 developing for 45 sec</td>
</tr>
<tr>
<td>II. Oxide etch:</td>
<td>70 sec Oxford Plasma Lab (ICP-RIE): 150 W RIE power, 1000W ICP power 8 mTorr: 20 sccm Ar/15 sccm C₄F₈/15 sccm CHF₃/20 sccm CF₄</td>
</tr>
<tr>
<td>III. XeF₂ etch:</td>
<td>45 sec XeF₂, 200 sccm/N₂ 300 sccm</td>
</tr>
<tr>
<td><strong>Island/Leads EBL</strong></td>
<td></td>
</tr>
<tr>
<td>I. Island: PMGI SF5 at 2500 rpm for 60 sec Leads: PMGI SF5 at 10000 rpm for 60 sec 180 °C bake for 5 min</td>
<td></td>
</tr>
<tr>
<td>II. EBL: Island: 7500 µC/cm² Leads: 8000 µC/cm² 5 nA, 200 µm beam current_apperture Develop in Xylenes for 12 min</td>
<td></td>
</tr>
<tr>
<td><strong>Island/Source-Drain Trench Etch</strong></td>
<td></td>
</tr>
<tr>
<td>I. Oxide etch:</td>
<td>10 sec Oxford Plasma Lab (ICP-RIE): 150 W RIE power, 1000W ICP power 8 mTorr: 20 sccm Ar/15 sccm C₄F₈/15 sccm CHF₃/20 sccm CF₄</td>
</tr>
</tbody>
</table>
### TABLE A-1 (CONTINUED)

<table>
<thead>
<tr>
<th>Process</th>
<th>Parameters</th>
</tr>
</thead>
</table>
| Ni Evaporation +Liftoff         | I.  E-beam Evaporation at $<8 \times 10^{-7}$ mTorr  
60 nm Ni at 2 Å/sec  
I.  Ni Liftoff in MR-Rem 400 at 80°C |
| Ni Planarization (CMP)          | I.  Logitech Orbis CMP  
60 nm Ni for the island: total polish time: 9 sec  
200 nm Ni for the leads: total polish time: 30 sec  
Eminess Ultrasol A19: H₂O 1:1  
Platen/carrier head rotation speed: 60 rpm  
Slurry-dispensing rate: 125 ml/min  
Applied pressure: 0.7 psi |
| Reduction H₂ Plasma             | I.  Oxford FlexAl PEALD system  
2 min Ar purge at 300°C  
II.  5 min H₂ plasma treatment at 300°C :  
50 sccm H₂, 10 mTorr-100 W power  
III.  30 sec final pump/purge |
| Bonding Pads                    | I.  Pads lithography:  
nLOF 2020 spun at 4000 rpm-90°C bake for 60 sec  
RTS AutoStep 200: 0.187 sec exposure  
Post exposure bake at 100°C for 60 sec  
MIF 917 developing for 45 sec  
II.  Pads etched in the oxide (damascene process)  
RIE system: 80 sec  
CHF₃ 7 sccm/Ar 10 sccm/CF₄ 5 sccm/O₂ 5 sccm/SF₆  
7 sccm at 15 mTorr-300 W |
REFERENCES


