DEVELOPMENT OF NANOMETER ION CONDUCTOR FOR 2D-CRYSTAL MEMORY AND UNIVERSAL TUNNEL TRANSISTOR SPICE MODEL

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A universal analytical TFET SPICE (Simulation Program with Integrated Circuit Emphasis) model has been developed to gain more insights into the benefits of TFETs in low power circuit applications and make performance projections. The model is valid in all four operating quadrants of TFETs. Based on the Kane-Sze formula for tunneling, this model captures the distinctive features of TFETs such as steep slope, superlinear onset, ambipolar conduction, and negative differential resistance. The TFET model has been validated on various TFET structures including a planar InAs double-gate TFET, an AlGaSb/InAs in-line TFET, and side-gate GaN/InN/GaN TFET, and good agreement is observed between the model and published simulations. To improve the accuracy of circuit simulation, more components have been added, in particular, a gate current model, a charge-based capacitance model, and a noise model. The model has been implemented in SPICE simulators using Verilog-A and implemented into native AIM-Spice, available on Mac, Windows, Android, and iOS.
Besides steep slope transistor models a further focus of this dissertation has been the exploration of new memory concepts. In particular a flash memory based on graphene and solid polymer electrolytes has been explored with the aim to provide nonvolatility, sub-volt access/program voltage, and low power consumption, but more importantly could provide nanosecond program/erase speed. Processes were developed for deposition of a 2D solid polymer electrolyte, 15-crown-5-ether-substituted cobalt(II) phthalocyanine (CoCrPc), the key enabling technology in the graphene flash memory. The 2D electrolyte was deposited by drop casting a CoCrPc-containing solution onto highly ordered pyrolytic graphite (HOPG) followed by Ar annealing. Atomic Force Microscopy (AFM) confirms that monolayer CoCrPc formation is achieved with a thickness of ~0.5 nm. A highly ordered flat CoCrPc layer with hexagonal symmetry is observed under ultrahigh vacuum scanning tunneling microscopy (UV-STM) and an average spacing of 4.09 ± 0.2 nm is measured. In-situ scanning tunneling spectroscopy (STS) is used to measure the bandgap of CoCrPc, which is 1.34 ± 0.07 eV. To understand the basic physics of ion-electron double layers across an ion conductor with nanometer thickness, a simplified memory structure was proposed and subsequently fabricated and tested. Program tests demonstrate that the memory cell can be programmed and erased by applying positive and negative back gate biases. Retention test indicates that the two states can be maintained for at least 30 minutes. Besides memory, the 2D electrolyte can also serve as a reconfigurable ion gate for 2D semiconductors or a doping technique in 2D FETs and TFETs.
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CHAPTER 1:
INTRODUCTION

In the quest for transistors that can replace CMOS as the power horse of the semiconductor industry, steep slope devices such as tunnel field-effect transistors (TFETs) have emerged as the leading contender because of their capability to keep scaling the supply voltage and lowering the power consumption. Meanwhile, as we approach the scaling limit, two-dimensional (2D) TFETs represent the ultimate low power thin channel device. To this end, it is highly desirable to construct the whole system on the same 2D platform. Therefore it is also important to explore new memory concepts that utilize 2D materials and provide fast program, erase, and read speed and nonvolatility. This chapter begins by introducing the context and motivation of TFETs and flash memory. Then we move on to discuss the memory state-of-the-art, and why new memory concepts are necessary. Next a new graphene flash memory concept is proposed and discussed in detail. Finally we conclude the introduction with the organization of this thesis.

1.1 Moore’s law and scaling

Moore’s law has been the driving force of the semiconductor industry since 1965 [1, 2]. The semiconductor industry has since been dominated by CMOS technology. Its low static power consumption, high noise margins, and high packing density make it the
workhorse of modern electronics. Faster switching speed used to be achieved by merely scaling the transistors size, known as Dennard scaling. The introduction of performance boosters such as strained SiGe channel, high-κ gate dielectrics, metal gates, and FinFET device structure was able to sustain the scaling trend until now, but with one exception, power consumption. Because of the increasing difficulty in reducing the power supply voltage and the off leakage current, the power density in CMOS processors has been increasing. Figure 1.1 shows the exponential increase of the power density with over 7 generations of Intel microprocessors. The power density has surpassed that of a hot plate at the 0.5 μm node and is now only one order of magnitude away from that of a nuclear reactor.

Figure 1.1. Power density of generations of Intel processors (Figure from Pollack [3]).

Figure 1.2 shows the number of transistors, clock speed, power, and performance per clock cycle, perf/clock (measured by ILP, instruction-level parallelism, the number of
instructions that can be executed simultaneously by a processor) of Intel x86 processors from 1970 to 2010. Judging from the number of transistors only, it seems that Moore’s law is still alive and well. But since around 2005, the traditional sources of performance improvements (clock frequency and ILP) have all been flattening, primarily due to the flattening of the CPU power consumption and the inability to keep scaling down the operating voltage.

Figure 1.2. Intel CPU trends from 1970 to 2010 (Figure from Shalf and Bashor [4]).

To mitigate the problem of increasing power consumption with climbing clocking speed, the industry shifted from Dennard scaling to multicore scaling by increasing the
counts of cores while maintaining the clocking speed at ~2 GHz around 2006 [5]. Even some experts in the field were taken by surprise with this sudden end of clock speed scaling. Figure 1.3 shows the sudden change in the International Technology Roadmap for Semiconductors (ITRS) projection for CPU clock rate from 2005 to 2007, which has been remarkably accurate in their projections until then.

However, adding more cores does not result in perfect scaling. First, not all programs can be parallelized. Second, in any parallelized program, performance is ultimately limited by the amount of serial code, code that can only be executed on one processor. Moreover, parallelism overheads, including cost of starting a thread or process, communicating shared data, and synchronizing across a large number of cores, can limit the practical scaling of multicore processors. The conventional multicore scaling approach adopted by the computing industry will eventually hit a performance plateau, just as ILP and clock rate scaling have been flattening since 2003, as shown in Figure 1.2 [4].
ITRS also projects that supply voltage must continue to be reduced to keep the power density from increasing. In Figure 1.4, according to the ITRS projections, the power supply voltage is targeted to decrease by $ \kappa T/q$ (where $\kappa$ is Boltzmann constant, $T$ is temperature in Kelvin, and $q$ is electron charge) for both high performance (HP) and low operating power (LOP) technologies. Because of the fundamental limit of 60 mV/decade subthreshold swing (the gate voltage needed to change the drain current by one decade), MOSFET speed is degraded as supply voltage is reduced below approximately 0.5 V for high performance (HP) CMOS and 0.4 V for low operating power (LOP) CMOS [6]. New materials and transistor concepts are needed to enable scaling beyond CMOS.
1.2 Emerging transistor – tunnel FETs

In the search for devices that can outperform or complement CMOS at low voltages, tunnel FETs (TFETs) have emerged as the leading contender [2, 7-12]. Unlike CMOS, which is limited by the 60 mV/decade at room temperature due to gate-controlled barrier lowering, TFETs utilize field-controlled interband tunneling as the current controlling mechanism. The subthreshold swing of TFETs is no longer limited to 60 mV/decade, but restrained by the sharpness of the exponentially decaying band tails that arise from imperfections and lattice disorders due to dopants, impurities, and phonons [13]. TFETs based on two-dimensional (2D) crystals such as graphene nanoribbon (GNR) and transition metal dichalcogenides (TMDs) such as MoTe$_2$ are projected to provide tunnel currents exceeding 100 $\mu$ A/\mu m at 0.1 V [10] because of their sharp band edge [14] and excellent gate electrostatics as a result of the atomically thin channel.

Figure 1.4. ITRS power supply projections for high performance (HP) and low operating power (LOP) technologies from the Process, Integration, Devices, and Structures (PIDS) tables in 2012 and 2013 (Figure from Seabaugh [6]).
Due to the superior subthreshold characteristics of TFETs that have been both theoretically projected and experimentally demonstrated, circuit designers have started to look into circuits that can maximize the potential of TFETs [15]. To gain more insights into the benefits of TFETs in low power circuit applications and make performance projections, I have developed a universal analytical TFET SPICE (Simulation Program with Integrated Circuit Emphasis) model that captures the essential features of the tunneling process. The model is valid in all four operating quadrants of TFETs. Based on the Kane-Sze formula [16] for tunneling, the model captures the distinctive features of TFETs such as steep slope, superlinear onset, ambipolar conduction, and negative differential resistance (NDR). An empirical charge-based capacitance model, a gate current model, and a primitive noise model have also been implemented. The model has been applied to a variety of TFET structures including a planar InAs double-gate TFET, an AlGaSb/InAs in-line TFET, and a GaN/InN/GaN side-gated TFET, and good agreement is observed between the model and published simulations [17-19]. The model has been implemented in SPICE simulators using Verilog-A and implemented into native AIM-Spice, available on Mac, Windows, Android, and iOS. At the same time, the model has also been made available to the broader nano-community through the NEEDS (Nano-Engineered Electronic Device Simulation Node) platform. NEEDS is an NSF-SRC sponsored program led by Purdue, MIT, UC Berkeley, and Stanford to provide support for the development of compact models for nanoscale devices and their dissemination to the nano-community [20].
1.3 The memory hierarchy

Memory has been an important part of the computer system since the beginning. Back in 1946, Burks, Goldstine, and von Neumann [21] predicted that ideally one would desire an indefinitely fast and large memory, but there exists a trade-off between memory speed and capacity and in a modern computer, it takes $\sim 10^3$ CPU cycles to access the main memory and $\sim 10^6$ CPU cycles to access the disk. The key to bridging this CPU-memory gap is to make use of a fundamental property of computer programs known as locality. Locality says that programs tend to use data and instructions they have recently used (temporal locality) and the data and instructions near those they have used recently (spatial locality). By making use of locality, we can construct a hierarchy of memories and caches (memories inside the CPU), each of which has greater capacity than the preceding level but with slower accessing speed.

Figure 1.5 shows a multilevel memory hierarchy including the typical sizes and access speeds of each level [22]. The goal is to provide a memory system with cost as low as the cheapest level and speed as fast as the fastest level. As one moves farther away from the processor, the memory size increases from KB (CPU register files) to MB (L3 cache), to GB (main memory), and then to TB (storage). The accessing time also increases from less than 1 ns (registers) to ms (disk storage) or $\mu$s (solid state storage).
Figure 1.5. The memory hierarchy in a typical computer system (modified from Figure 2.1 in Hennessy and Patterson [22]). The memory becomes slower and larger as one moves away from the processor, in the order of registers (static read only memory, SRAM), caches (SRAM), memory (dynamic RAM, DRAM) and storage (hard disk drive and/or solid state drive).

Figure 1.6 shows the internal die photograph of a quad-core Intel Core i7 processor. The L1 and L2 cache inside each core are not shown. It is clear that the shared L3 cache takes up a significant part of the chip area, almost 1.5\times the area of a single core.

Figure 1.6. Intel® Core™ i7 processor internal die photograph from Turley [23].
1.4 CPU-Memory gap

Driven by Moore’s law, the CPU cycle time decreases much faster than the main memory (DRAM) access time, and a gap between the two starts to appear around 1985 and has been widening ever since. Figure 1.7 shows the access time of disk, solid-state drive (SSD), DRAM, SRAM (from top to bottom), and the CPU cycle time plotted over time. So far the improvement rate in CPU cycle time exceeds that in memory. The CPU cycle time has been improving at a rate of roughly 60% per year, while memory (DRAM) access time has improved by less than 10% per year with the gap increasing exponentially with time [22, 24]. While the processor industry is focused on computing power, which translates into higher clock frequency and lower CPU cycle time, the memory industry is focused on capacity and cost, which is often traded off with access speed. Another reason for this gap is that in computers DRAM is oftentimes on a separate chip (offchip) from the CPU and this physical distance means increased DRAM access time.

It is worthwhile to notice from Figure 1.7 that the access time of SSD falls in the middle between DRAM and disk. Flash memory is now widely used as a cache layer for disk in personal computers, servers, and warehouse data centers. In the future, SSD may completely replace disks if the manufacturing cost of SSD can be reduced to that of disks [25].
Figure 1.7. The widening gap between DRAM, disk and CPU speeds. Note that the vertical axis must be on a logarithmic scale to record the size of the gap (Figure from Turley [22]).

1.5 Memory landscape

As the CPU-Memory gap keeps enlarging, it becomes imperative to address this gap between processor and main memory. Whereas this problem is mitigated by using multiple levels of caches inside the CPU, the slow speed of main memory and disk is still a bottleneck. With the advent of 2D materials and technology, it becomes possible to make use of their atomically thin dimensions and explore new memory concepts that can bridge the processor–memory performance gap.

The ideal memory would have long retention/nonvolatility, low cost, low power consumption, fast read/program/erase speed, and endurance against write/erase cycles. Figure 1.8 shows the current mainstream memories, memories that are still in prototype,
and a summary of emerging memories. As shown in column 1, the landscape of solid-state memory has been dominated by the hierarchy of DRAM (for main memory), and NAND flash (for mass storage) for a long time because the NAND is optimized for serial access and has limited endurance and DRAM has the advantages in high speed random access and unlimited endurance [25]. SRAM, used mainly in register files and cache inside the processors, is ignored because it is more expensive and less dense than DRAM.

<table>
<thead>
<tr>
<th>Incumbent memories (Mainstream)</th>
<th>Prototypical memories (In limited production)</th>
<th>Emerging memories (test structure level)</th>
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<tbody>
<tr>
<td>DRAM</td>
<td>FeRAM</td>
<td>FeFET</td>
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<tr>
<td>NAND</td>
<td>MRAM</td>
<td>Ferroelectric Polarization RAM</td>
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<td>MLC NAND</td>
<td>PCM</td>
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<td>3D NAND</td>
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Figure 1.8. Memory cell landscape: mainstream memories, prototypical memories, and emerging memories (Figure from Baldi [26]), where the acronyms are defines as follows, dynamic random-access memory (DRAM), NAND flash memory (NAND), multilevel cell NAND (MLC NAND), ferroelectric RAM (FeRAM), magnetic RAM (MRAM), phase change memory (PCM), three-dimensional NAND (3D NAND), ferroelectric FET (FeFET), spin-transfer-torque (STT), thermally assisted STT (TA STT), thermally assisted MRAM (TA MRAM), resistive RAM (RRAM), oxide bridge RRAM (Ox-RRAM), conductive bridge RAM (CBRAM), complementary resistive switch (CRS), nanoelectromechanical memories (NEM memories).
1.6 Flash memory state-of-the-art

Aided by the maturing of multilevel cell (MLC) technology, NAND flash overtook NOR as the dominant flash architecture around the year 2000 when the scaling of NOR flash began to slow down significantly. MLC allows 2 or more bits to be stored in a single cell by using multiple threshold levels to increase density and reduce cost per bit. MLC together with NAND’s superior scalability delivered 50,000x of cumulative cost reductions over the past 20 years and made NAND flash the most popular storage technology [25]. Table 1.1 shows several key features of state-of-the-art NAND flash. It is worthwhile to notice that the development of planar NAND flash is expected to reach the scaling limit in a few technology generations and the technology trend is now taking a shift to 3D NAND flash to increase the integration density of memory cells [27, 28]. Micron was able to pack 768 GB (3b/cell) into 179.2 mm\(^2\), corresponding to 4.29 GB/mm\(^2\) [28]. The average read and program time is still slow compared to the CPU clock rate. The large power supply voltage results because of the difficulty in scaling the tunnel SiO\(_2\) thickness, which is a significant challenge for future NAND transistor scaling [25].
According to the 2015 ITRS projections for flash memory [30], as shown in Table 1.2, 2D (including floating gate and charge trapping) and 3D NAND flash will be the dominant cell type. Whereas 2D flash still scales horizontally by decreasing the minimum feature size, 3D flash scales vertically by increasing the number of memory layers while keeping the minimum feature size constant. As a result, the product density of both 2D and 3D flash will keep increasing. The tunneling oxide is currently 6-7 nm thick and will stay the same for the next 3 generations. The maximum number of bits per cell and nonvolatile data retention will stay the same as well. The endurance – number of erase/write cycles – is projected to decrease from $10^4$ to $5 \times 10^3$ as the technology scales down.
### TABLE 1.2

2015 ITRS PROJECTIONS OF FLASH TECHNOLOGY [30], WHERE FG STANDS FOR FLOATING GATE, AND CT STANDS FOR CHARGE TRAPPING

<table>
<thead>
<tr>
<th>Year of production</th>
<th>2015</th>
<th>2016</th>
<th>2020</th>
<th>2022</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dominant cell type (FG, CT, 3D, etc.)</td>
<td>FG/CT/3D</td>
<td>FG/CT/3D</td>
<td>FG/CT/3D</td>
<td>FG/CT/3D</td>
</tr>
<tr>
<td>2D NAND Flash uncontacted poly 1/2 pitch – F (nm)</td>
<td>15</td>
<td>14</td>
<td>12</td>
<td>12</td>
</tr>
<tr>
<td>3D NAND minimum array 1/2 pitch – F (nm)</td>
<td>80</td>
<td>80</td>
<td>80</td>
<td>80</td>
</tr>
<tr>
<td>3D NAND number of memory layers</td>
<td>32</td>
<td>32-48</td>
<td>64-96</td>
<td>96-128</td>
</tr>
<tr>
<td>Product highest density (2D or 3D)</td>
<td>256 G</td>
<td>384 G</td>
<td>768 G</td>
<td>1 T</td>
</tr>
<tr>
<td>Maximum number of bits per cell</td>
<td>3</td>
<td>3</td>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td>Tunnel oxide thickness (nm)</td>
<td>6-7</td>
<td>6-7</td>
<td>6-7</td>
<td>6-7</td>
</tr>
<tr>
<td>Endurance (erase/write cycles)</td>
<td>1.0E+04</td>
<td>1.0E+04</td>
<td>5.0E+03</td>
<td>5.0E+03</td>
</tr>
<tr>
<td>Nonvolatile data retention (years)</td>
<td>10</td>
<td>10</td>
<td>10</td>
<td>10</td>
</tr>
</tbody>
</table>

### 1.7 Graphene flash memory

A graphene nanoionic flash memory was proposed in a patent application of Seabaugh and Fullerton in 2014 [31]. In contrast to resistive switching RAM (RRAM), which operates by the electrochemical formation and transfer of metal ions or oxygen vacancies between metal electrodes, the proposed memory uses graphene to sense the presence of ions without forming a conductive filament. The proposed graphene nanoionic flash memory is also different from existing graphene flash memory in that there is no charge trapping involved in the program/erase process.

Efetov and Kim showed that graphene can be doped electrostatically with a solid polymer electrolyte, polyethylene oxide (PEO) with LiClO$_4$ salt, with the induced sheet
carrier density as high as $4\times10^{14}/\text{cm}^2$ for both electrons and holes [32]. This is feasible because of the high capacitance density of the ion-electron electric double layer at the polymer electrolyte/graphene interface. One drawback of PEO/LiClO$_4$ is its minimum feature size as PEO is a high-molecular weight polymer. While the thickness of dropcast PEO:LiClO$_4$ film was measured as $\sim1$ $\mu$m in Li [33], thinner films ($\sim100$ nm) can be obtained by spin coating [34]. To reduce the thickness of the electrolyte down to only a few nanometers and achieve nanosecond switching, an alternative ion conductor is required. The ideal ion conductor needs to be easily cast into films a few monolayers thick, lay flat on graphene, be electrically insulating and ionically conductive, and present an energy barrier to Li ions that can be modulated to be low enough for fast switching and high enough for nonvolatility and long retention.

Figure 1.9 shows the circuit symbol and schematic of the originally proposed graphene nanoionic flash memory. It is a four-terminal device with source, drain, top gate and back gate. The back gate modulates the conductivity of the channel by shuttling Li$^+$ back and forth through the 2D electrolyte. Li$^+$ is chosen as the ion because it is the lightest solid element, can pass through the crown ethers that can lay flat on surfaces (i.e., 12-crown-4 and 15-crown-5) [35], has high ion mobility, and is chemically inert at the surface of graphene [36]. The electrolyte layer is chosen to solvate Li$^+$ between the channel and the back gate, and to introduce an electrostatic barrier to ion transport. The top part of the memory cell is a top-gated graphene FET, which is used to sense the presence of Li$^+$. When the Li$^+$ is close to the graphene channel, an electron-Li$^+$ double layer is formed via Coulomb forces that create a low-resistance on state (logic 1). When the Li$^+$ is pulled away from the channel, the device is in a high-resistance off state (logic
The Dirac point also shifts with the presence of Li⁺, with the shift being called the threshold voltage window. The memory cell is nonvolatile because the Li⁺ falls into energy minima on either side of the 2D electrolyte and is held onto the electrons in the graphene channel by non-bonded, Coulomb interactions even when the power is off. Even though the original memory is proposed as an alternative flash memory, it could potentially be used in DRAM if it can deliver similar or faster program/erase speed. Its nonvolatility will be a plus because DRAM is known for being volatile and requires refreshing every milisecond.

In the early stages of this dissertation research, I explored this memory concept with its many technical challenges. First, the 2D electrolyte must be at least a few layers thick to prevent electrons from tunneling across the ion conductor. Depositing a multilayer 2D electrolyte is the first task I addressed, as well as measuring transport in this type of structures. Assembly of the four-terminal memory device involves graphene layer transfer and alignment, which is a nontrivial task. One successful way to configure the device that was explored was to fabricate the top graphene FET structure first and then transfer it onto the bottom structure. However, this is not a process that is readily extendable to a batch fabrication process.
Figure 1.9. Graphene flash memory (a) circuit schematic that utilizes a bit line (BL) and a word line (WL) to address and read the state of the memory. The write line (WR) is used to induce ion motion and change the channel conduction. A graphene back gate shuttles the Li ions between top and bottom graphene surfaces and turns the device (b) on and (c) off. Drawing from Seabaugh and Fullerton [30].

Following this initial exploration we elected to simplify the device geometry to yield a device to help us understand the basic physics of ion-electron double layers across ion conductors with nanometer thickness. The cross-section is shown in Figure 1.10, with the energy band diagrams shown in Figure 1.11. The 2D electrolyte is deposited on top of the graphene channel in a back-gated graphene FET. The memory cell is programmed and erased by pulsing the back gate with a positive and negative voltage, as illustrated in Figure 1.12. The anions (ClO$_4^-$) are likely to be located near the cobalt atom of the CoCrPc because the region of low electronegativity near the cobalt will attract the negatively charge anion. The cations (Li$^+$) in the 2D electrolyte will increase the electric field at the surface and thus more carriers are generated in the graphene. The closer the cations are to the graphene, the stronger the electric field at the surface, and the higher the electron density in the graphene.
At the initial state, the lithium ions are randomly distributed and graphene is n-doped (Figure 1.11a and black line in Figure 1.12). The Li\(^+\) location within the 2D electrolyte is modulated by applying a back gate bias. A positive gate bias pushes the ions further away from the graphene surface, lowers the n-doping, and shifts the Dirac point to the right (Figure 1.11b and green line in Figure 1.12), while a negative gate bias pushes the ions closer to the graphene surface, increases the n-doping, and shifts the Dirac point to the left (Figure 1.11c and blue line in Figure 1.12). While this structure does not promise nanosecond program/erase time, which is hard to estimate without simulations, its easy fabrication allows us to quickly test whether the ions can be modulated by the back gate bias and whether the state can be maintained after the bias is taken away. Subvolt program/erase is not possible with this structure due to the 90 nm thick back gate oxide, which is necessary to identify graphene flakes under optical microscope. Nonvolatility may also suffer because the gate control is not as strong as in the original design.

![Graphene Flash Memory Diagram](image-url)

**Figure 1.10.** Simplified graphene flash memory at (a) logic 1 and (b) logic 0 state.
Figure 1.11. Schematic and band diagrams of the graphene flash memory at (a) initial state ($V_{GS} = 0$ V), (b) logic 1 ($V_{GS} > 0$ V) and (c) logic 0 ($V_{GS} < 0$ V). The drain source voltage $V_{DS}$ is kept at 0 V.

Figure 1.12. Illustration of the current-voltage characteristics of graphene nanoionic flash memory at logic 1 and 0.
1.8 2D electrolyte

One material that we determined can solvate metal ions [37, 38] and be physisorbed onto the graphene surface [39] is the crown ether family. Crown ethers, with the chemical formula $(\text{CH}_2\text{CH}_2\text{O})_n$, where $n$ is the number of repeating units that determines the size of the crown, are essentially 2D rings of PEO. The 15-crown-5 ether molecule, shown in Figure 1.13a, where 15 is the number of atoms in the ring and 5 is the number of oxygen atoms (i.e., 5 repeat units), can lay flat on surfaces and allow Li$^+$ to pass through the center. Density functional theory (DFT) has been used by our collaborators in Prof. K.J. Cho’s group at the University of Texas at Dallas to calculate the energy barrier and elucidate the switching mechanism of the crown ether-Li$^+$ complex [40].
Figure 1.13. (a) Top view of a 15-crown-5 molecule solvating one Li$^+$. (b) Side views of two energetically favorable locations of Li$^+$ on either side of 15-crown-5. Li$^+$, O, C, and H are represented by purple, red, gray, and white spheres. (c) Potential energy, $E$, vs. position between two graphene sheets with the two energy minima indicating the two stable Li$^+$ states in (b). (d) Binding energy, $E_b$, between Li$^+$ (q = +1, missing an electron) and graphene (8×8 unit cells) modulated by Fermi level, $E_F$, from DFT calculations. The parameter $E_A$ is the energy barrier separating the two states; $E_{Dirac}$ is the Dirac point. The figure is unpublished, courtesy of Prof. K. J. Cho, University of Texas, Dallas).

Figure 1.13b shows the two energetically favorable locations of Li$^+$ on either side of 15-crown-5, which correspond to the two energy minima separated by a switching energy barrier, $E_A$, as shown in (c). The barrier needs to be sufficiently low (~0.2 eV) to achieve < 1 ns switching, but sufficiently high (~1.2 eV) to achieve a 1 year retention. The energy barrier can be calculated by using the Arrhenius expression $\tau^{-1} = \nu \exp\left(-E_A/\kappa T\right)$, where $\tau$ is the switching time, $\kappa T$ is the thermal energy, and $\nu$ is the attempt frequency, which is the inverse of the bond vibration time (~$10^{-13} - 10^{-12}$ s).
DFT calculations show that during switching, Li\(^+\) encounters a barrier of 0.2 eV with an electric field of -1.5 V/nm. When the Li\(^+\) is located adjacent to graphene, the Li\(^+\)-electron Coulomb interaction deepens the potential well to meet the retention specification.

DFT calculations also show that the absolute value of the calculated binding energies between 15-crown-5 and Li\(^+\), -3.89 eV, is larger that of Li\(^+\)/graphene, -3 eV. Therefore, Li\(^+\) would prefer to bind to the 15-crown-5, not graphene, which makes it easier to trap Li\(^+\) inside the crown ethers and retention but harder for switching. Figure 1.13d shows that the binding energy between Li\(^+\) and graphene can be modulated by varying the Fermi level in the graphene channel. By moving the Fermi level in graphene by -1 eV through the back gate, the Li\(^+\)/graphene binding energy is increased to -4 eV, exceeding that of Li\(^+\)/crown ether by -0.11 eV.

Crown ethers can lay flat on surfaces if functionalized with metal phthalocyanine (Pc) molecules. Crown ether phthalocyanine molecules, including the one shown in Figure 1.14, can form an ordered monolayer and align parallel to surfaces including Au [37, 38]. The 15-crown-5-ether-substituted cobalt(II) phthalocynine (CoCrPc) molecule, shown in Figure 1.14, solvates\(^1\) metal cations with size smaller than the crown ether rings including Ca\(^{2+}\) [41, 42] and Li\(^+\) and meets the requirement of nanosecond switching and 1 year retention.

\(^1\) (Of a solvent) enter into reversible chemical combination with (a dissolved molecule, ion, etc.).
Figure 1.14. Chemical structure of 15-crown-5-ether-substituted cobalt(II) phthalocynine (CoCrPc) [38].

1.9 Organization of the thesis

My dissertation research has been split between development of a universal TFET SPICE model and exploration of nanoionic memory. Listed below are the publications resulting from this research subject. These are included as Appendices A to E except the second one, which is in preparation and will be submitted.


In this dissertation, I have demonstrated the successful deposition of the monolayer 2D electrolyte, CoCrPc:LiClO$_4$, onto bulk highly ordered pyrolytic graphite (HOPG) substrate and also the graphene channel of a back-gated graphene FET. I also present a universal TFET SPICE model for technology benchmarking and low power circuit simulation.

Chapter 2 discusses the deposition of the 2D electrolyte CoCrPc monolayer, the use of the CoCrPc:LiClO$_4$ in the graphene flash memory cell, as well as other potential applications of the 2D electrolyte. The 2D memory cell was fabricated and tested to characterize program, erase, read, and retention. The initial work on the CoCrPc deposition and morphological characterization was published in paper 1, in collaboration with Prof. Andrew Kummel’s group at University of California, San Diego. The second publication, which is focused on the electric double layer gating of graphene FET, is in preparation.

Chapter 3 presents the universal TFET SPICE model and the methodology used to optimize fitting of the model to higher level device models. Most of the work on TFET SPICE modeling has been published in papers 3–6. The TFET current-voltage (I-V) model in the first quadrant (when both $V_{GS}$ and $V_{DS}$ are positive) was presented at the *2014 International Conference on Ultimate Integration on Silicon (ULIS)* and the proceedings was published. In the follow-up paper in Solid State Electronics, the model
was extended to all operating regions of TFETs including the negative differential resistance (NDR) region and including the ambipolar conduction. A simple analytical capacitance model for the gate drain capacitance was also included. Capacitance models do not conserve charge which is important in switched-capacitor circuits, so in the following paper in the IEEE Journal of Exploratory Solid-State Computational Devices and Circuits I added a charge-based capacitance model to replace the old capacitance model. In addition, a gate current model and a primitive noise model are also added making this the first complete TFET device model. In my other paper on TFETs, “Tunnel field-effect transistors: state-of-the-art,” I summarized published simulations and experiments in TFETs and this paper has been cited more than 80 times in the past 2 years.

In the concluding chapter, Chapter 4, of the dissertation, I discuss future research directions for both 2D flash memory and TFET SPICE model development. Alternative channel material for the 2D memory are proposed to increase the on/off ratio and possible future applications of the technology such as memory selectors are identified. Future improvements of the TFET SPICE model are proposed, such as a physics-based charge model and an improved noise model as the research advances and more experimental data are available. This universal TFET model has been primarily applied for III-V TFETs, the most studied TFET material. This includes the GaN/InN material system. With 2D TFETs on the horizon, it is timely to consider how to expand the model and add support for the 2D material systems.
CHAPTER 2:

2D ELECTROLYTE FOR GRAPHENE NANOIONIC FLASH MEMORY

At the limit of scaling, 2D materials such as graphene, hexagonal boron nitride (h-BN), and TMDs are receiving much attention as potential elements in future electronic devices. While much effort has been devoted to 2D FETs and TFETs, the field of 2D memory has received much less attention. As discussed in the introduction, memory is essential in any electronic system and the development of a 2D memory is equally important for use with 2D transistors.

A 2D nanoionic flash memory based on graphene was proposed in Chapter 1. The memory utilizes a 2D electrolyte, CoCrPc:LiClO₄, to represent logic 1 and 0. Nonvolatility is enabled by the strong binding between the lithium ion and the graphene. The doping effect of CoCrPc:LiClO₄ can also be used to build 2D FETs and TFETs, where doping is essential to the transistor performance. It can also serve as a reconfigurable ion gate for 2D FETs or TFETs. Moreover, with a metal Pc in the center, CoCrPc can also be used as a seeding material for the gate dielectrics.

This chapter is organized as follows: Section 2.1 reviews the literature on the deposition methods of crown ether phthalocyanine. Then Section 2.2 summarizes the work published on the deposition and characterization of CoCrPc as published in [43] (Appendix A). Section 2.3 discusses the fabrication and characterization of the proposed simplified 2D graphene flash memory. Section 2.4 talks about the doping effect of CoCrPc and CoCrPc:LiClO₄ on graphene. The experiments and measurements in Section
2.3 and 2.4 are done in collaboration with visiting research assistant professor Ke Xu from Prof. Susan Fullerton’s group at University of Pittsburgh while he was in Notre Dame (CoCrPc deposition on the device - Lu; device fabrication, electrical measurements - Xu; CO$_2$ annealing - Kinder). A manuscript is in preparation (Xu et al. in draft) and will be submitted during fall 2016. The final Section 2.5 discusses how CoCrPc can be used to seed the ALD growth of gate dielectrics on 2D crystal channels, with the experiment conducted by Iljo Kwak from Prof. Andrew Kummel’s group at U.C. San Diego.

2.1 2D electrolyte – CoCrPc

The CoCrPc molecules, when complexed with Li$^+$, serve as the 2D electrolyte in the memory. CoCrPc was first synthesized by Prof. Nagao Kobayashi, Tohoku University [44-46]. Kobayashi and co-workers demonstrated that the CoCrPc molecules could be deposited in an ordered array and aligned in parallel to an Au(111) substrate simply by dip-coating the substrate in solution [37, 38]. They also demonstrated that crown ethers could complex with Ca$^{2+}$ cations, confirming that crown-ether-substituted Pc derivatives indeed have the ability of complexing with metal cations. Figure 2.1a shows two scanning tunneling microscopy (STM) images of CoCrPc and (b) CoCrPc containing Ca$^{2+}$ monolayer on Au (111) and (c) top and side models of CoCrPc containing Ca$^{2+}$ on an Au(111) surface. Each CoCrPc molecule exhibits a characteristic shape with the brightest spot in the center where the Pc is located. In the absence of Ca$^{2+}$, 4 additional small spots are observed at the corners. With the addition of Ca$^{2+}$, however, only two additional spots are observed at diagonal positions, as a result of the encapsulation of two Ca$^{2+}$ ions into the diagonal crown-ether rings of the CoCrPc molecule. Only two out of
the four crown ether voids trap Ca^{2+} because crown ethers with Ca^{2+} ions favor the site where the crown ether centers align with the center of the three gold atoms (the hexagonal close pack (hcp) and face-centered cubic (fcc) 3-fold hollow sites shown in red in Figure 2.1c). The crown ethers without Ca^{2+}, shown in green, are near bridge sites. It is also shown that CoCrPc on Au(100)-(1×1) does not trap Ca^{2+}. Therefore, the trapping of Ca^{2+} in CoCrPc depends on the crystallographic orientation of Au substrate and the relationship between the crowns and the underlying substrate is very important.

Likewise, Samori [39] deposited a monolayer of phthalocyanine molecules functionalized with ligands (dimethyloctyl substituted 18-crown-6) from a gel onto HOPG substrates. The gel is formed by dissolving the molecules in a 50:1 mixture of CHCl_3 and 1,2,4-trichlorobenzene, with the presence of helical fibers that are composed...
of Pc stacks. Figure 2.2a shows the structure of the molecule and (b) shows the STM image of the gel-HOPG interface. Because the monolayer was deposited from a gel instead of a solution, multiple domains formed with different packing configurations. Figure 2.2c shows a schematic representation of the “face-on” and “edge-on” packing structure. It is important to notice that the thickness of the monolayer will be different depending on the packing structure. The edge-on formation will result in a thin film with greater thickness than the face-on structure.

Figure 2.2. (a) The phthalocyanine molecule functionalized with ligands (dimethyloctyl substituted 18-crown-6) from Samori [39]; (b) STM image of the molecules at the gel-HOPG interface with three main features: (1) a thermodynamically stable, relatively loosely packed hexagonal lattice, (2) a metastable, more densely packed hexagonal phase, and (3, 4) lamellae. (c) Schematic representation showing the packing of molecules at the gel-HOPG surface in both “face-on” (areas 1 and 2 in (b)) and “edge-on” (lamella, areas 3 and 4 in (b)) structures.

Hosokai [47] deposited monolayer and bilayer dibenzo-18-crown-6 on HOPG. Figure 2.3 shows the chemical structure and molecular conformation of the molecule, as well as the molecular orientation in monolayer and bilayer form on HOPG. In the monolayer film in Figure 2.3c, the molecules are oriented upward. In the bilayer film,
alternate orientation of the molecule was observed in the first monolayer (upward) and second layer (downward). The orientation of the molecules is important to study when multilayers of CoCrPc are needed in the electrolyte.

Figure 2.3. (a) Chemical structure and (b) molecular conformation of dibenzo-18-crown-6 molecule from Hosokai [47]. The arrow shows the direction of the electric dipole moment. (c) Schematic molecular orientation and dipole direction of the molecule in monolayer and bilayer films.

2.2 CoCrPc monolayer deposition and characterization

The ability to prepare uniform, ordered and conformal monolayers of CoCrPc molecules represents the first step towards using these materials to provide a 2D electrolyte for the 2D flash memory. With these materials we have successfully formed a monolayer on highly ordered pyrolytic graphite (HOPG) using a solution drop casting method followed by thermal annealing. Because both HOPG and graphene share the same surface chemistry originating from \( sp^3 \) hybridization, it is reasonable to regard
HOPG and graphene as equivalent. The morphology of the CoCrPc monolayer at various annealing temperatures is characterized by AFM using a Bruker Dimension ICON scanning probe microscope.

A uniform and continuous CoCrPc layer is obtained on freshly cleaved HOPG by solution drop casting, followed by thermal annealing under ambient pressure in Ar in the temperature range of 150 – 210 °C. While the quality of the monolayer is independent of annealing time, the composition of the annealing atmosphere is critical. The effect of annealing environment is explored by annealing the sample in Ar and air. We found that exposure to ambient air degrades the quality of the monolayer over the timescale of minutes.

After the success demonstration of a monolayer CoCrPc, our collaborator, Prof. Andrew Kummel’s group from U.C. San Diego, used ultrahigh vacuum STM and scanning tunneling spectroscopy (STS) to characterize the monolayer on the atomic level. Using ultrahigh vacuum STM, a highly ordered and flat CoCrPc layer with hexagonal symmetry and average spacing of 4.09 ± 0.2 nm is observed, corresponding to a packing density of 1/16 nm². The band gap of the CoCrPc, measured by STS, is 1.34 ± 0.07 eV, which is larger than that of Si, 1.17 eV, but much smaller than that of a typical insulator, such as ~9 eV for SiO₂ and ~5 eV for Si₃N₄.

2.3 2D graphene flash memory

2.3.1 Experimental details

After the successful demonstration of monolayer CoCrPc on HOPG, we proceeded with the fabrication and test of the memory device, as shown in Figure 2.4.
The substrate is degenerately doped $p$-type Si substrate with 90 nm of thermal grown SiO$_2$ from Graphene Supermarket. Graphene flakes were mechanically exfoliated from HOPG and then transferred to SiO$_2$/Si substrate using scotch tape. Source and drain contacts were patterned by electron-beam lithography. Metal contacts consisting of Ti (5 nm) and Au (150 nm) were deposited by electron beam evaporation (base pressure $< 1.5 \times 10^{-6}$ Torr) and patterned by lift-off in hot acetone (70 ºC) for 1 hour, followed by mr-Rem 400 remover (Micro Resist Technology GmbH) for 5 minutes. The sample was finally rinsed with isopropanol followed by deionized water.

To reduce the PMMA resist residue left on the graphene FET channel as a residue-free surface is critical in the formation of a monolayer CoCrPc, a 30 minutes anneal in a CO$_2$ environment at 500 ºC was performed in a tube furnace following the method published in [48]. Raman spectroscopy on a separate set of samples was conducted to confirm that the graphene was not oxidized or damaged by the CO$_2$ anneal.
Afterwards, a 10 hour vacuum anneal was conducted in a Cascade Microtech PLC50 Cryogenic vacuum probe station at 127 °C (400 K) under \( \sim 10^{-6} \) Torr to correct the doping effects caused by the CO\(_2\) anneal, which will be discussed in detail in the next section.

Monolayer CoCrPc was deposited using the method discussed in previous section. An initial deposition of 125 µL CoCrPc solution (10 mg/L) was drop cast onto graphene FETs (substrate area \( \sim 1 \times 1 \) cm) in an Ar filled glovebox using a micropipette with a drop volume of 25 µL. To achieve the optimal coverage of CoCrPc on the wafer, a second deposition of 100 µL was applied after the previous drops were evaporated the sample surface appeared dry. A total amount of 225 µL CoCrPc solution is used. After drop casting the sample was transferred onto a hot plate and annealed at 180 °C for 30 minutes.

To prepare the 2D electrolyte, 140 µL of LiClO\(_4\) dissolved in ethanol (Sigma-Aldrich: 99.5% anhydrous ethanol) with a solution concentration of 1 mg/L was drop cast onto CoCrPc coated graphene FETs in an Ar filled glovebox using a micropipette. After deposition the LiClO\(_4\):CoCrPc ratio is 4:5, corresponding to a ratio of 1:5 Li\(^+\):crown ethers (4 crown ethers per CoCrPc molecule). The sample was transferred onto a hot plate and annealed at 180 °C for 30 minutes before removing from the glovebox for electrical measurements.

2.3.2 Programming tests

Two wafers are prepared for the programming tests. The first wafer labeled 1 was tested after each step to track the characteristics of the device and the effects of each processing step. A second wafer labeled 2 was prepared and deposited with only LiClO\(_4\) to isolate the effect of LiClO\(_4\) vs. CoCrPc. Table 2.1 summarizes the shift of Dirac point
and hysteresis between the forward and backward sweep, as observed from the $I$-$V$ measurements of the two wafers shown in Figures 2.5, 2.6, and 2.8. The effects of the processing steps are discussed following each figure.

Figure 2.5 shows the transfer characteristics of the graphene FET before CO$_2$ anneal, after CO$_2$ anneal, and after vacuum anneal. The graphene FET after metal liftoff is taken as the base line, and shows Dirac point around 2 V with no hysteresis, as shown in Figure 2.5a. After the CO$_2$ anneal, all devices shown strong $p$-doping with the Dirac point shifted to the right by more than 30 V, way out of the measuring window (-30 – 30 V), as shown in Figure 2.5b. The measuring window is cut off at 30 V to avoid oxide breakdown. The strong $p$-doping after the CO$_2$ anneal may be caused by high annealing temperature and H$_2$O and O$_2$ absorption. To remove adsorbates that could potentially cause $p$-type doping, the first wafer was annealed for 10 hours under vacuum (~10$^6$ Torr) at 127 °C. After vacuum annealing, the Dirac point shifted back into the measurement window and the hysteresis vanished (Figure 2.5b). The second wafer is not treated with CO$_2$ anneal and therefore vacuum anneal is not necessary.
TABLE 2.1

CONTROL SAMPLES WITH MEASURED DIRAC POINT POSITION AND HYSTERESIS

<table>
<thead>
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<th>Wafer No.</th>
<th>Sample</th>
<th>Dirac point</th>
<th>Hysteresis</th>
</tr>
</thead>
<tbody>
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<td>Graphene FET</td>
<td>~ 2 V</td>
<td>No</td>
</tr>
<tr>
<td>1</td>
<td>Graphene FET with CO2 anneal</td>
<td>&gt; 30 V</td>
<td>Yes</td>
</tr>
<tr>
<td>1</td>
<td>Graphene FET with CO2 anneal and vacuum anneal</td>
<td>~ 15 V</td>
<td>No</td>
</tr>
<tr>
<td>1</td>
<td>Graphene FET with CO2 anneal, vacuum anneal, and CoCrPc</td>
<td>~ –30 V, ~ 0 V</td>
<td>Yes</td>
</tr>
<tr>
<td>1</td>
<td>Graphene FET with CO2 anneal, vacuum anneal, CoCrPc, and LiClO4</td>
<td>~ 0 V</td>
<td>Yes</td>
</tr>
<tr>
<td>2</td>
<td>Graphene FET with LiClO4</td>
<td>&lt; –40 V</td>
<td>No</td>
</tr>
</tbody>
</table>

Figure 2.5. Transfer characteristics of (a) the as-fabricated graphene FET, (b) before and after CO₂ anneal, and after vacuum anneal.

Next, a monolayer of CoCrPc was deposited on the same sample. Following CoCrPc, LiClO₄ is deposited via drop casting and annealing with a Li⁺:crown ether molar...
ratio of 1:5. Besides the double $I-V$ sweep, a series of programming tests was applied to characterize the memory effect. First, a double sweep transfer curve was taken to determine the original Dirac point location (black curve). Next, a positive back gate bias, $V_{BG} = 30$ V, was applied for 5 minutes to push $\text{Li}^+$ away from graphene surface, and a single sweep transfer curve was taken immediately after to record the Dirac point shift (blue curve, $V_{BG}$ sweeps from 30 V to −30 V). Lastly, a negative back gate bias, $V_{BG} = −30$ V, was applied for 5 minutes to pull $\text{Li}^+$ close to graphene surface, which is also followed by a single sweep transfer curve (red curve, $V_{BG}$ sweeps from −30 V to 30 V). The sweep rate (6 V/s) is chosen to minimize the movement of $\text{Li}^+$ during the measurement so that the measured Dirac point is as accurate as possible. Neither the ± 30 V programming bias nor the 5-minute programming time were optimized and are simply a record of the performed tests.

Figure 2.6 shows the series of programming tests conducted on (a) bare graphene FETs after vacuum anneal, then (b) after the deposition of CoCrPc, and then (c) after the deposition of LiClO$_4$, with the first two sets as control experiments. As shown in Figure 2.6d, DFT calculations by Prof. K.J. Cho’s group at the University of Texas at Dallas show that crown ether (CE) and graphene exhibit two different contact configurations [40]: 1) CE(O) with the O atoms close to the graphene surface, and 2) CE(H) with H atoms close to but O atoms away from the graphene surface. The chemical interaction between the CE and the graphene would cause charge transfer and charge redistribution in the CE/graphene system, which would form electric dipoles at the interface and eventually lead to the change of work function and doping of graphene. Positive bias would attract O atoms which are more electronegative, resulting in a CE(O) contact.
configuration at the interface and $p$-doping of graphene (Figure 2.6b red curve). On the contrary, negative bias would push O atoms away, forming CE(H) contact configuration and $n$-type doping inside graphene (Figure 2.6b blue curve) and causing the left shift of Dirac point after adding CoCrPc right before any programming tests. As a result of the two stable states, hysteresis is observed in double-sweep transfer scans (black lines in Figure 2.6b).

Figure 2.6c shows the programming test result after the deposition of LiClO$_4$. As introduced in Chapter 1, the states of the memory cell are represented by the location of the Li$^+$ with respect to the graphene channel, which is modulated by the back gate voltage. Positive back gate voltage pushes Li$^+$ away from the graphene surface, weakening the $n$-type doping, and shifting the Dirac point to the right (Figure 2.6c red curve), while negative back gate voltage pulls Li$^+$ closer to graphene surface, inducing image charges, increasing $n$-type doping, and shifting the Dirac point to the left (Figure 2.6c blue curve). Even larger hysteresis in the double-sweep transfer scan is observed (Figure 2.6c black curve), because Li$^+$ responds more strongly to back gate bias.

The measured transfer characteristics shown in Figure 2.6c differ from the hand drawing in Figure 1.12 in the initial Dirac point position because the $n$-doping induced by CoCrPc neutralizes the strong $p$-doping caused by CO$_2$ anneal. The shift of the Dirac point after programming and erasing is as predicted. Hysteresis is not included in Figure 1.12 and thus not compared.
Figure 2.6. Electrical device characteristics of graphene FETs (a) after vacuum anneal, (b) after depositing CoCrPc, and (c) after depositing LiClO₄. (d) Side view of crown ethers (CEs) over graphene with two configurations: CE(O) with the O atoms close to graphene and CE(H) with the H atoms close to graphene.

**Discussions on bistability.** Figure 2.7 shows the shift of the Dirac point after the ±30 V program/erase test. The magnitude of the shift increased by more than 4 times compared with devices with CoCrPc only. Based on DFT calculations by Prof. K.J. Cho’s group at the University of Texas at Dallas [40], Li⁺ within the crowns of the CoCrPc molecules can be switched between the two contact configurations by applying a back gate voltage, as illustrated in Figure 1.13b. Meanwhile, the graphene channel is doped, leading to the shift of Dirac point after programming.
The magnitude of the shift for devices with CoCrPc and LiClO$_4$ is increased compared to devices with only CoCrPc, because Li$^+$ interacts more strongly with graphene to induce electrons and Li$^+$ can move closer to or further away from the graphene surface than the O atoms in the crown ethers. The blue bar, which represents the left Dirac point shift caused by is moving Li$^+$ or O atoms in the crown ether closer to graphene, is much taller than the red bar, which represents the right Dirac point shift caused by moving Li$^+$ or O atoms in the crown ether away from surface, consistent with the assumption that the anions, LiClO$_4$, are loosely attached to the Co atom and away from the channel.

![Figure 2.7. Dirac point shifts after ± 30 V programming tests for graphene FET (GFET), GFET + CoCrPc, and GFET + CoCrPc + LiClO$_4$. Error bar represents one standard deviation from the mean.](image)

One more control experiment on wafer 2 was conducted where LiClO$_4$ was deposited directly onto bare graphene FETs without any CoCrPc (the last row in Table 2.1). This purpose of this experiment is to confirm the source of the Dirac point shift is
moving Li$^+$ within the CoCrPc rather than moving Li$^+$ directly on the graphene surface. The same concentration of LiClO$_4$ equivalent to that of CoCrPc:LiClO$_4$ in the previous experiments was used. As shown in Figure 2.8, after adding LiClO$_4$, the graphene FET is strongly $n$-type doped, with the Dirac point shifted to the left by more than 40 V, way out of the measurement window, which suggests that Li$^+$ is near the surface while ClO$_4^-$ are further away because if the cations and anions were uniformly distributed on the graphene surface, no net doping would be observed and the Dirac point should remain around 0 V.

![Figure 2.8. Transfer characteristics of before and after adding LiClO$_4$ (no CO$_2$ or vacuum anneal).](image-url)
2.3.3 Memory tests

Following the characterization described in the last section, program/erase tests and retention tests were performed on the 2D memory wafer 1 (graphene FET with CoCrPc and LiClO$_4$).

**Program/erase test.** In this test, the drain voltage, $V_{DS}$, was fixed at 0.5 V while monitoring the drain current, $I_D$, continuously. The 0.5 V $V_{DS}$ was chosen to minimize the disturbing to the memory state during reading but still large enough to distinguish the two memory states. The device was programmed (logic 1) by applying a positive 40 V back gate voltage and erased (logic 0) by applying a negative 40 V back gate voltage, as shown in Figure 2.10a. The back gate voltage was held for a certain amount of time (i.e., the step width) to allow the Li$^+$ to respond. Figure 2.10b and d show the step tests with two different step widths, 9 s and 60 s. Program moves the Li$^+$ away from graphene surface, giving rise to a graphene/crown ether/Li$^+$ contact configuration. In contrast, erase moves the Li$^+$ towards the graphene surface to create the graphene/Li$^+$/ crown ether contact configuration. The memory state is read by measuring the drain current ($I_D$) at the same $V_{DS}$ in the absence of back gate bias ($V_{BG} = 0$ V).

Figure 2.10c shows $\Delta I_D$ plotted as a function of step width. $\Delta I_D$ is defined as the difference between $I_D$ after program after erase. To investigate the relation between $\Delta I_D$ and step width, the step tests are repeated with step widths of 3, 6, 9, and 60 s. For the 3, 6, 9 s step width tests one test cycle period is 40 s. For the 60 s step width test, the period is 180 s, the read time is 30 s each, and the cycle was repeated for 3 times. Data is averaged over 5 step cycles (3 for 60 s step width), and the error bar shows one standard
deviation away from the mean. Experiments with different step widths of 3, 6, 9, and 60 s suggest that longer program/erase time result in larger difference in $\Delta I_D$.

Figure 2.9. (a) Illustration for program (logic 1) and erase (logic 0) using the back gate voltage ($V_{BG}$). (b) Step test with 9 s step width. (c) $\Delta I_D$ right after program/erase step (start) and $\Delta I_D$ just before the next program/erase step (end). $\Delta I_D$ is averaged over 5 step cycles (3 for 60 s step width), and error bars indicate one standard deviation from the mean. (d) Step test with 60 s of step width. In (b) and (d) the 3rd row is a zoomed in view of $I_D$ from the shaded area in 2nd row.

**Retention test.** To further investigate the non-volatility of the device, a retention test was conducted by first applying a 60 s program/erase step, then grounding the back gate and monitoring $I_D$ for 30 minutes, as shown in Figure 2.10a. The two memory states,
represented by different drain current level, remained distinguishable even 30 minutes after removing the program/erase bias, with the difference, denoted by $\Delta I_D$, dropping from $\sim 50 \, \mu A$ immediately after the $V_{BG}$ step to $\sim 10 \, \mu A$ 30 minutes later. The relaxation time of the 2D electrolyte is estimated to be in the timescale of $10^3$ seconds, approximately $10^6$ times longer than the retention time of conventional solid polymer electrolytes, such as PEO:LiClO$_4$, which typically has a relaxation time of a few ms at room temperature [33].

![Figure 2.10.](image)

Figure 2.10. (a) Retention test with 60 s step width and 30 minutes of monitoring time. The 3rd row is a zoomed in view of the drain current from the shaded area in the 2nd row. (b) Drain current ($I_D$) as a function of time after removing the back gate voltage.

**Discussions on ion response time.** As shown the measurements in Figure 2.9, the program/erase speed of this 2D memory is on the scale of seconds, and the memory window – the shift of the Dirac point in this case – increases with the program/erase time. Classical molecular dynamics (MD) simulations by Uysal [49] show that there exist a fast and slow process in the formation of the electric double layer (EDL) structure of a room.
temperature ionic liquid electrolyte at an epitaxial graphene surface. The ions are uniformly distributed in the electrolyte. The moment the electric field is applied to the electrolyte, the ions at the interface react to the applied field on a nanosecond timescale and induce carriers in the graphene, which is referred to as the fast process. The slow process involves ions located further away from the surface, which may need much longer time (on a timescale of seconds) to drift to the electrode. It remains an open question that how much charge density the fast process can induce compared to the slow process.

It is clear that the ion transport process observed in the 2D memory is on a timescale of seconds and thus a slow process. However given the structural difference between the vertical graphene/ionic liquid/graphene structure and the horizontal structure shown in Figure 2.4, it is unclear whether the mechanism of the fast process occurs in the 2D memory. For one thing, the direction of the electric field is not vertical near the graphene/CoCrPc surface. The electric field may also be partially screened by the electrons in the graphene channel, increasing the switching time of the memory. Moreover, the fast process happens much quicker than the time resolution for the semiconductor analyzer (~0.5 s) and new approaches need to be developed for shorter time measurement.

2.3.4 Discussions on memory target attributes

Back when the original graphene flash memory was proposed, some of its target attributes include nonvolatility, nanosecond program/erase, and subvolt operation. However due to the challenges facing the assembly of the original design, the memory structure is significantly simplified for ease of device fabrication. At the same time,
because of the 90 nm back gate oxide used, which is necessary to distinguish graphene flakes under optical microscope, subvolt operation is compromised, which is confirmed by the transfer characteristics. As demonstrated by the program/erase tests, the program/erase speed is on the scale of seconds, which can be potentially faster if the fast process discussed in the previous section can be uncovered and utilized. The retention test has shown that the memory can retain its state for at least 30 minutes, which is significantly shorter than that required by flash memory (10 years), but longer than that of DRAM (~1 ms), making the memory suitable for DRAM applications, if the program/erase speed can be improved further.

2.4 Potential applications of CoCrPc as a doping technology

Electronic devices based on 2D crystals require doping methods. There are three common approaches to doping: substitutional, charge transfer, and electrostatic doping using either a metal gate or ions. Substitutional doping changes the optical band gap and can introduce defects that degrade electrical performance [50]. Charge transfer dopants, which rely on molecular physisorption, including NO$_x$ [51], SiN$_x$ [52], K [53], and benzyl viologen [54] are currently being explored. Similar to metal gates, ionic liquids and solid polymer electrolytes do not involve charge transfer, but instead rely on electrostatics to induce image charge in the semiconductor. Electrolytes such as DEME-TFSI,$^2$ EMIM-TFSI,$^3$ and PEO with LiClO$_4$ or CsClO$_4$ have been used extensively for reconfigurable doping of graphene [32, 55, 56] and TMDs [57-59].

---

$^2$ N,N-Diethyl-2-methoxy-N-methylethanaminium bis[(trifluoromethyl)sulfonyl]azanide  
$^3$ 1-ethyl-3-methylimidazolium bis(trifluoromethylsulfonyl)imide
As discussed previously, CoCrPc is a promising 2D electrolyte to provide doping to 2D crystals, where image charges are induced by lithium ions by applying a back gate bias. The Dirac point shift towards right/left after positive/negative programming tests, indicating that the doping is reconfigurable. The magnitude of the Dirac point shift indicates doping densities of \(~5 \times 10^{12}\) cm\(^{-2}\) for a crown ether to Li\(^+\) ratio of 5:1. Theoretically, each crown ether can accommodate one Li\(^+\), meaning that with a crown ether to Li\(^+\) ratio of 1:1, the maximum carrier density can be as high as \(~2.5 \times 10^{13}\) cm\(^{-2}\).

2.5 CoCrPc as an ALD seeding layer

High performance transistors based on 2D crystals require thin and defect-free gate dielectrics. However, due to the absence of dangling bonds, 2D semiconductors are generally unreactive, thereby making the deposition of dielectrics on the surface of these materials challenging. One approach to address this problem is the deposition of a seed layer onto which a gate dielectric is deposited [60]. The metal atom of the metal phthalocyanine (MPc) interacts strongly with the substrate [37, 38], enabling the use of MPcs to seed atomic layer deposition growth of high-\(\kappa\) dielectrics [60].

MPcs and their derivatives can be deposited in ultra high vacuum (UHV) by molecular beam epitaxy (MBE) onto Au(111) [61], graphene [62-64], and TMDs [60] to form perfectly ordered monolayers. Because of their excellent film growth and electronic properties, an MPc monolayer can be used to nucleate ALD of wide band gap oxides, such as Al\(_2\)O\(_3\) [65]. Although MBE deposition of MPcs allows for precise control of layer thickness for use as a crystalline multilayer, a monolayer of MPcs also can be prepared by simple solution phase deposition, which is more practical for commercial application.
compared to MBE, because solution deposition can be done at atmospheric pressure. For example, Kong et al. prepared a monolayer of TiOPc by drop casting from solution (1 µM TiOPc in toluene) onto freshly cleaved, HOPG and Au(111) under ambient conditions and performed STM measurements [66]. Their STM observations revealed that TiOPc molecules form a hexagonally packed monolayer on both substrates.

When the MPc molecule is functionalized with crown ethers, such as CoCrPc, the molecule can also function as a seeding layer for the atomic layer deposition of high-κ dielectrics. The Kummel group at UC San Diego studied ALD Al₂O₃ with CoCrPc as the seeding layer. We have concluded from our experiments that CoCrPc annealed in a water-free Ar environment is of the best quality and air exposure degrades the monolayer in the time frame of minutes [43]. Because Ar annealing is not available in UCSD, they used air annealing instead. Figure 2.11 shows the AFM images and line scan of ALD Al₂O₃ seeded with a monolayer of CoCrPc on HOPG. The CoCrPc was first dissolved in a mixture of benzene/ethanol (v/v 9: 1) with a concentration of 0.3 mg/L, and then drop cast onto freshly cleaved HOPG twice to achieve full coverage. The sample was annealed in air at 180 °C for 30 minutes. Then 30 cycles of Al₂O₃ is deposited via ALD at 120 °C with 20 cycles of trimethyl aluminum(TMA) prepulse. As can be seen from Figure 2.11a and b, Al₂O₃ successfully nucleated on CoCrPc, but many pinholes are observed, probably due to pinholes in the CoCrPc seeding layer. The height of the pinhole is ~3 nm, as measured by line scan in Figure 2.11c, equivalent to the thickness of 30 cycles of ALD Al₂O₃.
Figure 2.11. (a) and (b) AFM images and (c) line scan of 30 cycles of ALD Al₂O₃ on CoCrPc on HOPG with air anneal. The scanning area is (a) 5×5 μm² and (b) 2×2 μm² (unpublished work courtesy of Iljo Kwak and Prof. Andrew Kummel of UC San Diego).

Although the CoCrPc seeded Al₂O₃ is not pinhole-free, it does shown that CoCrPc has the ability to nucleate the ALD growth of Al₂O₃. To get pinhole-free Al₂O₃, the seeding layer must be free of pinholes, impurities, and defects, which has been demonstrated with UHV MBE grown TiOPc [60], but is very challenging with simple solution drop cast. Figure 2.12 shows the AFM image of a CoCrPc monolayer on HOPG prepared by drop casting followed by annealing in Ar for 30 minutes at 150 °C, from our previously published paper on the deposition and characterization of monolayer CoCrPc [43]. As shown in the figure, annealing in Ar at 150 °C yields nearly complete CoCrPc
coverage on the mesas as the CoCrPc film becomes continuous and uniform. However the continuity of the CoCrPc film is broken along the mesa edges and near the particles. In summary, CoCrPc is capable of nucleating ALD Al₂O₃, but in order to use CoCrPc as a seeding layer, we need to improve the purity of the CoCrPc source and optimize the deposition method so that pinhole-free films can be formed.

Figure 2.12. AFM image of a CoCrPc monolayer on HOPG prepared by drop casting 34 μL/cm² of 13 mg/L CoCrPc benzene-ethanol (9:1 v/v) solution followed by annealing in Ar for 30 minutes at 150 °C. The image size is 2 × 2 μm². The white particles are likely CoCrPc aggregates. This figure is from our previously published work [43] (Appendix A).
TFETs continue to be widely investigated to achieve sub-60-mV/decade subthreshold swing at room temperature for low power digital and analog applications [7, 10, 12, 67, 68]. To build TFET circuits and make performance projections, it is of interest to develop simple, closed-form expressions for the drain current that contain the basic physics of the tunneling process and can be implemented in circuit simulators, e.g. SPICE.

In this chapter, the universal TFET SPICE model developed in this research is described. The model provides a simple and continuous equation for the current-voltage characteristics of the TFET developed. The formulation is shown to be widely applicable across materials systems and device geometries. Fitting parameters are introduced into the equations to improve the fitting accuracy of the model.

The model was developed in several stages and each published paper represents a single stage. In the first stage, a continuous physics-based analytic model was developed to capture the essential features of the TFET [18], such as gate-bias-dependent subthreshold swing and superlinear current onset. In the second stage, the model was extended to include all four quadrants of the current-voltage characteristic [17] including the negative differential resistance of the source Esaki tunnel junction and an empirical capacitance model. However, since the capacitance model was not charge-based, charge
conservation was not guaranteed. In the third stage, the model was enhanced by including a charge-based capacitance model, gate tunneling current, and a noise model [19]. The supplementary information of [19] contains a full list of equations implemented in the latest version of the Verilog-A implementation of the model and parameters extracted by fitting to TCAD simulation data of GaN/InN/GaN TFET.

The model is coded in Verilog-A, which is well supported by all major commercial circuit simulators, such as HSPICE from Synopsys, Spectre from Cadence, and Eldo from Mentor Graphics. The Verilog-A code is then converted to C code and built into free circuit simulator AIM-Spice [69], available on multiple platforms including Windows, Mac OS, Android, and iOS.

This chapter is organized as follows. Section 3.1 presents the working principle of TFETs. TFETs rely on tunneling to conduct current, which is not limited to the room temperature 60 mV/decade subthreshold swing of MOSFETs. Section 3.2 summarizes the set of models included in the universal TFET model. Section 3.3 talks about the implementation details and optimization techniques of the SPICE model and the changes made to improve the fitting of the model. Section 3.4 outlines the fitting procedure of the SPICE model.

3.1 Working principle of TFETs

A TFET is essentially a gated $p-i-n$ tunnel diode and utilizes an MOS-gate to control the band-to-band tunneling across a degenerate $p-n$ junction. It typically has three terminals, gate (G), drain (D), and source (S). A body terminal is typically absent due to the extreme thin body of TFETs. The schematic cross-section and energy band diagrams
of $n$-channel TFET in off and on states are shown in Figure 3.1. The device is normally off. When zero bias is applied to the gate, the conduction band minimum of the channel is located above the valence band maximum of the source, so band-to-band tunneling is suppressed. A tunneling window opens up as the conduction band of the channel is shifted below the valence band of the source. Electrons in the valence band with energy in this tunneling window tunnel into empty states in the channel and the transistor is on.

The asymmetrical source/drain junction causes TFETs to have asymmetrical characteristics when the drain-source bias is reversed. When forwardly biased ($V_{DS} < 0$), the band-to-band tunneling current gradually gives way to the diffusion current as $V_{DS}$ is decreased, resulting in negative differential resistance in the $I_D-V_{DS}$. Also due to the asymmetrical doping, the tunnel junction shifts from the source-channel junction to drain-channel junction when the gate bias reverses, resulting in ambipolar conduction, which increases the design complexities of TFET circuits, especially in switch capacitor circuits. In cases where ambipolar current is undesired, GaN/InN/GaN TFETs are a good choice because due to the large bandgap of GaN, the ambipolar current is greatly suppressed and numerical simulation shows no current conduction at negative $V_{GS}$ [70]. The four quadrants are defined in Table 3.1.
Figure 3.1. Schematic cross-section and energy band diagram of an n-channel TFET when the device is biased in (a) off, (b) on-state, and (c) ambipolar conduction state where the symbols are defined as follows: $E_C$, conduction band, $E_V$, valence band, $V_{GS}$, gate-source voltage, $V_{DS}$, drain-source voltage, and $V_{TW}$, tunneling window.

### TABLE 3.1

<table>
<thead>
<tr>
<th>Quadrant</th>
<th>Voltages</th>
<th>Current conducting mechanism</th>
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<tbody>
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<td>I</td>
<td>$V_{GS} \geq 0, V_{DS} \geq 0$</td>
<td>Band-to-band tunneling</td>
</tr>
<tr>
<td>II</td>
<td>$V_{GS} &lt; 0, V_{DS} \geq 0$</td>
<td>Ambipolar current conduction</td>
</tr>
<tr>
<td>III</td>
<td>$V_{GS} &lt; 0, V_{DS} \leq 0$</td>
<td>Diode diffusion current</td>
</tr>
<tr>
<td>IV</td>
<td>$V_{GS} &lt; 0, V_{DS} &lt; 0$</td>
<td>Diode diffusion current &amp; tunneling current (NDR region)</td>
</tr>
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3.2 Overview and highlights of TFET SPICE model

This section presents an overview of the TFET SPICE model. It covers an essential set of models including I-V model, capacitance model, gate current model, and
noise model. Temperature is not included as a model parameter. If necessary, the model can be refitted to data at temperatures different from room temperature. For the model equations, the supplementary information of [19], is the best reference.

3.2.1 I-V model

I-V model is the core of an analytic device model. Accurate modeling of the I-V characteristics is a basic requirement of a good compact model. The central expression in the TFET model is an experimentally well-established equation for band-to-band, Zener tunneling in p-n junctions, the primary transport mechanism in tunnel transistors [12]. The two-terminal Zener tunneling behavior is then generalized to three terminals by introducing physics-based expressions for the bias-dependent tunneling window and a dimensionless factor which accounts for the superlinear current onset in the output characteristic. Figure 3.2 shows the modeled and TCAD simulated transfer and output characteristics of a sidewall double-gated GaN/InN TFET. Both the steep slope and the superlinear current onset are well captured by the model.
Because TFETs conduct current in all four quadrants, the $I-V$ model needs to be valid in those operating regions too. Because different current conducting mechanisms are involved, different expressions must be used to model the currents. In the second quadrant, the ambipolar current is tunneling current happening at the channel-drain junction. So the same tunneling model can be utilized to model the ambipolar current, by simply flipping the sign of $V_{GS}$. By adding a fitting function to the tunneling window expression in quadrant I, the NDR in the fourth quadrant can be modeled without adding anything else, as shown in Figure 3.3. The diode diffusion current in the fourth quadrant is modeled by the classical diode model. In the rarely visited third quadrant, the current is dominated by the diode diffusion current.

Figure 3.2. TCAD-simulated and modeled (a) transfer and (b) output characteristics of sidewall double-gated GaN/InN TFET (Figure from Appendix E).
Since different expressions are used to model the current in different quadrants, the $I-V$ model is no longer a single expression model. To avoid using if statements in the Verilog-A code, limiting expressions are used to turn off the component in regions that it is insignificant, which will be discussed in detail in section 3.3.

3.2.2 Capacitance model

Besides $I-V$ model, the capacitance model is another essential component of a compact device model for circuit simulation. Charge conserving model is usually favored over a model that does not guaranty charge conservation, because charge non-conservation can lead to non-physical results when used to simulate circuits that have charge storage nodes [71]. Charge built-up on these nodes are incorrectly predicted by simulation, often seen in charge pumps, static RAM, and switched-capacitor circuits [71].
Therefore the proper way to model capacitances is to assign charges to each terminal and model the charge directly. This is exactly the approach we used to model the TFET capacitances in the universal model. Empirical expressions are used to describe the drain and source charges. The gate charge is calculated by using the charge neutrality principle. This way, charge conservation is naturally guaranteed.

3.2.3 Gate current model

Band to band tunneling current not only occurs at the source-channel junction or channel-drain junction, it also occurs at the surface of the channel under the gate, especially when the gate oxide is only a few nanometers thick. As any other forms of leakage current, gate tunneling current will contribute to standby power and increase power consumption. But in the case of TFETs, significant amount of gate current will also degrade subthreshold swing, as well as other related figure-of-merits such as $g_m$ and $g_m/I_d$, and thus limiting the analog circuit performances.

Given the structural similarity between TFETs and MOSFETs (both have a MOS structure), the gate current model for TFETs can be modeled by modifying the MOSFET gate current model [19, 72]. Depending on the specific device, the partition of the gate current between source and drain can be vastly different. When the gate is primarily overlapped with the drain, such as in GaN/InN/GaN TFET, almost all of the gate current goes to the drain.

3.2.4 Noise model

The consideration of noise is increasingly important in compact device modeling, not only in analog and RF applications, but also in digital applications where noise can be
the limiting factor as in ultra-low-voltage circuit design. Due to the limited studies and reported data available, an entry-level noise model is included for exploring the limitations imposed by noise in TFET circuits.

Figure 3.4. (a) Origin of $1/f$ and $1/f^2$ noise in TFETs. (b) Measured drain current spectral density $S_{id}$ of six individual TFETs biased at $V_{DS} = 100$ mV, $V_{GS} = 0.6$ V. (c) TFET noise model consisting of $1/f$ noise in the gate and shot noise source at the source/channel junction (Figure a and b from Huang [74], c from Appendix E).

In the experimental reports low frequency noise is dominated by either flicker noise, with the form of $1/f$, or random telegraph noise (RTN), with the form of $1/f^2$ [73, 74]. As shown in Figure 3.4a, Flicker noise and RTN result from trapping-detrapping at the oxide/semiconductor surface at the channel and at the source/channel junction. The trapping-detrapping behavior, which causes fluctuation in the number of carriers, changes the internal tunnel-junction field and therefore the tunneling current, because the tunneling current is a function of the internal electric field at the tunnel junction [74]. The effective low frequency noise generating area is generally small in TFETs, therefore,
TFET low frequency noise shows a weak dependence on gate length, and is subject to noise variability due to differences in trap locations and densities in the active area, as shown by the noise measurements of six individual TFETs in Figure 3.4b. It is worthwhile to note that besides the $1/f$ and $1/f^2$ noise, all devices appear to be dominated by $1/\sqrt{f}$ noise above certain frequencies. So far the physics behind this high frequency behavior is unclear and further investigation is needed to clarify this issue.

In the noise model, we included expressions for shot noise (white noise), flicker noise ($1/f$ noise) and RTN noise ($1/f^2$ noise) with the latter two dominating the low-frequency noise, and a simplified equivalent circuit is shown in Figure 3.4c. At the source/channel junction, shot noise originates from the discrete nature of electric charge, and is modeled by the expression $\overline{I_{n,\text{v/f}}} = 2qI_D$ in A$^2$/Hz. In parallel with this source there should exist the junction flicker noise source as previously described. Here we lump both $1/f$ sources in a single source in the gate as in the MOSFET, $\overline{V_{n,\text{v/f}}} = K/f^n$ in V$^2$/Hz, where $K$ is a constant and $n$ is a factor to account for the frequency dependence ($n = 1$ for $1/f$ noise, and $n = 2$ for RTN noise), both of which can be extracted from measurements or simulation data.

3.3 Implementation of model in SPICE

The model was implemented using Verilog-A language, an industry standard modeling language for analog circuits, with the help of Prof. Trond Ytterdal from the Norwegian University of Science and Technology. The Verilog-A implementation enables automatic translation into C code and fast simulation at run time in circuit simulators such as HSPICE. It has also been converted to C code offline and integrated
into native AIM-Spice simulator, which is available online at aimspice.com (Mac and Windows version), in the iTunes App store (iOS version) and also Google Play store (android version).

3.3.1 Discontinuity issues

Implementation of a SPICE model is more than translating equations into code. Because different equations are used to describe the current and charge in different operation regions, they can be connected by way of either a piece-wise model using if statements or utilizing limiting equations to limit the range of the equations. Piece-wise models are known to have discontinuity problems, because the discontinuity of model equations can result in non-convergence in circuit simulation [71]. Here we choose to use limiting equations to turn off the inactive components in each quadrant. For example, in the first quadrant, only the source/channel junction tunneling current is active and the ambipolar current and other diode current are inactive. To illustrate, $V_{GO} (= V_{GS} - V_{OFF})$ is replaced by the effective gate voltage as in

$$V_{GOE} = V_{MIN} \left(1 + \frac{V_{GO}}{2V_{MIN}} + \sqrt{DELTA^2 + \left(\frac{V_{GO}}{2V_{MIN}} - 1\right)^2}\right)$$

(1)

where $V_{MIN}$ and $DELTA$ are parameters. As $V_{GO}$ goes below $V_{MIN}$, $V_{GOE}$ approaches asymptotically $V_{MIN}$. The parameter $DELTA$ determines the width of the transition region. As obvious from Figure 3.5, $V_{MIN} = 1e-3$ and $DELTA = 5$ is a good choice, and can be modified as needed. Please note that when their values are set too small, it may appear that $V_{GOE}$ is discontinuous at $V_{GO}$ around 0. This form of equation is not only used in this model, it is also used extensively in the implementation of universal MOSFET models in AIM-spice [75].
Another change we made in the implementation of the source charge $Q_S$ relation. Due to the nonlinear $V_{DS}$ dependence as shown in Figure 3.6, the same equation but with two sets of different parameters is used to describe the two linear regions. In order to obtain a smooth transition between the two regions, we interpolate $Q_S$ as follows:

$$Q_S = \frac{1}{ \frac{1}{Q_{SP}^{MQS}} + \frac{1}{Q_{SN}^{MQS}} }$$

where $Q_{SP}$ and $Q_{SN}$ are $Q_S$ with $V_{DS} > 0$ and $V_{DS} < 0$, respectively. Parameter $MQS$ is a constant determining the width of the transition region between the two linear regions. It is used as a fitting parameter.
3.3.2 More on negative differential resistance

In the original version of the model, the NDR region (quadrant IV) is modeled by different equations from the normal tunneling region (quadrant I) and connected by equation (1), which caused convergence issues in the simulation of RF circuits, as discovered by Prof. Peter Asbeck from U.C. San Diego. His graduate student Jie Min realized that by multiplying the tunneling window, $V_{TW}$, by an empirical fitting equation with $V_{DS}$ dependence, the NDR region and the normal tunneling region can be modeled by a single equation, as shown in Figure 3.7, which fixed the convergence issues they
experienced in circuit simulations. Still, the diode current is not accounted for and needs
to be added to the tunneling current. The modified tunneling window is given by

\begin{align}
V_{TW}(V_{GS}, V_{DS}) &= V_{TW0}(V_{GS}) \left\{ \frac{1}{2} \left[ \tanh \left( \frac{V_{DS} - V_{D1}}{V_{D2}} \right) + 1 \right] \right\} \\
V_{TW0}(V_{GS}) &= U \ln \left( 1 + e^{(V_{GS} - V_{TH})/U} \right)
\end{align}

where $V_{D1}$ and $V_{D2}$ are fitting parameters.

Figure 3.7. Plot of (a) the $f$ factor which dominates the $I_D$-$V_{DS}$
characteristics, (b) tunneling window $V_{TW}$, and (c) $fV_{TW}$ versus $V_{DS}$.
Even though the newly added equation is not physics based, it has improved the convergence and simulation accuracy of RF circuits and circuits that operate near $V_{DS} = 0$ V. It also simplifies the model and reduces the amount of code in the Verilog-A implementation. Please note that this change is only included in the Verilog-A code, not in the recently published paper on the universal TFET SPICE model ([19] and Appendix E).

3.3.3 Fitting improvement in the superlinear onset region

The superlinear onset of TFETs is tricky to model accurately because the extent of the superlinear onset can vary considerably depending on the geometry of TFETs. The original formulation in the universal model [17, 18] (Appendices C and D) turned out inadequate for devices with severe superlinear onset, such as the GaN/InN/GaN TFET in [19] (Appendix E) and was modified as follows for better fitting in this region.

The drain tunneling current is modeled by

$$I_{DF} = afV_{TW} \xi \exp\left(-\frac{b}{\xi}\right)$$

in which the $f$ function is given by

$$f = \frac{1 - \exp\left(-\frac{V_{DSE}}{\Gamma}\right)}{1 + \exp\left(\frac{V_{THDS} - V_{DSE}}{\Gamma}\right)}.$$  \hspace{1cm} (5)

where $V_{THDS}$ is the drain threshold voltage, defined as

$$V_{THDS} = \lambda \tanh(\kappa_1 V_{GO} + \kappa_0)$$

and $\Gamma$, a saturation shape parameter, is modified from a constant to

$$\Gamma = \Gamma_1 V_{GO} + \Gamma_0$$

(7)

to improve the fitting of the output characteristics at low $V_{DS}$. Figure 3.8 shows that the
fitting of the superlinear onset of the side gate GaN/InN/GaN TFET improves significantly after the modification.

![Figure 3.8. Fitting of the model to TCAD data of the side gate GaN/InN/GaN TFET with (a) $\Gamma$ as a constant and (b) the new formula.](image)

3.4 Parameter extraction procedure

To extract all the fitting parameters in the model, the user needs to fit each of the four equation sets in the model, i.e., $I-V$ model, capacitance model, gate current model, and noise model, to device data (either from simulation or experiment) in each quadrant.
Here we only discuss the fitting of the $I$-$V$ model in the first quadrant. Fitting in other quadrants or models follows a similar methodology.

The table in [17] is repeated and updated below with newly added parameters. The fitting methodology used to select the parameters in the table is outlined as follows. First note that the parameters in the table can be grouped between physical (from $E_G$ to $t_{CH}$) and adjustable (from $V_{TH}$ to $\lambda$). It is straightforward to set the material parameters for a homojunction TFET. For a heterojunction TFET, the material parameters for the channel material may be the best first choice. The adjustable parameters are obtained by fitting within the ranges given in the table manually or using the Curve Fitting Toolbox in MATLAB.
### TABLE 3.2

SUMMARY AND RANGE OF PARAMETERS IN THE FIRST QUADRANT DC MODEL

<table>
<thead>
<tr>
<th>Category</th>
<th>Parameters</th>
<th>Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>Material parameters</td>
<td>$E_G$ (eV)</td>
<td>–</td>
</tr>
<tr>
<td></td>
<td>$m_R^*$</td>
<td>–</td>
</tr>
<tr>
<td></td>
<td>$t_{CH}$ (nm)</td>
<td>–</td>
</tr>
<tr>
<td>$V_{GS}$ dependence</td>
<td>$V_{TH}$ (V)</td>
<td>$0 - V_{DD}$</td>
</tr>
<tr>
<td></td>
<td>$V_{OFF}$ (V)</td>
<td>$0 - V_{DD}$</td>
</tr>
<tr>
<td></td>
<td>$\xi_0$ (MV/cm)</td>
<td>$0.5 - 5$</td>
</tr>
<tr>
<td></td>
<td>$\gamma_2$ (m$^{-1}$)</td>
<td>$0 - 2$</td>
</tr>
<tr>
<td></td>
<td>$n$</td>
<td>$&gt; 1$</td>
</tr>
<tr>
<td></td>
<td>$\gamma_0$</td>
<td>$0 - 1$</td>
</tr>
<tr>
<td>$V_{DS}$ dependence</td>
<td>$V_{D1}$ (V)</td>
<td>$0 - V_{DD}$</td>
</tr>
<tr>
<td></td>
<td>$V_{D2}$ (V)</td>
<td>$0 - V_{DD}$</td>
</tr>
<tr>
<td></td>
<td>$\gamma_1$ (m$^{-1}$)</td>
<td>$0 - 1$</td>
</tr>
<tr>
<td></td>
<td>$\Gamma_0$ (V)</td>
<td>$0 - 1$</td>
</tr>
<tr>
<td></td>
<td>$\Gamma_1$ (V)</td>
<td>$0 - 1$</td>
</tr>
<tr>
<td></td>
<td>$\lambda$ (V)</td>
<td>$0 - 1$</td>
</tr>
</tbody>
</table>

The fits can be obtained manually or an automated fitting procedure can be utilized. If a manual approach is taken, the selection of $V_{TH}$ is essential to a good overall fit. It can be set roughly in the middle of the knee region of the transfer characteristic and then fine-tuned as needed. The minimum valid gate-source voltage, $V_{OFF}$, can be found as the gate voltage where the drain current has its steepest slope point on the logarithmic scale.
The rest of the adjustable parameters can be further divided into 3 groups: in the above-threshold region, $\xi$ and $\gamma_2$; in the subthreshold region, $n$ and $\gamma O$; and the rest for the output characteristic. A good starting point for $\xi$, the internal field, is 1 MV/cm. Then $\gamma_2$ is adjusted to get the desired slope in the above-threshold region. The value of $\gamma_2$ is not limited to $0 - 1$, because the impact of the gate bias on the electric field is twofold. It increases the internal field by increasing the tunnel junction barrier and narrowing the barrier. For the subthreshold region, $\gamma O$ and $n$ are adjusted at the same time to get the slope right. Adjusting $\gamma O$ is effective for $V_{GS}$ less than $V_{TH}$, and adjusting $n$ will affect the transition region between the below and above threshold region too. For the output characteristic, the $\lambda$ parameter controls the superlinear current onset, $\Gamma_0$ and $\Gamma_1$ controls the range over which the drain current saturates with respect to the drain bias, and $\gamma_1$ sets how abruptly the drain current increases with drain bias once the current is saturated. Parameters $V_{D1}$ and $V_{D1}$ are primarily for the NDR region, but they also affect the superlinear onset in the first quadrant.

The manual fitting methodology described above can be automated using functions from the MATLAB Curve Fitting Toolbox [41]. To help the fitting process converge, a rough manual fitting is recommended to find the starting points. The fitting process is two-step, $I_D-V_{GS}$ fitting and $I_D-V_{DS}$ fitting. In the first step, all fitting parameters are evaluated by fitting the $I_D-V_{GS}$ curve at $V_{DD}$ within the range given in Table 3.2 (only two variables $V_{GS}$ and $I_D$, line fitting). Then the new values of all the fitted parameters are ported to the second fitting process as the new starting points. In the second step, parameters $V_{OFF}$, $n$, and $\gamma O$ are fixed and the rest of the fitting parameters are the new
fitting parameters. In this step, the family $I_D-V_{DS}$ curves are used to get a better overall fitting (three variables, $V_{DS}$, $V_{GS}$, and $I_D$, surface fitting). The fitting method is robust nonlinear least squares. The fitting works by minimizing the least absolute residuals (LAR). The Trust-Region algorithm is used for the fitting procedure. If fitting is not successful at first, parameters such as maximum number of model evaluations (MaxFunEvals) and maximum number of fit iterations allowed (MaxIter) can be adjusted to find a better solution. Tolerances such as TolFun (termination tolerance used on stopping conditions involving the function/model value) and TolX (termination tolerance used on stopping conditions involving the coefficients) can be increased to relax the constraints and find a better overall fitting. After the two-step fitting, the parameters should be optimized.

Parameter extraction in quadrant II-IV can be done in a similar way. The gate current model is modeled as a function of $V_{GD}$, and therefore the fitting process is straightforward. The fitting of the charge model is more complicated and requires separate fitting to the drain and source charge. If the source charge shows nonlinear dependence on $V_{DS}$, as seen in Figure 3.3, the two linear regions need to be fitted separately and then connected using the interpolation equation.
4.1 Conclusions

In this work, a 2D ionic memory is proposed that utilizes a graphene channel to sense the presence of Li ions to store information. The 2D memory requires a flat-lying molecule, CoCrPc, as the host for Li ions. I have demonstrated the deposition of a monolayer CoCrPc on both HOPG and graphene, which was published in the paper included in Appendix A. A simplified approach to the 2D memory was later proposed to explore the electric double layer. In collaboration with Ke Xu, we fabricated and tested the device. Programming tests show that the memory has two states through ion doping and the memory state can be switched via a back gate bias, even though the measured switching time is on the timescale of seconds. Faster switching might be possible by applying a pulse to the back gate with higher field. Retention tests show that the memory can hold its state for at least 30 minutes after the back gate bias is removed and that the ion relaxation process has a time constant of \( \sim 10^3 \) seconds, much larger than that of polymer electrolyte PEO (~1 ms). Even though the memory did not demonstrate subvolt operation, nanosecond program/erase speed, and 10 years of retention time, it was shown to have two stable states and could switch between the two states with speed on the scale of seconds and the states could be retained for at least 30 minutes. By scaling the back gate oxide to below 10 nm, subvolt operation and faster switching speed could potentially
be possible. To realize the nanosecond program/erase speed, a different device structure might be required because the gate does not have direct control over the 2D electrolyte in the current device geometry.

The second part of this thesis is the universal TFET SPICE model, which was proposed for circuit designers interested in low power TFET circuit design. The model is intended to be universal, physics based, easy to use, and supports automatic parameter extraction. The model was built by adding one component at a time, starting from the $I-V$ model, then the empirical charge model, the gate current model, and lastly the noise model. The model has been implemented in Verilog-A, which is supported by all major SPICE vendors, as well as in AIM-Spice. Fitting of the model can be done in Matlab by calling the fitting routine provided by the Curve Fitting Toolbox. The accomplishments on the model were published in three papers, as included in Appendices C-E.

4.2 Future work – 2D memory

A memory cell in an array is typically composed of two components – the storage node and the selector [30]. The storage node is usually an element with switchable states, and the selector allows the storage node to be selectively addressed for read and write. Both components impact the scaling limits of memory. Flash memory is a storage node (floating gate) and a selector (transistor) combined in one device. Emerging memories, as those shown in Figure 4.1, are mostly two-terminal devices and may require separate selectors.
Two-terminal memories typically utilize the crossbar geometry, because it achieves the highest possible 2D memory packing density and allows vertical stacking to form 3D memory array, as illustrated in Figure 4.2. Selectors are necessary to minimize leakage current through sneak paths (unselected paths). Selectors can be classified into two categories, three-terminal transistors and two-terminal non-transistors, which achieves the selector function through asymmetry (e.g., rectifying diodes) or nonlinearity (e.g., nonlinear devices) [30]. For crossbar memories, non-transistor based selectors are preferred because two-terminal memory selector devices can be stacked with the storage device vertically and are therefore preferred for scalability. Figure 4.3 illustrates how selectors can cut off the sneak paths in a crossbar RRAM memory array.
Figure 4.2. Sneak path in crossbar memory from Chen [76].

Figure 4.3. Current paths in crossbar RRAM memory array without and with selectors from Jo [77].
Selectors have to meet certain performance requirements determined by applications and array design specifications, as shown in the ITRS 2013 projections for selector device (Table 4.1) [77]. Key requirements of selectors include high selectivity, steep turn on slope, high current density, fast turn on and recovery, and high endurance [78]. Figure 4.4 shows the example $I-V$ curves of a storage node (RRAM), a field assisted superlinear threshold (FAST) selector, and the memory cell (storage node + selector). The selector shows a selectivity of $\sim 10^{10}$, turn on slope $< 5$ mV/decade, fast turn on and recovery ($< 50$ ns), $> 100$ M endurance and processing temperature less than 300°C [78]. The FAST selector device utilizes a superlinear threshold layer in which a conduction path is formed at the threshold electric field and provides bidirectional volatile switching. A 4MB 1S1R (1 selector + 1 RRAM) RRAM array was demonstrated with large memory on/off ratio and selectivity.
TABLE 4.1

SELECTOR DEVICE REQUIREMENTS FROM ITRS 2013 ERD (EMERGING RESEARCH DEVICES) [77] WHERE BEOL STANDS FOR BACK-END-OF-LINE

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Driver</th>
<th>Target value</th>
</tr>
</thead>
<tbody>
<tr>
<td>On/off ratio, or selectivity</td>
<td>To minimize sneak current</td>
<td>&gt; 106</td>
</tr>
<tr>
<td>On current, IR</td>
<td>Sufficient for memory switching Sensing of memory state (fast read)</td>
<td>&gt; 1 MA/cm²</td>
</tr>
<tr>
<td>Threshold voltage, VTH</td>
<td>Minimized to reduce power</td>
<td>0 V</td>
</tr>
<tr>
<td>Switching speed</td>
<td>As fast as memory element</td>
<td>&lt; tens of ns</td>
</tr>
<tr>
<td>Scalability</td>
<td>As good as memory element</td>
<td>–</td>
</tr>
<tr>
<td>Operating polarity</td>
<td>Compatible with memory element</td>
<td>–</td>
</tr>
<tr>
<td>Processing temperature</td>
<td>Compatible with BEOL</td>
<td>&lt; 400 °C</td>
</tr>
<tr>
<td>Operating temperature</td>
<td>The top end spec for servers</td>
<td>85 °C</td>
</tr>
<tr>
<td>Operating temperature</td>
<td>NAND spec (the very embodiment of nonvolatile memory for the current state-of-the-art)</td>
<td>50 °C</td>
</tr>
</tbody>
</table>

Figure 4.4. I-V curves of a storage node (RRAM), a selector node, and the integrated memory cell from Jo [77, 78].
However, 2D memory requires a 2D channel, which is flat lying and may not be suited for the crossbar geometry. Therefore a three-terminal transistor may be acceptable as the selector. Figure 4.5 shows a three-terminal design of a 2D selector device in the off and on state. It utilizes a solid polymer electrolyte, PEO, rather than the 2D electrolyte CoCrPc. A larger ion, Cs\(^+\), is used instead of Li\(^+\) to avoid Li\(^+\) intercalation in the channel. An oxide wall along the drain is necessary so that only cations cause doping. By applying a positive gate bias and drain bias, the cations migrate to the source terminal and tunnel junction forms at the source, turning the tunneling current on.

![Figure 4.5. Ion enhanced selectors. Band diagram and schematic of three-terminal selector device in (a) off and (b) on state, unpublished from Seabaugh.](image)

The main issue with this proposed memory is turn-on slope and switching speed. It relies on tunneling through the source Schottky barrier as the turn-on mechanism, which is unable to beat the 60 mV/decade turn-on slope at room temperature [79]. As
discussed in Section 2.3.3, there are two processes involved in the formation of EDL, a fast process (~ns) and a slow process (~s). Unless we can unlock the fast EDL forming mechanism, the switching speed of the device will remain a bottleneck.

4.3 Future work – universal TFET SPICE model

As the experiments on TFETs move on, SPICE models must keep evolving to keep up with the experimental development. Future improvements of the model can possibly include a physics based noise model, a physics based charge model, and possibly extension to 2D TFETs. Physics based models similar to the analytic model for double gate TFET in Taur [80] and the semianalytic model for double gate and nanowire TFET in Wu [81] are also possible future directions for the universal TFET model. However the integral in the drain current expression will consume substantial amount of computation time and may result in convergence issues during circuit simulation and therefore needs to be simplified or approximated before implementation in Verilog-A.

The simple noise model included now is based on well-known expressions for shot noise, flicker noise, and random telegraph noise due to limited noise measurement data available in literature. Voltage dependence such as $V_{DS}$ and $V_{GS}$ dependence is not included. As the experimental effort keeps pushing forward in the LEAST center, when more TFET noise data are available, a more sophisticated noise model should be developed and verified against experimental data.

Currently the charge model in the universal TFET SPICE model is based on empirical equations. It is flexible and can be fitted to a wide variety range of device structures. However, a physics based charge model is preferred because physics based
models are more accurate and allows prediction of the transistor behavior by changing
the physical parameters. It is worthwhile to note that physics based models may not share
the same flexibility as empirical or semiempirical models because as the transistor
geometry changes, the physical equations may need to be changed accordingly.

Though still at its infancy, theoretical prediction shows that 2D TFETs have the
potential to achieve similar on-current with 14 nm Intel FinFET but with steeper
subthreshold slope [82]. The current universal model is based on the tunneling process in
traditional TFETs such as III-V and Si TFETs. 2D TFETs, however, utilize different
device structures from their 3D counterparts because of they are atomically-thin and
utilize remote doping techniques. These structural difference leads to difference in
tunneling transport bias dependence, which is different from 3D TFETs [9]. Therefore,
the universal TFET SPICE model cannot be directly applied to 2D TFETs and a new
model will be needed in these systems.
REFERENCES


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APPENDIX A:

SOLUTION-CAST MONOLAYERS OF COBALT CROWN ETHER
PHTHALOCYANINE ON HIGHLY ORDERED PYROLYTIC GRAPHITE

Solution-Cast Monolayers of Cobalt Crown Ether Phthalocyanine on Highly Ordered Pyrolytic Graphite

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Supporting Information

ABSTRACT: 15-Crown-5-ether-substituted cobalt(II) phthalocyanine (CoCrPc) is an atomically thin and flat-laying, electrically insulating molecule that can solvate ions; these properties are desirable for nanoelectronic devices. A simple, solution-phase deposition method is demonstrated to produce a monolayer of CoCrPc on highly ordered pyrolytic graphite (HOPG). A uniform and continuous CoCrPc layer is obtained on freshly cleaved HOPG by solution drop casting, followed by thermal annealing under ambient pressure in Ar in the temperature range of 150–210 °C. While the quality of the monolayer is independent of annealing time, the composition of the annealing atmosphere is critical; exposure to ambient air degrades the quality of the monolayer over the time scale of minutes. Using ultrahigh vacuum scanning tunneling microscopy, a highly ordered and flat CoCrPc layer with hexagonal symmetry and average spacing of 4.09 ± 0.2 nm is observed. The band gap of the CoCrPc, measured by scanning tunneling spectroscopy, is 1.34 ± 0.07 eV. The ability to prepare uniform, ordered, and conformal monolayers of CoCrPc molecules on HOPG represents the first step toward using these materials to seed dielectric growth on 2D crystals and provide a 2D electrolyte for the electrostatic gating of semiconductors at the ultimate limit of scaling.

1. INTRODUCTION

Two-dimensional (2D) crystals, such as graphene, hexagonal boron nitride (h-BN), and transition metal dichalcogenides (TMDs), such as MoTe₂ and MoS₂, are potential candidates for future electronic devices, including TMD-based field-effect transistors (FETs) and tunnel FETs (TFETs). High performance transistors based on 2D crystals require thin and defect-free gate dielectrics. However, due to the absence of dangling bonds, 2D semiconductors are generally unreactive, thereby making the deposition of dielectrics on the surface of these materials challenging. One approach to address this problem is the deposition of a seed layer onto which a gate dielectric is deposited.

In addition to gate dielectrics, electronic devices based on 2D crystals also require doping methods. There are three common approaches to doping: substitutional, charge transfer, and electrostatic doping using either a metal gate or ions. Substitutional doping changes the optical band gap and can introduce defects that degrade electrical performance. Charge transfer dopants, which rely on molecular physisorption, including NO₂, SiN, K, and benzyl viologen, are currently being explored. Similar to metal gates, ionic liquids and solid polymer electrolytes do not involve charge transfer, but instead rely on electromechanical stress to induce image charge in the semiconductor. Electrolytes such as DEME-TFSI (N,N-diethyl-2-methoxy-N-methyllethaniminum), EMIM-TFSI (1-ethyl-3-methylimidazolium bis(trifluoromethylsulfonyl)imide), and poly(ethylene oxide) with LiClO₄ or CsClO₄ have been used extensively for reconfigurable doping of graphene and TMDs. For basic research and development purposes, ionic liquids and polymer electrolytes are easy to use and enable higher capacitance density than a conventional oxide gate dielectric. However, due to their poor scalability to nanometer thicknesses and incompatibility with conventional photolithography, liquid and polymer electrolytes are unsuitable for 2D devices at the limit of scaling. Therefore, a solid electrolyte that is both 2D and can be deposited layer-by-layer is highly desirable.

To address the needs for dielectric deposition and electrolyte doping of 2D crystals, a flat-lying and insulating molecule is needed that can be deposited conformally with monolayer precision and can solvate alkali cations, such as Li⁺. One such
class of molecules is crown-ether-substituted phthalocyanine (Pc). Among the various crown ether metal Pc (MPc) molecules that can be obtained via peripheral substitution, 15-crown-5-ether-substituted cobalt(II) phthalocyanine (CoCrPc), as shown in Figure 1, can solvate cations smaller than the cavity size of the crown ethers and can lay flat on the substrate.\textsuperscript{32,33} The metal atom of the MPc interacts strongly with the substrate,\textsuperscript{32,33} enabling the use of MPcs to seed atomic layer deposition (ALD) growth of high-κ dielectrics.\textsuperscript{32,33} When the MPc molecule is functionalized with crown ethers, such as CoCrPc, the molecule can solvate various alkali cations,\textsuperscript{30,36} providing a potential doping strategy for 2D crystals.

MPcs and their derivatives can be deposited in an ultrahigh vacuum (UHV) by molecular beam epitaxy (MBE) onto Au(111),\textsuperscript{37} graphene,\textsuperscript{38–40} and TMDs\textsuperscript{41} to form perfectly ordered monolayers. Because of their excellent film growth and electronic properties,\textsuperscript{41} an MPc monolayer can be used to nucleate ALD of wide band gap oxides, such as Al₂O₃.\textsuperscript{32,33} Although MBE deposition of MPcs allows for precise control of layer thickness for use as a crystalline multilayer, a monolayer of MPcs also can be prepared by simple solution phase deposition, which is more practical for commercial application compared to MBE, because solution deposition can be done at atmospheric pressure. For example, Kong et al. prepared a monolayer of TiO₆Pc by drop casting from solution (9:1 TiO₆Pc in toluene) onto freshly cleaved, highly ordered pyrolytic graphite (HOPG) and Au(111) under ambient conditions and performed scanning tunneling microscopy (STM) measurements.\textsuperscript{32} Their STM observations revealed that TiO₆Pc molecules form a hexagonally packed monolayer on both substrates.

Previously, Yoshimoto and co-workers prepared a CoCrPc monolayer on both Au(100) and (111) and characterized the surfaces with STM.\textsuperscript{32,33} The CoCrPc monolayer was formed by immersing the Au substrate for 5 min in a benzene–ethanol (9:1 v/v) solution saturated with CoCrPc, followed by an ultrapure water rinse. STM measurements of the CoCrPc, made in 0.05 M HClO₄, confirmed that the molecules form an ordered, flat-lying array parallel to the Au surface and the CoCrPc layer had 4-fold symmetry, with spacing of 2.5 nm.\textsuperscript{32} They also showed that the crown ether moieties of CoCrPc can trap Ca²⁺ by making molecule–ion pairs. The imaging was performed in solution, where solvent–CoCrPc interactions may help stabilize the CoCrPc and facilitate the formation of a monolayer. In addition, strong interactions between the Au substrate and the phthalocyanine molecules may help to promote monolayer formation more than phthalocyanine deposited on a graphene substrate.\textsuperscript{39}

In this report, the solution phase deposition of a CoCrPc monolayer on HOPG is presented. The monolayer was prepared by solution drop casting, followed by annealing in Ar at ambient pressure. Because both HOPG and graphene share the same surface chemistry, originating from sp² hybridization, it is reasonable to regard HOPG and graphene as equivalent for the purposes of this study. The solution deposition and annealing conditions were optimized by characterizing the surfaces with atomic force microscopy (AFM). Using UHV-STM, the surface morphology and the packing structure of the monolayer were observed at the molecular level, and scanning tunneling spectroscopy (STS) was used to directly probe the band gap of the monolayer.\textsuperscript{43}

2. EXPERIMENTAL DETAILS

CoCrPc was synthesized following a previously published procedure.\textsuperscript{35} Because the crown ether ligands make the molecule hygroscopic,\textsuperscript{34} monolayer deposition and AFM characterization were performed inside an Ar-filled glovebox (O₂ and water < 0.1 ppm) and anhydrous solvents were used. A total of 1.3 mg CoCrPc was dissolved in a 100 mL mixture of anhydrous benzene–ethanol (9:1 v/v, Sigma-Aldrich: 99.8% anhydrous benzene, 99.5% anhydrous ethanol). To improve CoCrPc dispersion in the solvent, the solution was enclosed in a glass vial with a screw-top lid, removed from the glovebox, and sonicated for 60 min at 40 kHz (Branson Sonicator 2510). The solution was returned to the glovebox for sample preparation.

CoCrPc monolayers were deposited onto HOPG by drop casting from solution followed by thermal annealing in an Ar-filled glovebox. The CoCrPc solution was deposited onto 1.2 × 1.2 cm pieces of HOPG (2 mm thick, ZYB grade, Bruker) using a micropipettor with a drop volume of 2.5 μL Scotch tape (3M) was used to cleave the HOPG. Subsequent drops were applied after the previous drop evaporated and the sample surface appeared dry. After drop casting, the sample was transferred onto a hot plate and annealed in the temperature range of 120–500°C in an Ar ambient. After 30 min of annealing, the samples were transferred through an airlock into the second bay of the glovebox for atomic force microscopy (AFM) measurements without air exposure.

To determine how the quality of the CoCrPc monolayer depends on air exposure, the solution was drop cast onto a freshly cleaved HOPG surface, dried in the glovebox, and then brought into air for annealing. The same sample was annealed on the hot plate at 150°C for 5, 10, 15, and 35 min, and after each annealing period, the sample was returned to the glovebox for AFM measurements.

The topography of a CoCrPc monolayer was characterized using AFM (Dimension Icon Scanning Probe Microscope, Bruker) in ScanAsyst/ParkForce Tapping mode with silicon nitride ScanAsyst-air probes (Bruker). During the characterization, the box light and glovebox circulation were turned off to minimize noise. Line profiles were used to measure the thickness of a CoCrPc monolayer on a sample prepared with partial surface coverage.

Monolayer formation of CoCrPc was confirmed by STM. After drop casting 2 drops on freshly cleaved HOPG, the sample was annealed in a N₂-filled convection oven (Carbolite 301) for 20 min at 180°C at ambient pressure. The sample was immediately loaded into an Omicron multichamber ultrahigh vacuum system with base pressure less than 1 × 10⁻¹⁰ Torr. The sample topography was observed with a VT-STM.
(Omicron Nanotechnology) with tungsten tips made by electrochemically etching a tungsten wire. All STM images were acquired in constant current mode ($I = 0.2 \text{nA}$) with a sample bias of $-1.8 \text{V}$. STS was used to measure the band gap of monolayer CoCrPc using a variable $z$-mode with external lock-in amplifier in the sample bias range from $-1.5$ to $1.5 \text{V}$. In addition, a bare HOPG surface was measured as a control.

3. RESULTS AND DISCUSSION


After drop casting and solvent evaporation, the annealing temperature was varied between 120 and 500 °C to determine the optimum temperature range for obtaining a CoCrPc monolayer. The annealing time was fixed at 30 min; however, the quality of the CoCrPc monolayer was insensitive to annealing time in the range of 5 to 60 min. A total of two $25 \mu\text{L}$ drops ($34 \mu\text{L/\text{cm}}^2$) provide full coverage on a $1.44 \text{cm}^2$ HOPG surface. AFM images of the CoCrPc, as deposited on HOPG and after 30 min of annealing at five temperatures between 120−220 °C, are shown in Figure 2. Large particles line the step edges of the HOPG and are scattered randomly on the mesas. The lateral particle size and height vary between 10−100 nm and 1−10 nm, respectively. The particles are either impurities or undissolved CoCrPc aggregates; it is more likely that the particles are aggregates because their size and density decrease with annealing temperature.

The as-deposited film (Figure 2a) shows uneven coverage of CoCrPc. After annealing at 120 °C, full coverage is not achieved (Figure 2b); however, the CoCrPc thickness is at least one monolayer, as shown by line scans in Figure S2 with step heights of ∼0.5 nm. Note that the shape of the large particles changes from irregular to spherical after annealing at 120 °C. Annealing in the temperature range of 150−210 °C (Figure 2c−e) yields nearly complete CoCrPc coverage on the mesas as the CoCrPc film becomes continuous and uniform. The continuity of the CoCrPc film is broken along the mesa edges and near the particles. The dose of CoCrPc was optimized to provide the minimum amount of material required to cover the area of the HOPG substrate without observable CoCrPc vacancy islands (i.e., a single monolayer). When the dose of CoCrPc is insufficient to cover the entire area of the HOPG substrate, discontinuous islands are formed with veins joining them. Figure 3 represents an extreme case for which the dose is...
so small that isolated CoCrPc patches are formed. When the dose of CoCrPc exceeds that needed for a single monolayer, a second layer of islands start to form, nucleating primarily at the step edges of the HOPG substrate. When the annealing temperature increases beyond $210^\circ$C, the upper bound of the optimal annealing temperature window is reached, and the quality of the CoCrPc film starts to deteriorate (Figure 2f).

To measure the thickness of a single CoCrPc layer after 150 °C anneal, 12 μL of CoCrPc solution (8 μL/cm$^2$) was used to intentionally provide incomplete coverage (Figure 3a). The thickness of the layer, 0.46 ± 0.01 nm is quantified by averaging 10 line scan over a large CoCrPc island (Figure 3b). This agrees with the thickness of an individual CoCrPc molecule measured by STM (0.42 nm),$^{33}$ indicating that the CoCrPc molecules lie flat on the HOPG surface. The line scan also indicates that the CoCrPc forms a uniform monolayer over the distance of the line scan.

Within the annealing window of 150–210 °C, the quality of the coverage and the layer thickness are insensitive to temperature. However, as mentioned above, at an annealing temperature of 220 °C, the CoCrPc monolayer becomes inhomogeneous. The monolayer continues to degrade with increasing temperature, as shown by the AFM scans in Figure 4, where the annealing temperature is varied from 230 to 500 °C. Specifically, the presence of large, nonspherical aggregates is observed at $T \geq 300^\circ$C. It is expected that the ether bonds in the crowns of the CoCrPc decompose at $T > 300^\circ$C, further contributing to the significant change in the surface morphology at $T = 500^\circ$C.

The surface roughness is quantified as a function of temperature in Figure 5a by averaging over five area scans of size 0.3 × 0.3 μm$^2$. At temperatures below 210 °C, the surface roughness decreases with increasing annealing temperature by a factor of ∼4; however, at temperatures larger than 240 °C, surface roughness increases by a factor of ∼6 as the CoCrPc

Figure 4. AFM images of degrading CoCrPc monolayer on HOPG. The CoCrPc monolayer was prepared by drop casting 34 μL/cm$^2$ of 13 mg/L CoCrPc benzene–ethanol (9:1 v/v) and (a) annealed in Ar for 30 min at 230, (b) 240, (c) 300, and (d) 500 °C. All images are 2 × 2 μm$^2$. A line scan of (d) is shown in Figure S3 in the Supporting Information.

Figure 5. Statistical analysis of as-deposited and annealed CoCrPc from AFM scans in Figures 2 and 4. (a) Root mean squared roughness ($R_q$) of bare HOPG and as-deposited and annealed CoCrPc within the temperature range of 120–500 °C ($n \leq 5$). The roughness data is taken on the mesa where a continuous CoCrPc monolayer is formed. (b) Particle height, (c) area, and (d) diameter of CoCrPc annealed within the temperature range of 120–300 °C. All errors are standard errors.
molecules rearrange and aggregate. It is possible that the CoCrPc molecules are partially desorbing from the surface at $T \geq 240^\circ C$, contributing to the increased surface roughness. In addition to surface roughness, the height, area, and diameter of the spherical particles observed at $T \leq 300^\circ C$ are quantified in Figure 5 by averaging over all particles in the AFM images in Figures 2 and 4. Generally, the size of the spherical particles decreases with increasing temperature. At higher temperatures, the molecules acquire sufficient thermal energy to aggregate significantly larger than the size of the original aggregates observed at $T \leq 300^\circ C$. The scan at $500^\circ C$ is excluded from the analysis because at such high temperatures, the molecules acquire sufficient thermal energy to aggregate into non-spherical clusters that are significantly larger than the size of the original aggregates.

3.2. Effect of Air Exposure. To characterize the stability of the CoCrPc films in air, samples were prepared in Ar by drop casting without annealing, then transferred from the glovebox and annealed in air at 150 $^\circ C$ for varying amounts of time. As shown in Figure 7, the quality of the CoCrPc monolayer significantly degrades compared to samples prepared under Ar atmosphere.

Figure 6: AFM images of CoCrPc monolayer after air anneal. A thin CoCrPc film was prepared on HOPG by drop casting 34 $\mu$L/cm$^2$ of 13 mg/L CCP benzene–ethanol (9:1 v/v) solution and (a) annealed in air at 150 $^\circ C$, (b) an additional 5 min, (c) an additional 15 min, and (d) an additional 20 min. The total annealing time is 5, 10, 15, and 35 min. (e) Line scan following the yellow line in image (b), and (f) line scan following the yellow line in image (d). All AFM images are 2 $\times$ 2 $\mu$m$^2$.

Figure 7: Statistical analysis of particle density and size observed in Figure 6 as a function of annealing time in air: (a) particle density, (b) height, (c) area, and (d) diameter of CoCrPc annealed in air at 150 $^\circ C$. All errors are standard errors.
annealing. The morphology of the CoCrPc monolayer changes dramatically when the annealing time increases from 5−10 min to 15−35 min. Because of the morphological similarity of the images before 10 min and after, Figure 5a and b are denoted as annealing stage 1, and Figure 5c and d are denoted as annealing stage 2. In annealing stage 1, instead of forming a continuous monolayer, the CoCrPc molecules form clusters, some of which have small spacing, ∼10 nm, and some large spacing, ∼50−100 nm. In annealing stage 2, the CoCrPc clusters form a film that is more continuous, but rough. As a result, large areas (−0.5 µm) with less CoCrPc coverage are created. As shown in the line scans in Figure 6e and f, the thickness of CoCrPc film is measured as 0.46 ± 0.03 nm (stage 1) and 0.46 ± 0.12 nm (stage 2) by averaging five line scans. The standard error of the measured thickness of CoCrPc film annealed in air is 3 to 12 times larger than those annealed in Ar, further indicating that the quality of the monolayer has degraded.

The size and density of the spherical particles also change significantly upon exposure to air while annealing. Based on the AFM scans in Figure 6, the particle density, height, area and diameter are quantified in Figure 7 by averaging over all particles in Figure 6a−d. The particle density decreases by a factor of 2 between annealing stage 1 and stage 2. In addition, the particles in annealing stage 2 are smaller in height, area, and diameter than those in annealing stage 1. Even when a sample is deposited and annealed in the glovebox, postannealing air exposure at room temperature will degrade the quality of the CoCrPc monolayer (Figure S4 in Supporting Information), consistent with metal phthalocyanines ability of bond oxidizing molecules.45

3.3. STM and STS. UHV STM was employed to confirm that CoCrPc lies flat on HOPG. As mentioned above, a flat-lying CoCrPc molecule is required for both seeding ALD growth of high-κ gate dielectrics and electrostatic doping via ions located in the crowns. Using the same method as described in the above AFM studies, 2 drops of 10 mg/L CoCrPc in anhydrous benzene−ethanol (9:1 v/v) were drop cast onto freshly cleaved HOPG and annealed in 1 atm of N2 at 180 °C for 20 min. Note that the samples were transferred in air to the STM and outgassed in UHV at 3 × 10−10 Torr for 10 min. In addition, a bare HOPG surface was measured as a control. Figure 8a shows a topographic STM image of bare HOPG with lattice parameters $a = 0.22 \pm 0.07 \text{nm}$, $b = 0.21 \pm 0.1 \text{nm}$, and $\alpha = 58 \pm 2^\circ$. STM was measured with $V_{\text{sample}} = -1.8 \text{V}$ and $I_t = 0.2 \text{nA}$ at $-180 \text{°C}$. (b) STS $dI/dV/(I/V)$ spectra (average of 20 measurements) of a bare HOPG sample showing no apparent energy gap. (c) Filled-state STM image of a CoCrPc monolayer on HOPG with lattice parameters $a = b = 4.08 \pm 0.2 \text{nm}$, $\alpha = 59 \pm 1^\circ$. A highly ordered and flat CoCrPc layer with hexagonal lattice structure is observed. (d) STS $dI/dV/(I/V)$ spectra of a CoCrPc layer on HOPG. STS curve shows that the CoCrPc layer has a 1.34 ± 0.07 eV band gap. $E_F$ is the position of Fermi energy level, located at 0 V.
observed. Figure 8c is a STM image of a solution casted CoCrPc layer on HOPG, where a highly ordered and flat CoCrPc layer is observed with hexagonal symmetry. This packing arrangement is different from the quadratic packing geometry of CoCrPc deposited on Au(100) and (111), consistent with the substrate controlling the packing geometry of MPC molecules. However, in contrast to CoCrPc, TiOPc packs hexagonally on both HOPG and Au(111) substrates are similar: $a = b = 1.3 \pm 0.1$ nm, $a = 60 \pm 1^\circ$; and $a = b = 1.0 \pm 0.2$ nm, $a = 60 \pm 2^\circ$, respectively. In the present study, the unit cell length of CoCrPc on HOPG is significantly larger, $a = b = 4.08 \pm 0.2$ nm, $a = 59 \pm 1^\circ$, than TiOPc on HOPG. This is due, in part, to the larger size of CoCrPc; however, the CoCrPc linear is also larger than the previously reported spacing of CoCrPc on Au(111), 2.5 nm. The lower packing density of CoCrPc on HOPG compared to Au(111) is attributed to weaker binding of CoCrPc and HOPG due to the lower electron density of HOPG compared to Au. In contrast, the negligible spacing change for TiOPc on both HOPG and Au is likely the consequence of a much stronger molecule-substrate binding interaction due to the large dipole of TiOPc.

Using STS, the normalized differential conductivity ($dI/dV/(I/V)$) of the bare HOPG and CoCrPc layer are measured as a function of scan voltage ($V$), as shown in Figures 8b and d. For the sample covered in CoCrPc, the STS data were measured on the center of the CoCrPc molecules. The scan bias was swept from $-1.5$ to $1.5$ V. A total of 20 STS curves were obtained from different points and averaged to estimate the band gap. The $dI/dV/(I/V)$ curve obtained on the bare HOPG surface is shown in Figure 8b. The curve has a parabolic shape, indicating there is no apparent energy gap due to the high conductivity of the HOPG sample. In contrast, the energy band gap is clearly observed in the sample covered by CoCrPc (Figure 8d). The locations of the valence-band maximum ($E_v$) and conduction-band minimum ($E_c$) are determined by assuming linear onsets in the differential conductance in Figure 8d. Straight lines are drawn through the spectra on either side of an onset, and the band edge onset position is obtained by the intersection of the lines and horizontal axis. The data indicate a valence band edge (left) and conduction band edge (right) at $-0.58 \pm 0.04$ and $0.76 \pm 0.03$ eV, respectively, giving a band gap of $1.34 \pm 0.07$ eV.

To our knowledge, this is the first reported measurement of the band gap of CoCrPc with STS. This small band gap is similar to previously reported values for other metal phthalocyanines on an HOPG substrate. For example, Park et al. reported a band gap of 1.75 eV for single layer copper phthalocyanine (CuPc) on HOPG. They also show that the band gap depends on the number of layers: multilayer CuPc film has a band gap of 2.3 eV. The fact that the STS measurements in Figure 8d are uniform across the entire scan area also supports the assertion that the CoCrPc coverage is a single monolayer.

4. CONCLUSION
A monolayer of CoCrPc was deposited on HOPG by simple drop casting from solution followed by thermal annealing in Ar under ambient pressure. The effects of annealing temperature and air exposure on the CoCrPc layer were characterized. A uniform and continuous film was obtained by Ar annealing in the temperature range of 150–210 °C, nearly independent of annealing time. However, the quality and coverage of the CoCrPc layer was observed over time by air annealing, and when the sample was exposed to air after argon annealing. Therefore, an inert environment is needed to maintain the quality of the monolayer on HOPG. STS shows that the CoCrPc monolayer lays flat on the HOPG surface with hexagonal symmetry, and for the first time, the band gap of the CoCrPc monolayer was measured by STS. This study lays the groundwork for using a monolayer of CoCrPc molecules in nanoelectronic devices as an ion conductor or as a seeding layer for ALD growth on 2D crystals. When complexed with alkali cations, the CoCrPc molecules could be used as a 2D electrolyte for electrostatic doping or memory in 2D crystals.

ASSOCIATED CONTENT

Supporting Information
The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acs.jpcc.5b05233.

Line scans of as-deposited CoCrPc and annealed at 120 °C; line scans and roughness of bare HOPG, and CoCrPc annealed at 150 and 500 °C; AFM of Ar-annealed CoCrPc after 15 min and 48 h of air exposure (PDF)

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Notes
The authors declare no competing financial interest.

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2


A.1 Supporting information for solution-cast monolayers of cobalt crown ether phthalocyanine on highly ordered pyrolytic graphite

Additional atomic force microscopy (AFM) images and line profiles are provided for cobalt crown ether phthalocyanine (CoCrPc) films deposited on highly ordered pyrolytic graphite (HOPG).

Figure A.1 shows the measurements of as-deposited CoCrPc single and bilayers on HOPG. Line scans indicate a single layer thickness of approximately 0.5 nm and a bilayer thickness of 1 nm.

Figure A.2 shows the same film after Ar annealing at 120 °C for 30 minutes. The line scan indicates the CoCrPc thickness is ~0.5 nm, which is on the order of one monolayer.

Figure A.3 shows AFM images and line scans of bare HOPG and CoCrPc on HOPG annealed at 150 and 500 °C for 30 minutes in Ar. The surface roughness, calculated by averaging over 5 area scans with size 0.3 × 0.3 μm², is 0.0435 ± 0.0003, 0.1015 ± 0.0016, 0.4510 ± 0.0087 nm, respectively. The line scans and surface roughness indicate that the surface of the CoCrPc monolayer is more rough than that of bare HOPG, and that the surface roughness at $T = 500$ °C increases dramatically as the CoCrPc molecules rearrange and aggregate.

Figure A.4 shows AFM images and line scans of Ar-annealed CoCrPc after air exposure for 15 minutes and for 48 hours at room temperature. The surface morphology of CoCrPc starts to degrade after being exposed to air for 15 minutes. The degradation becomes significant after 48 hours air exposure, indicating that the quality of CoCrPc monolayer is sensitive to the ambient environment.
Figure A. 1. AFM image (a) and line scans (b) of as-deposited CoCrPc in an Ar ambient. CoCrPc is prepared by drop casting 34 μL/cm^2 of 13 mg/L CoCrPc benzene-ethanol (9:1 v/v) solution on HOPG. Following the orange line, the thickness of a CoCrPc monolayer is represented by the step height change of ~0.5 nm. Following the blue line, the larger step height change represents the thickness a CoCrPc double layer, which is ~1 nm. Image size is 2 × 2 μm^2.
Figure A. 2. AFM image (a) and line scans (b) of CoCrPc annealed at 120 °C in Ar. CoCrPc is prepared by drop casting 34 μL/cm² 13 mg/L CoCrPc benzene-ethanol (9:1 v/v) solution on HOPG. Image size is 2 × 2 μm².
Figure A. 3. AFM images of (a) HOPG, (b) CoCrPc annealed at 150 °C, and (c) CoCrPc annealed at 500 °C. The CoCrPc monolayer in (b) and (c) is prepared by drop casting 34 μL/cm² 13 mg/L CoCrPc benzene-ethanol (9:1 v/v) solution on HOPG and annealed in Ar for 30 minutes. All images are 2 × 2 μm². (d) Line scans corresponding to the yellow lines in (a-c).

Figure A. 4. AFM images of a CoCrPc monolayer on HOPG prepared by drop casting 34 μL/cm² 13 mg/L CoCrPc benzene-ethanol (9:1 v/v) solution and (a) annealing in Ar at 180 °C for 30 minutes, (b) after 15 minutes air exposure at room temperature, and (c) 48 hours air exposure at room temperature. All images are 2 × 2 μm².
APPENDIX B:

TUNNEL FIELD-EFFECT TRANSISTORS: STATE-OF-THE-ART

Tunnel Field-Effect Transistors: State-of-the-Art

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ABSTRACT
Progress in the development of tunnel field-effect transistors (TFETs) is reviewed by comparing experimental results and theoretical predictions against 16-nm FinFET CMOS technology. Experiments lag the projections, but sub-threshold swings less than 60 mV/decade are now reported in 14 TFETs. The lowest measured sub-threshold swings approaches 20 mV/decade, however, the measurements at these lowest values are not based on many points. The highest current at which sub-threshold swing below 60 mV/decade is observed is in the range 1–10 nA/µm. A common approach to TFET characterization is proposed to facilitate future comparisons.

INDEX TERMS
Band-to-band tunneling, sub-threshold swing, TFET, tunnel field-effect transistor, tunneling.

I. INTRODUCTION
TUNNEL field-effect transistors (TFETs) use electric-field control of band-to-band tunneling as the current gating mechanism [1], [2]. These transistors have emerged as leading contenders to outperform CMOS at low voltages [3], [4]. This stems from the ability of the TFET to achieve a sub-threshold swing (SS) of less than 60 mV/decade at room temperature. Lower subthreshold swing enables a reduction in voltage supply and a path to lower system power.

In this rapidly advancing field, quantitative comparisons are needed to gauge progress and shed light on the current state-of-the-art. This paper updates comparisons provided in [1] with special attention given to the measured transistor reports of SS below 60 mV/decade. In addition, two-dimensional (2-D) crystal technology [5] based on the monolayer transition-metal dichalcogenides (MX₂) [6], [7] and ultra-thin topological insulators such as Bi₂Se₃ [8] is now included in the simulation comparison along with the recently-proposed resonant TFET [9].

II. CURRENT STATUS OF TUNNEL FETS
Fig. 1 shows the projected n- and p-channel TFET drain current per unit width \( I_D/W \) versus gate-to-source bias \( V_{GS} \), for a given drain-to-source bias \( V_{DS} \), against 16-nm low-power FinFET CMOS (gate length 34 nm) [10]. For the purpose of comparison, the current-voltage (\( I_D-V_{GS} \)) characteristics are shifted horizontally so that the gate voltage where the sub-threshold slope is the steepest is at the origin, which can be experimentally achieved by engineering the work function of the gate metal.

The general trends of Fig. 1 have already been discussed [1]. Group IV materials such as Si [11], [12] and Ge [12]–[14] exhibit smaller ON-currents resulting from their indirect band gaps and lower tunneling probability. Group III-V materials like InGaAs [3], InAs [15], [16], and InSb [17] have higher ON-currents due to their narrower and direct band gaps. The use of staggered and broken-gap heterojunctions, such as AlGaSb/InAs [18] and InAs/GaSb [9], boosts the ON-current by shortening the tunneling distances. The introduction of resonant tunneling into TFETs pushes the SS down to \( \sim 25 \) mV/decade by sharpening the tunneling window [9].

While III-V materials can provide high performance n-channel TFETs, the performance of p-channel devices is limited by the low conduction-band density-of-states [14], [19], [20]. For both n- and p-channel TFETs, graphene nanoribbons (GNR) [21] and monolayer MX₂ [6] with sufficient doping produce some of the best predicted TFET performances due to the high electrostatic gate control expected in single-atomic layer materials. Complementary n- and p-type configurations are available for graphene nanoribbons [21], monolayer TMD [22], and layered TMD heterostructure [7]. Carbon nanotube (CNT) n-TFETs, free from edge effects, provide the highest currents at the limits of scaling [23], [24]. MX₂ nanotubes are also a natural structure to minimize edges at the limits of scaling.
Fig. 1. Comparison of projected TFET drain current per unit width versus gate-to-source voltage for p-channel (left) and n-channel (right) transistors published since 2010. Dashed lines indicate experimental 16-nm low-power FinFET CMOS technology [10]. The curves are shifted so that the gate voltage where the steepest sub-threshold slope occurs is at the origin. The numbers indicate the drain-to-source voltage. Legends are listed in order of magnitude of currents from top to bottom. Notations in the figure include DG for double gate, GAA for gate-all-around, HJ for heterojunction, NT for nanotube, NW for nanowire, R-TFET for resonant-TFET, s for strained, SG for single gate, and in-line meaning gate electric field and tunnel-junction field point in the same direction. The I-V curve of p-type MoS$_2$/ZrS$_2$ DG TFET is calculated using the same methodology in [7].

The transfer characteristics for the best experimentally demonstrated TFETs are shown in Fig. 2. Best is defined as those devices that report a subthreshold swing near or below 60 mV/decade, or transistors in which both negative differential resistance is observed in the source-channel junction and where data is provided at supply voltages of 0.5 V or below. Using the later criteria, representative devices are selected across materials systems. As in Fig. 1, the $I_D$-$V_{GS}$ curves are shifted horizontally to allow easier comparison.

Consistent with theoretical predictions, experimental Si TFETs [25]–[30] generally display lower ON-currents. The use of strain engineering [31], and integration with Ge [32], and InAs nanowire [33], [34] improves the current. Other group IV materials such as strained Ge [35], GeSn [36], and strained SiGe [37] enhance the tunnel current; the GeSn [36] TFET does not show negative differential resistance (NDR) in the forward-biased tunnel junction, but is included as a best result for this material system. Homojunction III-V TFETs such as InGaAs [38], [39] and InAs [40] show higher ON-currents. The heterojunction III-V nanowire TFET based on InP/GaAs [41] shows a subthreshold swing at drain currents below 10 pA/µm. The heterojunction III-V TFETs like InGaAs/GaAsSb [42], [43], InAs/GaSb [44], InAsSb/GaSb [45], AlGaSb/InAs [20], [46], and In$_{0.53}$Ga$_{0.47}$As/In$_{0.7}$Ga$_{0.3}$As [47] have achieved the highest ON-currents thus far, however these also show the worst subthreshold swings. There does not appear to be a fundamental limitation in these systems to achieving subthermal swings and these numbers can be expected to improve with gate stack optimization, better electrostatics with self alignment, and better passivation. The carbon nanotube TFETs [48], [49] demonstrated to date do not show the high drive current predicted in [23], [24], but these transistors do not have optimized geometries.

The measured subthreshold swing versus $I_D/W$ for all n- and p-channel transistors (excluding two CNT TFETs [48], [49]) is shown in Fig. 3; there are 14 reports of SS below 60 mV/decade. These devices are taken from Fig. 2. The majority of these devices are group IV materials, such as Si [26]–[31], Si/Ge [32], strained SiGe [37], and strained Ge [35]. The InGaAs homojunction TFET [39] has exhibited a minimum subthreshold swing of 64 mV/decade at approximately 100 pA/µm drain current, while a subthreshold swing of 58 mV/decade at 1 nA/µm drain current has been obtained in an In$_{0.53}$Ga$_{0.47}$As/In$_{0.7}$Ga$_{0.3}$As heterojunction TFET [47]. Nanowire III-V TFETs have shown even lower subthreshold swing: 30 mV/decade at 1 pA/µm in an InP/GaAs heterojunction [41], and approximately 20 mV/decade in a Si/InAs heterojunction [33]. This 20 mV/decade finding is the lowest among all TFET reports.
and spans over three orders of magnitude of drain current. However, as Fig. 3 shows, there are only a few data points 
defining this result and this is the case in most of the 14 
reports of sub-60-mV/decade swing. The most stable and 
substantial measurements showing sub-60-mV/decade swing 
are given for Si in [26], [29], [31] and for InGaAs in [47]. 
The current range for subthreshold swing to be useful is so 
far insufficient for device applications. For TFETs to be suit-
able for low power applications, subthreshold swing should 
remain less than 60 mV/decade for current levels extending 
to 1-10 µA/µm as discussed in [50].

The comparison plot in Fig. 3 is particularly useful in 
evaluating progress in TFET development. Therefore, we 
recommend that both simulation and experimental studies 
make a practice of providing this data in future publications. 
The plot clearly displays the minimum SS, the highest current 
at which 60 mV/decade is achieved [50], and the range over 
which SS below 60 mV/decade is obtained.

III. BRIDGING THE GAP BETWEEN EXPERIMENTS AND 
SIMULATIONS
Comparing Figs. 1 and 2, it is apparent that there exists a 
large gap between theoretical projections and experiments. 
So far, no one has demonstrated a tunnel FET that has simul-
taneously both an ON-current comparable to CMOS and a 
subthreshold swing of less than 60 mV/decade. The highest 
current for which a subthreshold swing of 60 mV/decade is 
observed is approximately 1 nA/µm [47]. Generally, 
ON-current predictions are in reasonable agreement with 
theory. The greatest disparity has been in measured vs. sim-
ulated subthreshold characteristics. The reasons for this are 
that simulations shown in Fig. 1 generally neglect nonide-
alities that contribute to larger SS such as band tails due to 
phonons and heavy-doping, defect-assisted tunneling, inter-
face roughness, and interface and border traps at the high-k 
dielectric/semiconductor interface [51].

The theoretical treatment of these effects is at an early 
stage, and proceeding in advance of detailed characterization 
of TFETs. Close coupling with experiments is needed to 
understand the limits. Interface traps act as stepping-stones 
for electron tunneling though the gap. These traps both add 
current and perturb the device electrostatics [52], [53]. Band 
tails are density-of-states tails that extend exponentially into 
the band gap, and caused by phonons, thickness and interface 
fluctuations, substitutional and geometrical impurity disor-
der due to high doping and alloys [54], [55]. Band tails 
degrade device performance in the subthreshold region [55], 
and place a fundamental limit on subthreshold swing [54].

IV. 2-D-CRYSTAL TFETS
Although still at an early stage, 2D crystals have attributes 
of interest for TFETs [5] and open up an application
space outside of CMOS for light weight and flexible electronics. As already shown in Fig. 1, TFETs with graphene nanoribbons and MoTe$_2$ promise an ON-current close to 1 mA/um because of their light effective mass, small and direct bandgap, and excellent gate control owing to the ultrathin body. In atomically-flat single-layer 2D crystals, thickness fluctuations are eliminated, leading to sharper band edges [56]. Substitutional doping in bulk crystals is limited by the solid solubility to concentrations of approximately $10^{20}$/cm$^3$. These doping limits then set limits on internal electric field in the range of 2-4 MV/cm. In 2D crystals, doping is achieved by charge transfer or electrostatic doping from adjacent layers or plates, which means higher doping densities can be achieved with higher internal fields, and higher currents. Further tunneling enhancements can be anticipated with staggered or broken gap heterojunction alignments [57] and layered heterostructures TFETs [7]. At the limits of scaling, these 2D crystals can be formed into tubes for optimized electrostatics [58] without the complication of edges.

**V. CONCLUSION**

A comprehensive review of the state-of-the-art in tunnel field-effect transistors has been prepared to allow a clear assessment of current progress. This study shows the importance of more extensive characterizations of the subthreshold region in future simulations and measurements.

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APPENDIX C:

CONTINUOUS SEMIEMPIRICAL MODEL FOR THE CURRENT–VOLTAGE CHARACTERISTICS OF TUNNEL FETS

Continuous Semiempirical Model for the Current–Voltage Characteristics of Tunnel FETs

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Abstract—A simple analytic model based on the Kane-Sze formula is proposed to describe the current-voltage characteristics of tunnel field-effect transistors (TFETs). This model captures the unique features of the TFET including the decrease in subthreshold swing with drain current and the superlinear onset of the output characteristic. The model has fairly general validity and is not specific to a particular TFET geometry. Good agreement is shown with published atomistic simulations of an InAs double-gate TFET with gate perpendicular to the tunnel junction and with numerical simulations of a broken-gap AlGaSb/InAs TFET with gate in parallel with the tunnel junction.

Keywords—Band-to-band tunneling, compact model, tunnel field-effect transistor (TFET), tunneling.

I. INTRODUCTION

Tunnel field-effect transistors (TFETs) are candidates to compete with CMOS at low voltages because of their capability to achieve a subthreshold swing (SS) of less than 60 mV/decade at room temperature [1, 2]. To build TFET circuits and make performance projections, it is of interest to develop simple, closed-form expressions that contain the basic physics of the tunneling process and can be implemented in circuit simulators, e.g. SPICE.

Quite a few compact analytic models for the TFET have been developed [3-13]. References [3-8] employ a semi-analytical solution of Poisson’s equation in the channel region to model the channel charge [3] or to obtain the current-voltage characteristics [4-8]. These reports focus on particular TFET gate configurations, or on specific aspects of the transport. In most cases, the resulting expressions for the drain current are complex because the aim is to be predictive. The closest approach to our paper is that of Hong [13] where the motivation is to develop an analytic model for use in circuit modeling. The resulting model gives good representation of the TFET characteristics, but is discontinuous and lacks an intuitive connection to the device physics.

Our intent has been to provide a simple, continuous, and large-signal equation set to describe the TFET current-voltage characteristics. The resulting model produces the current-voltage characteristics of the TFET at the level of an elementary MOSFET SPICE model. This model is shown to capture the essential features of the TFET predicted by very comprehensive numerical simulators. The formulation does not rely on any specific TFET embodiment and is widely configurable.

The paper is organized as follows. Section II outlines the physics of the subthreshold and above-threshold regions and shows how these regions are connected. In Section III, the model is applied to the representation of a homojunction InAs double gate p-i-n TFET and a broken-gap AlGaSb/InAs vertical TFET.

II. MODEL DEVELOPMENT

Tunnel FETs utilize an MOS-gate to control the band-to-band tunneling across a degenerate p-n junction, as shown in Fig. 1. The device is normally off. When zero bias is applied to the gate, the conduction band minimum of the channel is located above the valence band maximum of the source, so band-to-band tunneling is suppressed and the tunneling window is significantly minimized for electrons in the source. The tunneling window opens up as the channel conduction band is shifted below the source valence band. Then electrons in the valence band with energy in this tunneling window, $qV_{TW}$, tunnel into empty states in the channel and the transistor is on.

As an overview of the modeling approach, the central portion of the TFET model utilizes an experimentally well-established expression for band-to-band, Zener tunneling in p-n junctions [14, 15], the primary transport mechanism in tunnel transistors [1, 16]. The two terminal Zener tunneling behavior is then generalized to three terminals by introducing physics-based expressions for the bias-dependent tunneling window and a dimensionless factor which accounts for the superlinear current onset in the output characteristic.

The signature feature of the TFET is the decrease in subthreshold swing with decreasing drain current, which is well established in both simulations [15, 17] and experiments [18, 19]. The model assumes that this behavior is caused by the exponential band tails that arise from imperfections and lattice disorder due to impurities,
where the symbols are defined as follows: $E_c$, conduction band; $E_v$, valence band; $V_{GS}$, gate-source voltage; $V_{DS}$, drain-source voltage; and $V_{TH}$, tunneling window.

dopants, and phonons [20, 21]. This band tail represents a fundamental limit to the steepness that can be practically achieved [22] and thus becomes a critical element in the model. The subthreshold swing can be degraded by interface states and defects [23, 24]. These effects are not included in the model, but could be added as experiments reveal the generic aspects of these mechanisms.

A. Kane-Sze Model

The TFET model is built on the Kane-Sze tunneling formula, which is evaluated by integrating the product of charge flux and the tunneling probability in the tunneling window calculated by using the Wentzel-Kramers-Brillouin (WKB) approximation [25]

$$I_p = aV_R \xi \exp \left( -\frac{b}{\xi} \right),$$  

(1)

where $V_R$ is the reverse bias on the tunnel junction, $\xi$ is the maximum electric field in the reverse biased junction, and $a$ and $b$ are coefficients determined by the material properties of the junction, given by [1]:

$$a = \frac{4q}{8\pi^2 \hbar^2} \frac{2m_e^*}{E_G}$$

(2)

$$b = \frac{4}{3} \frac{2m_e^* E_G^{1/3}}{3q\hbar},$$

where $m_e^* = (1/m_e + 1/m_h)^{1/2}$ is the reduced effective mass, which is the average of the electron, $m_e$, and hole, $m_h$, effective masses, $E_G$ is the semiconductor band gap, and $\hbar$ is the reduced Planck’s constant. The cross-sectional area of the junction, $A$, is the product of the channel thickness, $t_{ch}$, and the channel width, $W$.

The Kane-Sze expression, (1) is adapted to the following form,

$$I_D = aV_{DS} \xi \exp \left( -\frac{b}{\xi} \right),$$  

(3)

where the term $V_R$ is split into $f$ and $V_{TW}$. The first term, $f$, is a dimensionless factor controlling the current onset and saturation, which is based on the Fermi occupancy probability of filled states in the valence band and unfilled states in the conduction band. The second term, $V_{TW}$, the tunneling window, is related to the crossing and uncrossing of the energy bands. Because of the smearing of the band edge caused by the exponential decay of the band-tails in the band gap as $\sim e^{E_b/kT}/E_0$, with $E_0$ being the Urbach parameter [22], the tunneling window is assumed to increase exponentially with $V_{GS}$ before the bands cross and linearly after the bands have crossed.

B. Electric Field

It has been shown by Hurks [26] that the maximum electric field can be used effectively here without taking the actual electric field distribution near the tunnel junction into account. The maximum electric field in (3) is taken to be linearly dependent on $V_{GS}$ and $V_{DS}$

$$\xi = \xi_0 (1 + \gamma_1 V_{DS} + \gamma_2 V_{DS}).$$  

(4)

The electric field, $\xi_0$, is the built-in electric field at the source-channel tunnel junction when zero bias is applied to both gate and drain terminals. Parameters, $\gamma_1$ and $\gamma_2$, are linear coefficients with units of inverse volts. Increasing gate bias enhances the electric field at the source-channel junction by both enlarging the voltage drop (compared to the built-in voltage) and narrowing the tunneling barrier region. Increasing the drain bias has the same effect, but to a lesser degree because the drain field is screened by the gate electrode.

The use of (4) remains physically meaningful for broken-gap heterojunctions, where the concept of tunneling path and electric field can still be phenomenologically applied. Koswatta [27] shows that quantization effects along the transport direction produce a forbidden gap in the local density-of-states in the broken-gap junction. There exists an electron energy barrier for tunneling in the AlGaSb/InAs heterojunction that approaches a rectangular barrier with nanometer-scale thickness in the ON-state.
C. Subthreshold and Above-Threshold Region

In the subthreshold region, the drain current of a TFET depends exponentially on $V_{GS}$, which is dominated by the exponential decrease of the tunneling window with $V_{GS}$ below the threshold voltage. Accordingly, the tunneling window in the subthreshold region can be expressed by

$$V_{TW} = U \exp \left( \frac{V_{GS} - V_{th}}{U} \right) \quad (5)$$

Here, the factor, $U$, called the Urbach factor, is given by

$$U = \gamma_0 U_0 + (1 - \gamma_0)U_0 \left( \frac{V_{GS} - V_{OFF}}{V_{OFF} - V_{th}} \right) \quad (6)$$

where $\gamma_0$ controls how quickly the tunneling window closes with gate bias, $n$ is the subthreshold ideality factor, $V_{OFF}$ is the minimum voltage for which $V_{GS}$ is valid. The threshold voltage, $V_{TH}$, is defined as the gate-source bias at which the source valence-band-maximum equals the channel conduction-band-minimum (for an $n$-channel TFET). The dependence of $V_{TW}$ on $V_{GS}$ is plotted in Fig. 2 for different $\gamma_0$ values.

The drain current in the above-threshold region is directly controlled by the tunneling window. Above-threshold the tunneling window is given by

$$V_{TW} = V_{GS} - V_{TH}, \quad (7)$$

which can be called the overdrive voltage.

D. Bridging the Below and Above-Threshold Regions

A function is needed to connect the subthreshold and above-threshold regions smoothly. Borrowing from Khakifirooz [28] and Wright [29] for MOSFETs, the following expression allows a continuous transition between the subthreshold and above-threshold regions,

$$V_{FW} = U \ln \left[ 1 + \exp \left( \frac{V_{GF} - V_{OFF}}{U} \right) \right], \quad (8)$$

where $V_{FW}$ is the threshold voltage, $U$ is a constant, and $f$ is the function to connect the subthreshold and above-threshold regions.

The superlinear onset of the output characteristic is another signature behavior of the TFETs. De Michielis [12] showed that this characteristic arises from the Fermi occupancy of filled states in the source and unoccupied states in the channel. However, their expression for the drain current was not devised to account for the saturation of the drain current. This can be readily modified as shown below. Initially the following simple function $f$, was used to describe both the superlinear onset and the saturation of drain current with drain bias,

$$f = \frac{1 - \exp \left( -V_{DS}/\Gamma \right)}{1 + \exp \left( V_{THDS} - V_{DS}/\Gamma \right)} \quad (9)$$

where $\Gamma$ is a constant and $V_{THDS}$ is the drain threshold voltage, the minimum drain voltage needed to initiate the tunneling current [30]. In Fig. 4, (9) is plotted together with the expression from De Michielis [12]. The superlinear onset degrades drastically as $V_{THDS}$ becomes bigger than 0.1 V. In the low $V_{DS}$ region, the nonlinear turn-on of the drain current is well captured by (9). At large $V_{DS}$, the function, $f$, saturates to 1.

In utilizing (9) to fit TFET simulations, it became apparent that the drain threshold voltage, $V_{THDS}$, should be made sensitive $V_{GS}$. The drain threshold voltage has been found to increase linearly with gate voltage and then saturate at large $V_{GS}$ [30]. To account for this dependence, the drain threshold voltage was modified to

$$V_{THDS} = \lambda \tanh \left( \frac{V_{GS} - V_{OFF}}{U} \right) \quad (10)$$

where $\lambda$ is a constant with the unit of volts and the voltage inside the $\tanh$ function is normalized to 1 V.
Figure 5. Modeled and simulated transfer and output characteristics of a 20 nm InAs double-gate TFET. Atomistic simulation data are from [31].

Figure 6. Modeled and simulated transfer and output characteristics of a 20 nm broken-gap AlGaSb/InAs TFET. Numerical simulation data are from [32].

III. APPLICATIONS
The model is applied to a simulated double-gate (DG) InAs TFET [31] and a broken-gap AlGaSb/InAs TFET [32] and the results shown in Figs. 5 and 6. The channel length and width are 20 nm and 1 μm, respectively. The model shows good agreement to the simulations. Differences at low $V_{GS}$ in the transfer characteristics, Figs. 5(a) and 6(a), result because the ambipolar band-to-band tunneling current at the channel-drain junction is not accounted for in the model. Excellent representation of the superlinear current onset is shown in Figs. 5(b) and 6(b).

IV. CONCLUSION
An analytic n-channel TFET model for circuit simulation is shown to capture the current-voltage characteristics of the TFET. The model accounts for bias dependent subthreshold swing, saturation, and the superlinear current onset, in one continuous analytic equation. To justify the versatility of the model, the model is applied to a planar double-gate InAs TFET and a vertical broken-gap AlGaSb/InAs TFET, and good agreement is demonstrated between the model and both simulations. The simple equation set enables the implementation of an entry-level DC TFET model for exploration of steep transistor circuits. A generic terminal charge model is needed to enable transient and frequency-response analysis in SPICE.

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APPENDIX D:

UNIVERSAL ANALYTIC MODEL FOR TUNNEL FET CIRCUIT SIMULATION

Universal analytic model for tunnel FET circuit simulation

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1. Introduction

Tunnel field-effect transistors (TFETs) are candidates to compete with complementary metal-oxide-semiconductor (CMOS) FETs at low voltages because of their capability to achieve a subthreshold swing of less than 60 mV/decade at room temperature [1–3]. To build TFET circuits and make performance projections, it is of interest to develop simple, closed-form expressions for the drain current that contain the basic physics of the tunneling process and can be implemented in circuit simulators, e.g. SPICE.

Quite a few compact analytic models for the TFET have been developed [4–14]. Refs. [4–9] employ a semianalytical solution of Poisson’s equation in the channel region to model the drain current that contain the basic physics of the tunneling process and can be implemented in circuit simulators, e.g. SPICE. In most cases, the resulting expressions for the drain current are complex because the aim is to be predictive. The closest approach to our paper is that of Hong et al. [14] where the motivation is to develop an analytic model for use in circuit modeling. The resulting model gives good representation of the TFET characteristics, but is discontinuous and lacks an intuitive connection to the device physics.

Our intent has been to provide a simple and continuous equation set to describe the TFET current–voltage (I–V) characteristics. In this paper our model is extended into all operating regions and a capacitance model is added. The resulting model produces the I–V characteristics of the TFET at the level of an elementary MOSFET SPICE model. This model is shown to capture the essential features of the TFET predicted by more comprehensive numerical simulators. The generalized formulation does not rely on a specific TFET embodiment, e.g. lateral, vertical, inline, single-gate, double-gate, gate-all-around, inversion-mode, enhancement-mode, gate-field aligned to the tunnel junction, or gate-field perpendicular to the tunnel junction, hence the model is widely configurable. The purpose is to provide a model that has the core physics, like in the level 1 MOSFET SPICE model, which can be easily implemented and fitted to experimental data, and allow elementary circuit design.

The paper is organized as follows. Section 2 describes the development of the model in the normal operating region, including the physics of the subthreshold and above threshold regions and how these regions are connected. In this section, the model is applied to the representation of a homojunction InAs double-gate p–i–n TFET and a broken-gap AlGaSb/InAs single-gate inline TFET. Section 3 extends the model into other operating regions by incorporating the ambipolar current and negative differential resistance (NDR).
Section 4 introduces a simple empirical capacitance model that is shown to capture the behavior of capacitances in TFETs.

2. Model development

Tunnel FETs utilize an MOS-gate to control the band-to-band tunneling across a degenerate p-n junction. The schematic cross-section and energy band diagrams of n-channel TFET in OFF and ON states are shown in Fig. 1. The device is normally off. When zero bias is applied to the gate, the conduction band minimum of the channel is located above the valence band maximum of the source, so band-to-band tunneling is suppressed. A tunneling window, \( qV_{GS} \), opens up as the conduction band of the channel is shifted below the valence band of the source. Electrons in the valence band with energy in this tunneling window tunnel into empty states in the channel and the transistor is ON. The principle of operation is the same for a p-i-n TFET, except that the n-channel TFET is an enhancement-mode device while the p-i-n TFET is inversion-mode.

The central expression in the TFET model is an experimentally well-established equation for band-to-band, Zener tunneling in p-n junctions [16,17], the primary transport mechanism in tunnel transistors [1,18]. The two-terminal Zener tunneling behavior is then generalized to three terminals by introducing physics-based expressions for the bias-dependent tunneling window and a dimensionless factor which accounts for the superlinear current onset in the output characteristic.

The signature feature of the TFET is the decrease in subthreshold swing with decreasing drain current, which is well established in both simulations [17,19] and experiments [20,21]. The model assumes that this is caused by the exponential band tails that arise from imperfections and lattice disorder due to impurities, dopants, and phonons [22,23] and extend into the band gap. This band tail, also known as the Urbach tail, represents a fundamental limit to the steepness that can be practically achieved [24] and thus becomes an adjustable element in the model. The subthreshold swing can be degraded by interface states and defects [25,26]. While the physics of these effects are not included in the model, they presumably could be added as experiments reveal the generic aspects of these mechanisms.

2.1. Kane–Sze model

The TFET model is built on the expression for the current in a p+n+n tunnel junction described by the Kane–Sze tunneling formula,

\[
J_p = qV_{in} \exp \left( \frac{b}{T} \right),
\]

where \( V \) is the reverse bias on the tunnel junction and physically accounts for the energy range, \( qV \), over which the tunneling occurs, \( \xi \) is the maximum electric field in the reverse biased junction, and \( a \) and \( b \) are coefficients determined by the material properties of the junction, given by [1]:

\[
a = \frac{1}{12} V_0^{1/3}, \quad b = \frac{4}{3} V_0^{2/3}
\]

where \( m^* \) is the reduced effective mass, \( V_0 \) is the product of the channel thickness, \( t_{on} \), and the width of the channel, \( W \).

The Kane–Sze expression, (1) is adapted to the following form,

\[
J_p = qV_{in} \xi \exp \left( \frac{b}{T} \right),
\]

where the term \( V \) is split into two bias-dependent terms, \( f \) and \( V_{TW} \). The first term, \( f \), is a dimensionless factor controlling both the current onset and saturation versus \( V_{in} \), which is based on the Fermi occupancy probability of filled states in the valence band and undoped states in the conduction band. The second term, \( V_{TW} \) is the tunneling window, in volts, related to the crossing and uncrossing of the energy bands. Because of the smearing of the band edge caused by the exponential decay of the band-tails in the band gap as \( e^{-\frac{E}{V_0}} \), with \( E_0 \) being the Urbach parameter [28], the tunneling window is assumed to increase exponentially with gate bias before the bands cross and then linearly after the bands have crossed.

The maximum electric field, \( \xi \), is assumed to be linearly dependent on the gate–source bias, \( V_{GS} \), and drain–source bias, \( V_{DS} \). In deriving (1), the tunneling process is approximated by a particle tunneling through a triangular barrier, with a slope given by the electron charge times the electric field \( V \). It has been shown by Hurks [26] that the maximum electric field can be used effectively here without taking the actual electric field distribution near the tunnel junction into account. Mathematically speaking, the detailed dependence of maximum electric field on \( V_{GS} \) and \( V_{DS} \) can always be approximated with a polynomial of certain degree. To make the model widely applicable to devices with different architectures, the maximum electric field is taken to be linearly dependent on \( V_{GS} \) and \( V_{DS} \) by dropping the second and higher order terms.

2.2. Electric field

The maximum electric field in (3) is taken to be linearly dependent on gate–source bias, \( V_{GS} \), and drain–source bias, \( V_{DS} \).

\[
\xi = \xi_0 \left( 1 + \gamma_1 V_{GS} + \gamma_2 V_{DS} \right).
\]

The electric field, \( \xi_0 \), is the built-in electric field at the source–channel junction when zero bias is applied to both gate and drain terminals. Parameters, \( \gamma_1 \) and \( \gamma_2 \), are linear coefficients with units of inverse volts. Increasing gate bias enhances the electric field at the source–channel junction by both enlarging the voltage drop (compared to the built-in voltage) and narrowing the...
tunneling barrier region. Increasing the drain bias has the same effect, but to a lesser degree because the drain field is screened by the gate electrode.

It is worth noting that the use of (4) remains physically meaningful even for broken-gap heterojunctions, where the concept of tunneling path and corresponding electric field can still be phenomenologically applied. Consideration of quantization effects along the transport direction produce a forbidden gap in the local density-of-states in the broken gap junction. Also note that there exists an electron energy barrier for tunneling in the AlGaSb/InAs heterojunction that approaches a rectangular barrier with nanometer-scale thickness in the ON-state. As a result, a current relation of the same form of (4) can be expected.

2.3 Subthreshold region

In the subthreshold region, the drain current of a tunnel FET depends exponentially on the gate bias, which is dominated by the exponential decrease of the tunneling window with $V_{CG}$ below the threshold voltage. Accordingly, the tunneling window in the subthreshold region can be expressed by

$$V_{TW} = U \exp \left( \frac{V_{CG} - V_{TH}}{U} \right).$$

(5)

Here, the factor, $U$, called the Urbach factor, is given by

$$U = \gamma_0 U_0 + (1 - \gamma_0) U_0 \exp \left( \frac{V_{CG} - V_{OFF}}{U_0} \right),$$

(6)

where $\gamma_0$ is a parameter that controls how quickly the tunneling window closes with gate bias, $n$ is the subthreshold ideality factor, $V_{OFF}$ is the minimum $V_{CG}$ voltage for which (6) is valid. The threshold voltage $V_{TH}$ is defined as the gate–source bias at which the source valence-band-maximum equals the channel conduction-band-minimum (for an $n$-channel TFET). The expression (6) causes the subthreshold swing to decrease linearly with gate bias. When $V_{CG}$ equals $V_{OFF}$, $U$ is $\gamma_0 U_0$, and $\gamma_0$ is a factor less than or equal to 1. When the gate bias is equal to the threshold voltage then $U$ equals $U_0$.

The dependence of the tunneling window on gate–source bias is plotted in Fig. 2 for different $\gamma_0$ values. When the parameters $\gamma_0$ and $n$ equal one, $U$ reduces to $U_0$, and the tunneling window is represented by a straight line in a semilog plot, corresponding to an exponentially closing tunneling window of 60 mV/decade. If $\gamma_0$ is reduced below 1, the subthreshold swing decreases as the gate–source voltage decreases as can be observed in Fig. 2.

2.4 Above-threshold region

According to (3), the drain current in the above-threshold region should be directly controlled by the tunneling window. Above-threshold the tunneling window should be given by

$$V_{TW} \approx V_{CG} - V_{TH},$$

(7)

which can be called the overdrive voltage.

2.5 Bridging the subthreshold and above-threshold regions

A function is needed to connect the subthreshold and above-threshold regions smoothly. Borrowing from Khakifirooz [30] and Wright [31] for MOSFETs, the following expression allows a continuous transition between the subthreshold and above-threshold regions,

$$V_{TW} = U \ln \left( 1 + \exp \left( \frac{V_{CG} - V_{TH}}{U} \right) \right).$$

(8)

Fig. 3 shows the tunneling window as a function of gate–source voltage. When in the subthreshold region, the tunneling window grows exponentially with gate bias, but in the above-threshold region, it tends to a linear dependence on the gate bias. Whereas the mathematical expression in (8) is able to describe both exponential and linear regions in a single equation, there is no physical basis to justify its accuracy in the transition region, $\sim 3nKt$. This is also true in the MOSFET where this function has been effectively utilized to link subthreshold and linear regions [30,31].

2.6 Superlinear current onset

The superlinear onset of the output characteristic is another signature behavior of the TFETs. De Michiels [13] showed that this characteristic arises from the Fermi occupancy of filled states in the source and unoccupied states in the channel. However, their expression for the drain current was not devised to account for
the saturation of the drain current. This can be readily added as shown below. Initially the following simple function was used to describe both the superlinear onset and the saturation of drain current with drain–source bias,

\[
f = \frac{1 - \exp\left(-\frac{V_{DS}}{\lambda}\right)}{1 + \exp\left(\frac{V_{DS}}{\lambda}\right)}
\]

(9)

where \(\lambda\) is a constant and \(V_{THDS}\) is the drain threshold voltage which corresponds to the minimum drain voltage needed to initiate the tunneling current \([32]\). When \(V_{DS}\) equals zero, then (9) and the tunneling current are zero. When \(V_{DS}\) becomes large, the function \(f\) tends to one.

In Fig. 4, (9) is plotted together with the expression from De Michiels \([13]\). In the low \(V_{DS}\) region the nonlinear turn-on of the drain current is well captured by (9). The superlinear onset degrades drastically as \(V_{THDS}\) becomes bigger than 0.1 V. At large \(V_{DS}\), the function \(f\) saturates to 1, as desired.

In utilizing (9) to fit TFET simulations, it became apparent that the drain threshold voltage, \(V_{THDS}\) should be made sensitive to gate bias. The drain threshold voltage has been found to increase linearly with gate voltage and then saturate at large \(V_{GS}\) \([32]\). To account for this dependence, the drain threshold voltage was modified to

\[V_{THDS} = \lambda \tanh\left(V_{GS} - V_{OFF}\right),\]

(10)

where \(\lambda\) is a constant with the unit of volts and the voltage inside the tanh function is normalized to 1 V. The hyperbolic tangent function is chosen because when \(V_{GS} < V_{OFF}\) is small,

\[
\tanh\left(V_{GS} - V_{OFF}\right) \approx V_{GS} - V_{OFF},
\]

(11)

and when \(V_{GS} - V_{OFF}\) is large,

\[
\tanh\left(V_{GS} - V_{OFF}\right) \approx 1.
\]

(12)

The function \(f\) in (9) then becomes

\[
f = \frac{1 - \exp\left(-\frac{V_{DS}}{\lambda}\right)}{1 + \exp\left(\lambda \tanh\left(V_{GS} - V_{OFF}\right)\right)}
\]

(13)

In order to test the ability of the model to represent TFET physics, we have fitted the model to two very different TFET embodiments. The first is a double-gate p-i-n InAs TFET \([33]\) with characteristics predicted by an atomistic quantum–mechanical device simulator, and the second is a single-gate in-line broken-gap AlGaSb/lnAs TFET \([34]\) as predicted by Synopsis technology computer-aided design (TCAD). The results are shown in Figs. 5 and 6. The channel length and width are 20 nm and 1 \(\mu m\), respectively. The model shows good agreement to the simulations. Excellent representation of the superlinear current onset is shown in Figs. 5b and 6b. Close inspection of the bias dependence of the transconductances and conductances obtained by the model shows that the terminal dependences are not matched precisely owing to the generic nature of the tunneling description.

The device model parameters in Table 1 represent two markedly different transistor geometries, a DG homojunction TFET and a SG heterojunction in-line TFET. The two devices share the same InAs channel, so \(E_c\) and \(m_{i}\) are the same. For both transistors, \(\gamma_s\) is the prefactor for \(V_{THs}\), which is much smaller than \(\gamma_d\), the prefactor for \(V_{THd}\), because the \(V_{THd}\) dependence of the electric field is much stronger than the \(V_{THs}\) dependence as a result of the screening effect of the gate electrode. The in-line TFET has a smaller \(\gamma_d\) than the double-gate TFET, perhaps a measure of the superiority of DG vs. SG geometries.

### 3. Complete DC model of TFETs

The model discussed thus far is valid for positive \(V_{GS}\) and \(V_{DS}\). Often in RF or transient simulations all four quadrants of the \(I_D-V_{DS}\) characteristic may be needed. A tunnel FET is essentially a gated p-i-n tunnel diode. The asymmetrical source/drain junction causes tunnel FETs to have asymmetrical characteristics when the drain–source bias is reversed. When forwardly biased \((V_{DS} < 0)\), the band-to-band tunneling current gradually gives way to the diffusion current as \(V_{DS}\) is decreased, resulting in NDR in the \(I_D-V_{DS}\) characteristic. Also due to the asymmetrical doping, the tunnel junction shifts from the source–channel junction to drain–channel junction when the gate bias reverses, resulting in ambipolar conduction.

To fully make use of these features in circuit design, our model is extended into all four quadrants of operation: (1) \(I_D\) \([V_{DS} > V_{OFF}, V_{GS} > 0]\), (2) \(I_D\) \([V_{DS} < V_{OFF}, V_{GS} > 0]\), (3) \(I_D\) \([V_{DS} < V_{OFF}, V_{GS} < 0]\), and (4) \(I_D\) \([V_{DS} > V_{OFF}, V_{GS} < 0]\). The equation set outlined in Section 2 describes a model that operates in the first quadrant only. In this section, currents in the other three quadrants are defined.

#### 3.1. Second quadrant – the ambipolar current: \(I_D\) \([V_{GS} > 0, V_{DS} < 0]\)

In the conventional mode of operation, the TFET tunnel current is suppressed when \(V_{DS}\) is low and then the tunnel window at the source junction is opened with positive \(V_{GS}\). However the TFET can also turn on when gate bias is sufficiently negative. As shown in Fig. 7a, for a p-i-n TFET, when the gate bias is negative, the valence band maximum of the channel can be shifted above the conduction band minimum of the drain. Meanwhile, the drain–channel junction narrows as a result of the large voltage drop on the junction, leading to electrons tunneling from the channel into the empty states in the drain. Therefore, the tunneling window opens up again, with the tunnel junction shifted from the source–channel junction to the drain–channel junction. When this happens the channel conduction changes from one carrier type to another and the current is said to be ambipolar. Ambipolar current is not limited to p-i-n TFETs. At negative gate bias, a parasitic junction can form near the drain contacts even in an n-channel TFET, leading to the ambipolar conduction actually reported in \([34]\).

The ambipolar current is added to the model by copying the current for \(V_{DS} > V_{OFF}\) to \(V_{DS} < V_{OFF}\) and multiplying the current by a smoothing function, \(f_s\). The term \(V_{DS}\) is replaced with \(V_{DS} - V_{OFF}\) in (4). To preserve the current continuity at \(V_{DS} = V_{OFF}\), \(f_s\) decreases from 1 when \(V_{DS} < V_{OFF}\) to an attenuation factor \(s\) when \(V_{DS} < V_{OFF}\).
As $V_{GS}/C_0$ decreases from 0, as shown in Fig. 7b, the ambipolar drain current is given by

$$I_D(\text{V}_{GS}<\text{V}_{OFF}) = I_D(\text{V}_{GS} > \text{V}_{OFF})f_s$$

$$f_s = (1 - (1 - s) \tanh \left( -\frac{V_{GS}}{V_{OFF}} \right)).$$

where $s$ is an attenuation factor that sets the ratio of $I_D(\text{V}_{GS}<\text{V}_{OFF})$ to $I_D(\text{V}_{GS} > \text{V}_{OFF})$. In cases where the ambipolar current is suppressed, $s$ can be set to a small number. The scaling factor, $s$, is taken to be dimensionless, because $V_{GS}/C_0$ in the argument of the tanh function is considered to be normalized to 1 V. Fig. 8 shows the drain current plotted as a function of gate–source bias from $-0.5$ V to 0.5 V with $s$ set to 1 and 0.1, respectively.

3.2. Third quadrant: $I_D(\text{V}_{GS}<\text{V}_{OFF}, \text{V}_{DS}<0)$

The third quadrant is the least used region. In this region, the current is defined using the universal diode current equation,

$$J_D = \frac{J_0}{C_0} \frac{e^{V_{DS}/NkT}}{1 + e^{V_{DS}/NkT}}$$

where $J_0$ is the saturation current and $N$ is the ideality factor.

3.3. Fourth quadrant – the negative differential resistance region: $I_D(\text{V}_{GS}>\text{V}_{OFF}, \text{V}_{DS}<0)$

When the drain–source bias, $V_{DS}$, is negative, the source–channel junction is forward biased and behaves like a forward-biased diode.
tunnel diode. The NDR is included by modifying a model for the tunnel diode from Sze and Ng [35].

\[
J = J_0 e^{V_{DS}/V_T} + J_0 \left( e^{V_{DS}/V_T} - 1 \right).
\]

(16)

Adapted to the notation of our model, this formula becomes

\[
J_0 = -\left( \frac{J_0}{e^{V_{DS}/V_T}} \left( V_{DS} - V_{th} \right) + J_0 \left( e^{V_{DS}/V_T} - 1 \right) \right)
\]

(17)

The six parameters \(J_0, \eta, V_p, K, \eta, \) and \(n\) are fitting parameters. Parameter \(K\) has unit of \(V^{-1}\). Parameter \(\eta\) and \(n\) are dimensionless. Parameter \(n\) is the diode ideality factor and shares the same value as \(n\) in (6). As shown in Fig. 9, the experimental NDR behavior is well captured by this semi-empirical equation. Series drain and source resistance can always be added as subcircuit parameters to account for parasitic resistances.

4. Capacitance model

The partitioning of gate capacitances between the source and drain in TFETs is significantly different from CMOS, primarily due to the difference in the distribution of inversion charge [36,37]. Under positive bias, while the channel of an \(n\)-channel TFET is accumulated with electrons, the channel of a \(p-i-n\) TFET is inverted, which means that the inversion layer is formed at a higher \(V_{GS}\) for \(p-i-n\) TFETs. Because \(C_{GS}\) is much smaller compared to \(C_{GD}\) and will be dominated by interconnect capacitance, it is set as a constant. Noticing the similarity between the \(f\) function (Fig. 4) and the behavior of \(C_{GD}\) with increasing \(V_{GS}\) and \(V_{DS}\) (Fig. 10), the \(f\) function is modified to model the behavior of \(C_{GD}\):

\[
C_{GD} = C_{GD,\text{MIN}} + (C_{GD,\text{MAX}} - C_{GD,\text{MIN}}) \frac{\left( 1 + \beta V_{DS} \right)}{1 + \exp \left( \frac{V_{DS} - V_{th}}{V_T} \right)} \]

(18)

where \(C_{GD,\text{MIN}}\) and \(C_{GD,\text{MAX}}\) are the approximate minimum and maximum of \(C_{GD}\). Parameters \(\alpha, \beta, \Gamma,\) and \(m\) are fitting parameters, in
5. Conclusion

An analytic n-type TFET model for circuit simulation is shown to capture the current–voltage characteristics of the TFET in all operation regions. The model can be readily adapted to describe the p-type TFET. The model accounts for bias dependent subthreshold swing, saturation, the superlinear current onset, ambipolar conduction, and negative differential resistance. A simple behavioral capacitance model is also included. To justify the versatility of the model, the model is applied to two TFETs with distinctly different geometries, a planar double-gate InAs TFET and a broken-gap AlGaSb/InAs inline TFET, and good agreement is demonstrated between the model and both simulations. The equation set enables the implementation of an entry-level TFET model for exploration of steep transistor circuits.

Acknowledgements

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References


APPENDIX E:

UNIVERSAL TFET SPICE MODEL INCLUDING NOISE, GATE TUNNELING, AND CHARGE

Universal Charge-Conserving TFET SPICE Model Incorporating Gate Current and Noise

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ABSTRACT An analytical compact model for tunnel field-effect transistor (TFET) circuit simulation is extended by adding a gate tunnel current model, a charge-based capacitance model, and a noise model. The equation set is broadly applicable across materials systems and TFET geometries and is readily fitted to rigorous physics-based device simulations and experimental results. To validate the gate current and charge models, technology computer-aided design (TCAD) simulations of a GaN/InN/GaN TFET are used. TCAD simulations show that the gate tunneling current depends on the gate–drain bias with a 100%/0% drain/source current partition. Terminal capacitances evaluated from the charge model agree well with simulations. The model is implemented in Verilog-A and the significance of gate current in the circuit design is illustrated in an amplifier design.

INDEX TERMS Gallium nitride (GaN), gate leakage, semiconductor device noise, SPICE, subthreshold swing, tunnel field-effect transistor (TFET).

I. INTRODUCTION

Tunnel field-effect transistors (TFETs) continue to be widely investigated to achieve sub-60-mV/decade subthreshold swing at room temperature for low-power digital and analog applications [1]–[5]. SPICE-friendly analytic TFET models are needed for TFET circuit design. In 2014, a continuous physics-based analytical model was reported [6]. The aim of this model was to provide an equation set with wide applicability across materials systems and device geometries. Gate-bias-dependent subthreshold swing and superlinear current onset were both captured in this first model. In 2015, the model was extended to include all four quadrants of the current–voltage characteristic [7], including the negative differential resistance of the source Esaki tunnel junction and an empirical capacitance model. However, since the capacitance model was not charge based, charge conservation was not guaranteed for all possible parameter values. In this paper, we enhance the model by adding a gate tunneling current model, a charge-based capacitance model, and a noise model.

Gate leakage becomes a significant part of the total leakage current when the gate-stack is aggressively scaled as is necessary to achieve steep subthreshold swing. Gate current limits the ON–OFF ratio and degrades subthreshold swing. The inclusion of a gate tunneling current model is essential for subthreshold, near-threshold, and ultralow voltage circuit design [8]. A generalized charge model is needed to guarantee charge conservation in switched-capacitor and charge-pump circuits. There are prior reports of charge models for TFETs; Yang et al. [9] successfully adapted a formulation from BSIM3 to describe the drain charge, and Zhang et al. [10], [11] developed an analytical charge model for double-gated Si TFETs. However, these previous methods
are not readily generalized to new materials and transistor geometries. Our formulation for the terminal charges is in agreement with technology computer-aided design (TCAD) simulations and is sufficiently general to apply broadly across TFET geometries.

As technology continues to scale down, the presence of electrical noise poses great challenge to the design of high-performance circuits for low-voltage and low-power applications. Based on the recommendations provided in [3], a simple noise model is included to provide a framework for consideration of noise. There are a few reports of noise measurements in Si TFETs [12]–[14] and GaAsSb/InGaAs-based III–V TFETs [15], [16]. An analytical model including both low- and high-frequency noise sources in III–V heterojunction TFETs has been reported in [17]. But the proposed model may not apply to other material systems or device geometries. With limited experimental measurements available, this simplified noise model is proposed as an approximation for circuit design, allowing easy fitting to simulations and experiments.

Both the gate leakage model and the charge model are verified against TCAD simulations for the GaN/InN TFET [18]. Finally, the model is coded in Verilog-A, and as an example, a TFET-based amplifier is implemented to show the impact of gate current on the design. The model is now available in AIM-SPICE [19] and Verilog-A [20]. The complete equation set, including the dc model [6], [7], the gate tunneling model, the simplified noise model is proposed as an approximation for circuit design, allowing easy fitting to simulations and experiments.

The gate leakage model and the charge model are verified against TCAD simulations for the GaN/InN TFET [18]. Finally, the model is coded in Verilog-A, and as an example, a TFET-based amplifier is implemented to show the impact of gate current on the design. The model is now available in AIM-SPICE [19] and Verilog-A [20]. The complete equation set, including the dc model [6], [7], the gate tunneling model, the simplified noise model, and all the parameters are summarized in the supplementary information.

![FIGURE 1. (a) Schematic and band diagram of sidewall double gate GaN/InN heterojunction TFET along the (b) x- and (c) y-direction.](image)

**II. DEVICE STRUCTURE AND NUMERICAL SIMULATION**

To illustrate the model and further show how it extends across materials systems, a double-gate GaN/InN heterojunction TFET, as shown in Fig. 1(a), is used to provide the reference data. The nitride TFET, simulated by TCAD (Synopsys Sentaurus [21]), has several appealing attributes relative to TFETs in other systems. The 3.2-eV bandgap of GaN provides a low OFF current, $I_{OFF}$, while effectively eliminating ambipolar current. The use of InN, with a bandgap of 0.7 eV and strong polarization discontinuity with respect to GaN, results in a $\sim 20$ MV/cm built-in electric field within the p-GaN/InN/n-GaN heterojunction and a tunneling distance of approximately 1 nm [see Fig. 1(c)]. Simulation of the device ON current in this heterojunction indicates that $I_{ON} = 200 \mu A/\mu m$ at 0.4 V is possible [18]. While the GaN/InN/GaN TFET TCAD simulations provide a good basis for developing the SPICE model, the model does not include the effects of scattering caused by phonons, impurities, and defects in the junction, which could be significant in this structure.

**III. TFET GATE TUNNELING CURRENT MODEL**

The gate leakage current in TFETs originates from direct tunneling current through the gate oxide. The band diagram across the gate-stack is shown in Fig. 1(b). Because of the intimate connection between the channel and drain, TCAD simulations show that the gate leakage current is predominantly controlled by the gate–drain voltage $V_{GD}$. Based on this understanding, the semi-empirical gate tunneling model developed for CMOS [22], [23] can be adapted to describe the TFET. In CMOS, the gate tunneling current is divided between the source and drain terminals, while in TFETs the gate current is collected primarily at the drain for most bias conditions of interest.

The gate tunneling current is modeled by the following equation obtained from [23]:

$$J_g = \frac{nq}{8\pi \hbar \phi_B k_{B,0}} C(V_{GD}, T_{PHY}, \phi_B) \lim_{x \to \infty} \exp \left[ -8\pi \sqrt{2m_{OX}(\epsilon\phi_B)^3/2} \left( 1 - \frac{|V_{GD}|}{\phi_B} \right)^{3/2} \right]$$

where one additional parameter $n_0$ is added to account for the number of gates (i.e., 1 for single-gated devices and 2 for double-gated devices) and the electric field across the gate dielectric, $E$, is assumed to be uniform and modeled by $V_{GD}/T_{PHY}$. It is reasonable when the channel is conducting. In device structures where the electric field relation is more complex, this formulation will need revision; however, we have found that this simple relation provides a good representation for the cases we have considered. Other parameters include $\phi_B$, the Ti/AI$_2$O$_3$ barrier height, $\kappa_0$, the gate dielectric constant, and $T_{PHY}$, the physical thickness of the gate dielectric. The electron effective mass in the oxide, $m_{OX}$, is used as a fitting parameter. The empirical correction function of Lee and Hu [22], $C(V_{GD}, T_{PHY}, \phi_B)$, is given by

$$C(V_{GD}, T_{PHY}, \phi_B) = N \left( \frac{V_{GD}}{T_{PHY}} \right) \exp \left[ 20 \frac{|V_{GD}|}{\phi_B} \left( 1 - \frac{|V_{GD}|}{\phi_B} \right) \right]$$

where $\alpha$ is a fitting parameter. The auxiliary function $N$ represents the density of carriers in the channel and is expressed...
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2329-9231 (c) 2016 IEEE. Translations and content mining are permitted for academic research only. Personal use is also permitted, but republication/redistribution requires IEEE permission. See

by [22], [23]

\[
N = \frac{kT_0}{T_{PHY}} \left[ n_T V_T \ln \left( 1 + \exp \left( \frac{V_{GD} - V_{OFF}}{n_T V_T} \right) \right) \right] + n_A V_A \ln \left( 1 + \exp \left( -\frac{V_{GD} - V_A}{n_A V_A} \right) \right) \tag{3}
\]

where \( V_T = kT/q \) is the thermal voltage, parameters \( n_T \) and \( V_{OFF} \) set the current for positive \( V_{GD} \), and \( n_A \) and \( V_A \) for negative \( V_{GD} \).

By [22], [23]

\[
Q_D = n_0 WL \frac{kT_0}{T_{PHY}} \left[ -A_D \ln \left( 1 + \exp \left( \frac{V_{GS} - B_D}{A_D} \right) \right) \right] + C_D V_{GS} + D_D
\]

\[
Q_S = -n_0 WL \frac{kT_0}{T_{PHY}} \left( A_S \ln [1 + \tanh(B_S V_{GS} + C_S) \right] + D_S V_{GS} + E_S
\]

\[
Q_G = -(Q_S + Q_D) \tag{4}
\]

where \( W \) is the gate width and the coefficients \( A \) to \( E \) are modeled as linear functions of \( V_{GS} \)

\[
X_{D,S} = X_{D1,S1} V_{DS} + X_{D2,S2}
\]

\[
X = [A, B, C, D, E] \tag{5}
\]

where \( X_{D1,S1} \) and \( X_{D2,S2} \) are coefficients (e.g., \( A_D = A_{D0} V_{DS} + A_{D2} \), \( A_S = A_{S1} V_{DS} + A_{S2} \)).

The form of \( Q_D \) in (4) is chosen to account for the two different charge regimes, i.e., that due to ionized impurities in the channel at low \( V_{GS} \) and that due to free-carrier charge at high \( V_{GS} \). The proposed formula of \( Q_D \) in (4) connects two approximately linear charge–voltage relationships in Fig. 3. The first two terms in (4) have the form ln(1 + e^ax) + bx with the property that when \( x \ll 0 \), ln(1 + e^ax) \approx e^{-ax} + bx \approx ax + bx \), and when \( x \gg 0 \), ln(1 + e^ax) + bx \approx ax + bx \). Therefore, (4) provides a function that gives one linear \( Q–V \) relation at low \( V_{GS} \) and another at high \( V_{GS} \).

IV. TFET CHARGE MODEL

In TFETs, the charge partition is significantly different from MOSFETs, primarily due to differences in the channel charge distribution [9]. The terminal charges \( Q_D \) and \( Q_S \) are modeled using parameterized empirical expressions, which are chosen to match the form of the TCAD-simulated terminal charge

\[
Q_0 = n_0 WL \frac{kT_0}{T_{PHY}} \left[ -A_0 \ln \left( 1 + \exp \left( \frac{V_{GS} - B_0}{A_0} \right) \right) \right] + C_0 V_{GS} + D_0
\]

\[
Q_S = -n_0 WL \frac{kT_0}{T_{PHY}} \left( A_S \ln [1 + \tanh(B_S V_{GS} + C_S) \right] + D_S V_{GS} + E_S
\]

\[
Q_G = -(Q_S + Q_D) \tag{4}
\]

where \( W \) is the gate width and the coefficients \( A \) to \( E \) are modeled as linear functions of \( V_{GS} \)

\[
X_{D,S} = X_{D1,S1} V_{DS} + X_{D2,S2}
\]

\[
X = [A, B, C, D, E] \tag{5}
\]

where \( X_{D1,S1} \) and \( X_{D2,S2} \) are coefficients (e.g., \( A_D = A_{D0} V_{DS} + A_{D2} \), \( A_S = A_{S1} V_{DS} + A_{S2} \)).

The form of \( Q_D \) in (4) is chosen to account for the two different charge regimes, i.e., that due to ionized impurities in the channel at low \( V_{GS} \) and that due to free-carrier charge at high \( V_{GS} \). The proposed formula of \( Q_D \) in (4) connects two approximately linear charge–voltage relationships in Fig. 3. The first two terms in (4) have the form ln(1 + e^ax) + bx with the property that when \( x \ll 0 \), ln(1 + e^ax) \approx e^{-ax} + bx \approx ax + bx \), and when \( x \gg 0 \), ln(1 + e^ax) + bx \approx ax + bx \). Therefore, (4) provides a function that gives one linear \( Q–V \) relation at low \( V_{GS} \) and another at high \( V_{GS} \).

In Fig. 3, the modeled terminal charges (solid lines) agree well with TCAD simulation (symbols). The values of the fitting parameters are presented in Table 1. Because the
The two most significant capacitances for the transistor in the first quadrant, $C_{DG}$ and $C_{SG}$, are computed as

$$C_{DG} = -\frac{\partial Q_D}{\partial V_G}$$

$$C_{SG} = -\frac{\partial Q_S}{\partial V_G}$$

In Fig. 4, the two terminal capacitances computed from the model are shown to match well with the TCAD simulations.
$I_{n,1/f}^2 = 2qI_D$ in A$^2$/Hz. In parallel with this source, there should exist a junction flicker noise source as previously described. This source is uncorrelated with the conventional MOS flicker noise, and both have $1/f^n$ dependence. Here we lump both $1/f$ sources in a single source in the gate as in the MOSFET, $V_{n,1/f}^2 = K/f^n$ in V$^2$/Hz, where $K$ is a constant and $n$ is a factor to account for the frequency dependence ($n = 1$ for $1/f$ noise, and $n = 2$ for RTN noise), both of which can be extracted from measurements or simulation data. In the absence of measured or modeled TFET noise data, Pandey et al. [17] provide an analytical model developed for the III–V heterojunction TFETs, which can be used to provide baseline estimates of the factor $K$ and its dependence on trap density, electric field, dielectric constant, and geometry.

### TABLE 2. DC model parameters.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value 1</th>
<th>Value 2</th>
<th>Value 3</th>
</tr>
</thead>
<tbody>
<tr>
<td>$E_g$ (eV)</td>
<td>0.8</td>
<td>$\gamma_s$</td>
<td>0.2411</td>
</tr>
<tr>
<td>$\Gamma_{s}$ (V)</td>
<td>0.0118</td>
<td>$\gamma_{i}$ (m$^{-1}$)</td>
<td>0.01</td>
</tr>
<tr>
<td>$\Gamma_{i}$ (V)</td>
<td>0.1901</td>
<td>$\gamma_{i}$ (m$^{-1}$)</td>
<td>0.1107</td>
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<tr>
<td>$\lambda$ (V)</td>
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<td>$L_{eff}$ (nm)</td>
<td>10</td>
</tr>
<tr>
<td>$\kappa_0$</td>
<td>0.2569</td>
<td>$V_{off}$ (V)</td>
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</tr>
<tr>
<td>$\kappa_i$ (V$^{-1}$)</td>
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<td>$V_{on}$ (V)</td>
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</tr>
<tr>
<td>$m_n^*$</td>
<td>0.1</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

As shown in Fig. 7, the small-signal characteristics such as transconductance and output conductance calculated from the model are in close agreement with TCAD simulation over the bias range of Fig. 6, making the model suitable for analog applications.

### VII. CIRCUIT APPLICATION

To illustrate some of the features of the universal model in a circuit context, a simple common-source low-power amplifier has been designed and simulated using the Verilog-A implementation of the model and the Eldo simulator from Mentor Graphics. The schematic of the amplifier and the model of the source are shown in Fig. 8.

To illustrate the effect of gate leakage current, the amplifier is driven by a high-impedance source and is simulated with and without gate leakage and using two different threshold voltages for $M_1$. The high-impedance source can be viewed.
as a preceding amplifier stage having a high output resistance. The gate leakage current generally causes the source signal to be attenuated at the amplifier input, but the effect of leakage current is more pronounced in a low-$V_{TH}$ TFET versus a high-$V_{TH}$ TFET.

Fig. 9 compares the voltage gain for a 10-GΩ source resistance for two different threshold voltage GaN TFETs with and without gate leakage current enabled. Table 3 shows how the operating points change in these comparisons. The amplifier takes advantage of the high intrinsic gain of the TFET, enabling the gate leakage current makes the low-frequency gain drop from 52 to 20 dB, and $V$(out) drops from 0.34 to 0.14 V. When $V_{TH}$ is 0.45 V, the gain barely changes when gate leakage current is enabled while $V$(out) stays almost the same. The gate leakage current, which is the same as the current going through $R_S$, the low-frequency gain drop increases from 4.57 to 246.4 fA when $V_{TH}$ changes from 0.45 to 0.15 V.

The effect of threshold voltage change can be understood by noting that the gate leakage current increases exponentially with $|V_{GD}| = V_{DS} - V_{GS}$; lowering the $V_{TH}$ of $M_1$ decreases $V_{GS}$ while keeping the overdrive constant. Due to the high intrinsic gain of $M_1$, a small change at the input changes the operating point at the output (and thus the gain) significantly.

**VIII. CONCLUSION**

With the development of a gate tunneling current model, charge-based capacitance model, and noise model, a universal TFET SPICE model for circuit design is presented. The model is universal in the sense that it covers all operating regions and biases of interest for low-power applications and can be applied to TFETs with various geometries and across material systems. With the addition of gate current, charge-based capacitance, and noise, the model now has capabilities needed for analog circuit design.

While the model is physics based, it is not predictive and relies on fitting to TCAD or other device simulators. Readers should recognize that the gate tunneling model introduced here is valid for devices where the gate is substantially on the drain, and the gate leakage flows to the drain. It does not comprehend effects of gate–source overlap. Similarly, the noise model should be recognized as an entry-level model for exploring the limitations imposed by noise in TFET circuits.

<table>
<thead>
<tr>
<th>$V_{TH}$ [V]</th>
<th>Gate leakage</th>
<th>$V(s)$ [mV]</th>
<th>$V(im)$ [mV]</th>
<th>$V$(out) [mV]</th>
<th>$V(bp)$ [mV]</th>
<th>$I(R_S)$ [fA]</th>
</tr>
</thead>
<tbody>
<tr>
<td>No leakage</td>
<td>106.0</td>
<td>106.0</td>
<td>343.1</td>
<td>394.1</td>
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<td>-246.4</td>
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<td>108.5</td>
<td>134.0</td>
<td>394.1</td>
<td>-246.4</td>
<td>-246.4</td>
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<tr>
<td>No leakage</td>
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<td>405.6</td>
<td>497.8</td>
<td>394.1</td>
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<tr>
<td>With leakage</td>
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<td>405.7</td>
<td>485.0</td>
<td>394.1</td>
<td>-4.570</td>
<td>-4.570</td>
</tr>
</tbody>
</table>

**REFERENCES**


benchmarking of tunnel FETs.


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ALAN SEABAUGH received the Ph.D. degree in electrical engineering from the University of Virginia, Charlottesville, VA, USA, in 1985.
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Dr. Seabaugh received the Symposium on Compound Semiconductors Quantum Devices Award in 2011 for seminal contributions and leadership in semiconductor devices and circuits based on quantum mechanical tunneling.
E.1 Supplementary information for universal charge-conserving TFET SPICE model incorporating gate current and noise

The complete model equations describing the DC model, the gate leakage model, the charge model and the noise model and the model parameters are provided. For a description of the DC model, refer to [1]. Figure A.1 shows the equivalent circuit of the modeled tunnel FET.

\[ I_D = I_{DT} + I_{DA} + I_{DR} \] (1)

E.1.1 Drain-source tunneling current

The drain-source tunneling current is described by
\[ I_{DF} = a f V_T \xi \exp \left( -\frac{b \xi}{\xi} \right) \]  
(2)

where

\[ a = \frac{W_{CH} q^3}{8 \pi^2 h^2} \sqrt{\frac{2 m_R^*}{E_G}} \]  
(3)

\[ b = \frac{4 \sqrt{2 m_R^* E_G}}{3 q h} . \]

The \( f \) function is given by

\[ f = \frac{1 - \exp \left( -\frac{V_{DSE}}{\Gamma} \right)}{1 + \exp \left( \frac{V_{THDS} - V_{DSE}}{\Gamma} \right)} . \]  
(4)

where \( V_{THDS} \) is the drain threshold voltage, defined as

\[ V_{THDS} = \lambda \tanh(\kappa_1 V_{GO} + \kappa_0) \]  
(5)

and \( \Gamma \) is a saturation shape parameter given by

\[ \Gamma = \Gamma_1 V_{GO} + \Gamma_0 . \]  
(6)

Eq. (5) and (6) have been modified from the original equations in [1, 2] to improve the fitting of the output characteristics at low \( V_{DS} \).

The tunneling window is given by

\[ V_{TW} = U \ln \left[ 1 + \exp \left( \frac{V_{GS} - V_{TH}}{U} \right) \right] , \]  
(7)

where \( U \), the Urbach factor, is

\[ U = \gamma_0 U_0 + (1 - \gamma_0) U_0 \left( \frac{V_{GSE}}{V_{TH} - V_{OFF}} \right) \]  
(8)

\[ U_0 = n_1 k_B T_0 / q . \]

where temperature parameter \( T_0 \) is a constant fixed at room temperature. Therefore, parameter \( U_0 \) has no temperature dependence. To avoid confusion with the parameter \( n \) in (14), \( n \) in (8) is denoted \( n_1 \).
The electric field is defined by

$$\xi = \xi_0 (1 + \gamma_1 V_{DSE} + \gamma_2 V_{GSE})$$ \hspace{1cm} (9)

In the implementation, effective gate-source voltage, $V_{GOE}$, is used instead of $V_{GS}$, which is defined as

$$V_{GOE} = V_{MIN} \left( 1 + \frac{V_{GO}}{2V_{MIN}} + \sqrt{\text{DELT}A^2 + \left( \frac{V_{GO}}{2V_{MIN}} - 1 \right)^2} \right)$$ \hspace{1cm} (10)

where

$$V_{GO} = V_{GS} - V_{OFF}$$ \hspace{1cm} (11)

Similarly, effective drain source voltage is defined as

$$V_{DSE} = V_{DSMIN} \left( \frac{V_{DS}}{2V_{DSMIN}} + \sqrt{\text{DELT}A^2 + \left( \frac{V_{DS}}{2V_{DSMIN}} - 1 \right)^2 - \sqrt{\text{DELT}A^2 + 1} } \right)$$ \hspace{1cm} (12)

Ambipolar drain-source tunneling current

$$I_{DA} = s \cdot I_{DT} (-V_{GS} + 2V_{OFF}, V_{DS})$$ \hspace{1cm} (13)

Esaki tunneling drain-source current

$$I_{DR} = -Wt_{CH} \left( -J_p \frac{V_{SDE}}{V_p} KV_{GOE} \exp \left( 1 + \frac{-V_{SDE} + \eta V_{GS}}{V_p} \right) \right)$$

$$+ J_s \left( \exp \left( \frac{V_{SDE}}{n_2 kT/q} \right) + 1 \right) \right).$$ \hspace{1cm} (14)

where parameter $n_2$ is the same as $n$ in [1, 2] and $V_{SDE}$ is the effective source-drain voltage,

$$V_{SDE} = V_{DSMIN} \left( \frac{V_{SD}}{2V_{DSMIN}} + \sqrt{\text{DELT}A^2 + \left( \frac{V_{SD}}{2V_{DSMIN}} - 1 \right)^2 - \sqrt{\text{DELT}A^2 + 1} } \right)$$ \hspace{1cm} (15)
Unlike $T_0$ in (8), $T$ in (14) is a variable, the same as in the ideal diode equation. Because there is no temperature dependence in the tunneling current, the model does not support temperature analysis. The simulating temperature should be fixed at room temperature.

E.1.2 Gate leakage current

The gate leakage current is modeled by

$$I_G = I_{G0}CN\exp\left[-T_{PHY}\frac{B_G}{V_{GDE} + V_{EGE}}\sqrt{2m_{ox}m_0}\left(1 - A_{POWE}^{3/2}\right)\right]$$  \hspace{1cm} (16)

where constants are defined as

$$I_{G0} = n_0WLA_G$$  \hspace{1cm} (17)

$$A_G = \frac{q^2}{8\pi h\kappa\epsilon_0\phi_B}$$  \hspace{1cm} (18)

$$B_G = \frac{8\pi}{3h}(q\phi_B)^{3/2}$$  \hspace{1cm} (19)

and $C$ and $N$ are

$$C = \frac{V_{GD}}{T_{PHY}}\exp\left[\frac{20}{\phi_B}\left(1 - \frac{V_{GDE} + V_{DG}}{\phi_B}\right)\left(\frac{V_{GDE} + V_{DG}}{\phi_B}\right)^\alpha\right]$$  \hspace{1cm} (20)

$$N = \frac{\kappa\epsilon_0}{T_{PHY}}\left[u_{0G}\ln\left(1 + \exp\left(-\frac{V_{GD} - V_{OFFG}}{u_{0G}}\right)\right) + u_{AG}\ln\left(1 + \exp\left(-\frac{V_{GD} - V_A}{u_{AG}}\right)\right)\right]$$  \hspace{1cm} (21)

where the parameters are defined as follows

$$u_{0G} = n_T k_BT_0/q$$  \hspace{1cm} (22)

$$u_{AG} = n_A k_BT_0/q$$

and effective $V_{GD}$ and $V_{DG}$ are used.
\begin{align}
V_{GDE} &= V_{MIN} \left[ 1 + \frac{V_{GD}}{2V_{MIN}} + \sqrt{\text{DELTA}^2 + \left( \frac{V_{GD}}{2V_{MIN}} - 1 \right)^2} \right] \tag{23} \\
V_{DGE} &= V_{MIN} \left[ 1 + \frac{V_{DG}}{2V_{MIN}} + \sqrt{\text{DELTA}^2 + \left( \frac{V_{DG}}{2V_{MIN}} - 1 \right)^2} \right] \tag{24}
\end{align}

and \( A_{POWE} \) is defined as

\begin{align}
A_{POWE} &= A_{MIN} \left[ 1 + \frac{A_{POW}}{2A_{MIN}} + \sqrt{\text{DELTA}^2 + \left( \frac{A_{POW}}{2A_{MIN}} - 1 \right)^2} \right] \tag{25}
\end{align}

and

\begin{align}
A_{MIN} &= 10^{-6} \\
A_{POW} &= 1 - \frac{V_{GDE} + V_{DGE}}{\phi_B} \tag{26}
\end{align}

E.1.3 Charge model

The drain charge \( Q_D \) is modeled by

\begin{align}
Q_D &= W_L \frac{\kappa \epsilon_0}{T_{PHY}} \left\{ -A_{DQ} \ln \left[ 1 + \exp \left( \frac{V_{GSE} - B_{DQ}}{A_{DQ}} \right) \right] + C_{DQ} V_{GSE} + D_{DQ} \right\} \tag{27}
\end{align}

where fitting parameters are defined as

\begin{align}
A_{DQ} &= A_{D1} V_{DS} + A_{D2} \tag{28} \\
B_{DQ} &= B_{D1} V_{DS} + B_{D2} \tag{29} \\
C_{DQ} &= C_{D1} V_{DS} + C_{D2} \tag{30} \\
D_{DQ} &= D_{D1} V_{DS} + D_{D2} \tag{31}
\end{align}

The source charge \( Q_S \) is modeled by

\begin{align}
Q_S = \frac{1}{\left( \frac{1}{Q_{SP}^{MQS}} + \frac{1}{Q_{SN}^{MQS}} \right)^{1/MQS}} \tag{32}
\end{align}
where parameter $MQS = 13$, and $Q_{SP}$ is defined as

$$Q_{SP} = -WL \frac{\kappa E_0}{T_{PHY}} \left\{ A_{SQ} \ln \left[ 1 + \tanh(B_{SQ} V_{GSE} + C_{SQ}) \right] + D_{SQ} V_{GSE} + E_{SQ} \right\}$$

$$A_{SQ} = A_{S1} V_{DS} + A_{S2}$$

$$B_{SQ} = B_{S1} V_{DS} + B_{S2}$$

$$C_{SQ} = C_{S1} V_{DS} + C_{S2}$$

$$D_{SQ} = D_{S1} V_{DS} + D_{S2}$$

$$E_{SQ} = E_{S1} V_{DS} + E_{S2}$$

$Q_{SN}$ is defined as

$$Q_{SN} = -WL \frac{\kappa E_0}{T_{PHY}} \left\{ A_{SQN} \ln \left[ 1 + \tanh(B_{SQN} V_{GSE} + C_{SQN}) \right] + D_{SQN} V_{GSE} + E_{SQN} \right\}$$

$$A_{SQN} = A_{S1N} V_{DS} + A_{S2N}$$

$$B_{SQN} = B_{S1N} V_{DS} + B_{S2N}$$

$$C_{SQN} = C_{S1N} V_{DS} + C_{S2N}$$

$$D_{SQN} = D_{S1N} V_{DS} + D_{S2N}$$

$$E_{SQN} = E_{S1N} V_{DS} + E_{S2N}$$

The gate charge is calculated from the charge neutrality equation

$$Q_g = -(Q_D + Q_s)$$

Fixed capacitances are described by

$$C_{FD} = C_{FDW} \cdot W$$

$$C_{FS} = C_{FSW} \cdot W$$

$$C_{GBE} = C_{GBEW} \cdot W$$

$$C_{GDE} = C_{GDEW} \cdot W$$

$$C_{GSE} = C_{GSEW} \cdot W$$
\[ C_{SBE} = C_{SBEW} \cdot W \] (51)

E.1.4 Noise model

The noise model is modeled by

\[ I_{DSN}^2 = I_{SN}^2 + I_{FN}^2 \] (52)

where the shot noise is modeled by

\[ I_{SN}^2 = 2qI_D \] (53)

and the flicker noise and RTN noise are modeled by

\[ I_{FN}^2 = \frac{K}{f^{\text{ef}}} \] (54)

The complete set of model parameters of the GaN/InN TFET with their values and units are listed below in alphabetical order in Table E.1.

### TABLE E. 1

**UNIVERSAL TFET MODEL PARAMETERS FOR THE GaN/InN TFET DESCRIBED IN THE PAPER**

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<td>0.21722</td>
</tr>
<tr>
<td>$E_{S2}$</td>
<td>Stored charge parameter</td>
<td>V</td>
<td>0.057985</td>
</tr>
<tr>
<td>$E_{S2N}$</td>
<td>Stored charge parameter</td>
<td>V</td>
<td>0.09701</td>
</tr>
</tbody>
</table>

**Fixed capacitances parameters**

| $C_{DBEW}$ | Extrinsic drain-bulk capacitance per unit gate width | F/$\mu$m | 0 |
| $C_{FDW}$ | Fringe gate-drain capacitance per unit gate width | F/$\mu$m | 0.5f |
| $C_{FSW}$ | Fringe gate-source capacitance per unit gate width | F/$\mu$m | 0.5f |
| $C_{GBEW}$ | Extrinsic gate-bulk capacitance per unit gate width | F/$\mu$m | 0 |
| $C_{GDEW}$ | Extrinsic gate-drain capacitance per unit gate width | F/$\mu$m | 0 |
| $C_{GSEW}$ | Extrinsic gate-source capacitance per unit gate width | F/$\mu$m | 0 |
| $C_{SBEW}$ | Extrinsic source-bulk capacitance per unit gate width | F/$\mu$m | 0 |

**Noise parameters**

| $EF$ | Noise frequency exponent | - | 1.0 |
| $K$ | $S_{ns}$ at 1 Hz | $A^2\text{Hz}^{EF-1}$ | 1E-18 |
E.1.5 References
