CdSe NANOWIRE FIELD-EFFECT TRANSISTORS

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Abstract

by

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We report the fabrication and characterization of single and network of CdSe nanowire (NW) field-effect transistors (FETs). The NWs are grown by the Solution-Liquid-Solid (SLS) technique and are on an average 10 nms in diameter and few microns in length.

Back gating is employed to fabricate FETs. Electrical contacts are defined to network of NWs by photolithography while E-beam lithography (EBL) and Focussed Ion Beam (FIB) methods are employed to contact single NWs that act as channels of the FETs. Fabrication of NW FETs, with problems encountered and possible solutions to the problems are discussed in detail.

Individual CdSe NWs are found to be very resistive with current levels in a few pAs for few volts of applied bias. Pronounced photoconductivity is observed in the presence of visible light with current levels increasing from a few pAs to 100s of pAs for single NWs and a few nAs to few µAs for network of NWs.

Field effect characterization indicates n-type unintentional doping of CdSe NWs. In dark, turn-on to turn-off current ratios between 10 and $10^3$ for single NWs and between $10^3$ and $10^6$ for network of NWs FETs have been realized.

Under optical illumination, current increment from over 10 to $10^3$ as gate bias is changed from +40V to -30V is observed for single NW FETs while current...
increment from over 10 to $10^6$ is observed for network of NWs FETs as gate bias varies from +10V to -10V. Loss of gate control under optical illumination is observed for both single and network of NWs.

Our NW FETs show high photoconductivity which makes them suitable for NW based optical sensing.
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CHAPTER 1
INTRODUCTION AND MOTIVATION

Integrated Circuit (IC) technology constitutes an unprecedented revolution in today’s society. Most inventions, [1] like the loom and the steam engine, are labor-saving devices. Other inventions, like the telescope improve people’s ability to comprehend their universe. They extend the senses. But IC technology simply goes about its business in a different, less visible way. ICs are at the heart of all electronic equipment today that have revolutionized the way we live: computers, navigational systems, pocket calculators, industrial monitoring and control systems, digital watches, digital sound systems, word processors, communications networks, and innumerable others. Few of these devices would exist, or would not work as reliably, without IC.

The properties that encourage the wide use of ICs are their small size and reliable performance. Nearly 40 years ago, Intel co-founder Gordon Moore had forecast the rapid pace of IC technology. His prediction, popularly known as Moore’s Law states that the transistor density on an IC doubles about every two years. Even today, the semiconductor industry continues to follow Moore’s Law, which has led to increased functionality, performance and a decrease in costs. One of the most important factors that has made it possible is scaling of device features such as the gate length of a MOSFET. The gate length has been scaled from 1µm in early 80’s to less than 0.1µm in late 90’s (Figure 1.1). Recently, Intel
Corporation has built fully functional SRAM (Static Random Access Memory) chips using 65 nanometer (nm) technology [2].

As the MOSFET gate lengths enter the nanometer regime, however, short channel effects (SCEs) such as threshold voltage ($V_{th}$) rolloff and drain-source punch-through become increasingly significant [3]. They limit the scaling capability of planar bulk or SOI (silicon-on-insulator) MOSFETs. At the same time, the relatively low carrier mobility, saturation velocity, and other material parameters of Si (compared with other semiconductors) may also degrade the MOSFET device performance (e.g. saturation current and intrinsic device delay). Further, traditionally devices are fabricated by the top-down approach in which small features are carved out of big pieces of materials. However, fabricating very small, nanosized devices put a lot of constraints on tools such as lithography.

An alternative approach is the bottom-up approach to make devices. For the above mentioned reasons, various novel device structures and materials are being
explored, among the most popular being carbon nanotube FETs [4], nanowire transistors [5] and molecular transistors [6]. These novel devices, owing to their nanoscale size, have physics quite different from conventional larger devices. Hence, they not only have conventional electronics and photonics applications but are ideal for exploring new quantum effect based devices. In the following section we describe some of the novel structures which are being researched currently.

1.1 Nanostructures

**Nanocrystals**: Nanocrystals (Figure 1.2) are aggregates of anywhere from a few hundred to tens of thousands of atoms that combine into a crystalline form of matter known as a *cluster*, as shown in Figure 1.2 [7]. Typically around

![Figure 1.2. TEM of CdSe nanocrystal.](image)
ten nanometers in diameter, in nanocrystals, carriers are confined in all three dimensions and therefore exhibit physical and chemical properties different from bulk devices. Given that a nanocrystal is virtually all surface and no interior, its properties can vary considerably as the crystal grows in size. Nanocrystals are being explored for several applications like biological sensing [8]. Size-controlled optical emission is also under study.

**Nanotubes**: Carbon nanotubes (CNT) are fullerene-related cylindrical structures. They are simply graphite sheets wrapped seamlessly onto themselves to form graphite cylinders (as shown in Figure 1.3 [9]) of a few nanometers in diameter (on the order of one ten-thousandth the width of a human hair) and up to few microns in length.

Figure 1.3. Schematic of single-wall carbon nanotubes showing that the tubes are sheets of graphene that are rolled up into seamless cylinders.
There are two types of carbon nanotubes [9]. One is called single-wall nanotube, or SWNT containing only one-atom-thick layer of graphite (called graphene). The other type of CNT are multi-wall nanotubes, or MWNTs which is a group of concentric SWNTs with smaller SWNTs placed inside larger SWNTs. After growth, CNTs can be either metallic or conducting due to which separating them is an issue. This is a potential problem from a device application viewpoint. Many devices have been demonstrated from CNTs such as FETs [10], tunnel barriers [11], Atomic Force Microscope (AFM) tips [12], etc.

**Nanowires:** Semiconducting nanowires have in the last decade become an extensively researched field because, like other novel structures (CNTs, molecular transistors), they provide natural scaling. More importantly, nanowires are much easier to fabricate and can be designed to be either metallic or semiconducting, as opposed to CNT’s. Several kinds of nanowires, made of different material systems (such as Si [13], Ge [14], GaAs [15], InP [16] etc.), have been grown using different mechanisms (such as Vapor-Liquid-Solid VLS technique [13],[15], [16] and electrochemical deposition [14]). Many room temperature applications have been demonstrated such as nanowire based FETs, diodes and logic gates, using both p-type and n-type nanowires [17], [18], [19]. Optical properties of various nanowires have been studied [20].

### 1.2 CdSe Nanowires

In the present work, we report the realization of field effect devices where the channel is formed by CdSe NWs. We chose to work on CdSe NWs because of the following reasons:

- CdSe NWs can be grown by the Solution-Liquid-Solid (SLS) technique.
This is different from the conventionally used technique, Vapor-Liquid-Solid (VLS) which was first developed by Wagner and Ellis in the mid 60’s [21].

- CdSe NWs can be branched. Branched nanowires are expected to show optical and electrical transport properties that are not only size- but also shape-dependent.

- CdSe is a direct bandgap semiconductor and expected to show strong photoconductivity.

We discuss each of the aforementioned points in the following sections.

1.2.1 Solution-Liquid-Solid(SLS) technique

Figure 1.4 shows the set-up required for the synthesis of NWs by SLS technique. Details of synthesis are mentioned in [22]. Here we give a brief outline of the growth.

In the solution-based approach, Bi nanoparticles with diameters between 1.5 and 3 nms are used to catalyze the nanowire growth. Both Bi particles and a common Se precursor (trioctylphosphine selenide, TOPSe) are mixed in a glove box and are then rapidly introduced into a solution containing fatty acid coordinated Cd ions. A rapid color change is observed, indicating a reaction between the Cd and Se ions. Nanowire growth is achieved by the presence of the metallic catalyst particle, which promotes crystallization exclusively along the \(<111>\) and \(<0001>\) directions of the zincblende and wurtzite phases of CdSe respectively. This asymmetric crystallization, in turn, leads to the creation of CdSe nanowires with varying lengths and shapes.

Typical VLS wire diameters are on the order of 20nm whereas the SLS grown CdSe NWs are on an average 10nm or lower. (refer to Figure 1.5).

The exciton Bohr radius is the natural physical separation in a crystal between an electron in the conduction band and the hole it leaves behind in the valence
band. The size of this radius controls how large a crystal must be before its energy bands can be treated as continuous. Therefore, the exciton Bohr radius can rightly be said to define whether a crystal can be called a semiconductor quantum dot/wire, or simply a bulk semiconductor. Since the exciton Bohr radius of CdSe is 5.6nm, these NWs (which are on an average 10nms in diameter) are capable of exhibiting quantum confinement effects in both optical and electrical properties. Also, solution based preparation is cost effective and has quick turn-around times. Typical cost per reaction is 5 dollars, which should be compared to the instrumentation and maintenance costs of Molecular-Beam-Epitaxy (MBE) and Chemical- Vapor-deposition (CVD) based VLS approaches. Reactions can be
conducted from beginning till end in about 1 hour, allowing rapid prototyping. Hence, the SLS technique provides an attractive alternative for nanowire growth.

1.2.2 Branched nanowires

Using the SLS technique, fascinating geometrical structures of nanowires have been demonstrated recently [22], [23]. Figure 1.6 shows branched NWs that have been synthesized by SLS technique.

Such solution-grown branched and hyper-branched NWs are expected to exhibit potentially interesting optical and electrical transport properties that are
not only size- but also shape-dependent.

1.2.3 CdSe: Material properties

Data shown in table 1.1 has been taken from National Compound Semiconductor Roadmap (NCSR) website [24].
TABLE 1.1
MATERIAL PARAMETERS FOR CdSe (BULK).

<table>
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<td>Crystal Structure</td>
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<tr>
<td>Density</td>
</tr>
<tr>
<td>Electron mobility (at 300K)</td>
</tr>
<tr>
<td>Electron effective mass (at 300K)</td>
</tr>
<tr>
<td>Bandgap (at 300K)</td>
</tr>
<tr>
<td>Lattice constant</td>
</tr>
<tr>
<td>Relative Dielectric constant</td>
</tr>
</tbody>
</table>

\(m_o^* = 9.1 \times 10^{-31} \text{ kg}\)

Note that CdSe can also exist in the zinc blende structure, having slightly different material properties [24].

CdSe is a direct bandgap semiconductor material (Figure 1.7), irrespective of its crystal structure. Hence as for the case of bulk, CdSe nanowires too are expected to show strong photoconductivity.

From literature, the bulk bandgap of CdSe is \(E_g = 1.75 \text{ eV}\). Note that due to confinement, the bandgap of a nanowire is more than that of bulk [25]. The change in bandgap \(\Delta E_g\) is a strong function of NW diameter \((\Delta E_g \propto 1/d^2)\). So, the bandgap of a CdSe nanowire is more than 1.75 eV. Visible light has wavelengths between 400-700 nms which correspond to an energy range of 2-3 eVs (more than CdSe nanowire bandgap). Hence, like in bulk, visible light has sufficient energy to excite electrons from the valence band to the conduction band in CdSe nanowires.
CdSe nanowires are, therefore, expected to show strong photoconductivity under optical illumination with visible light. Figure 1.8 shows the absorption spectra of CdSe NWs showing both absorption and emission close to the bandgap.

Because of the aforementioned points, we study CdSe nanowires. The aim is to realize field effect devices where the channel is formed by SLS grown CdSe nanowires. Based on the transport measurements, we have attempted to characterize the properties of the nanowires.
The work in this thesis is organized as follows: In chapter 2, we describe the principle of operation of the device structure fabricated and the processing steps involved in making the FETs where the channel is formed with a network and single NWs. In chapter 3, we report and discuss the measurements performed on the fabricated devices. We then discuss the problems and possible solutions to those problems in fabricating nanowire devices. Finally, we summarize the work and discuss future work in chapter 4.
CHAPTER 2

FABRICATION AND MEASUREMENTS

The concept of a field-effect transistor (FET) was first proposed by Lilienfeld (1930) [3]. The device operates as a capacitor with one plate serving as a conducting channel between two ohmic contacts-source and drain contacts. The other plate-the gate-electrostatically controls the charge flowing in the channel. The carriers enter the channel from the source and move across the channel into the drain. This basic principle has been implemented in a variety of devices, such as Metal Oxide Semiconductor Field Effect Transistor (MOSFET), Junction Field Effect Transistor (JFET), Metal Semiconductor Field Effect Transistor (MESFET), Heterostructure FETs (HFETs) [26] etc.

This chapter is devoted to nanowire FET’s. We begin with the description of the device structure followed by the fabrication steps involved.

2.1 Device Structure

Figure 2.1 shows the device structure we have employed for CdSe NW FETs.

The FET channel is formed by the NWs (single/network). The basic idea is to make ohmic contacts to NWs and then modulate the current through NWs by a control gate which is separated from the NWs by an insulator. To realize such a device for CdSe NWs, two important steps are of concern.
Figure 2.1. Figure showing the NW FET device structure. As shown, CdSe NWs form the channel of the device. Back gating is used to modulate channel (i.e. nanowire) current.

- Control gate
- Contacts to NWs

We discuss each of them in detail below.

2.1.1 Control gate

The first important concern is to fabricate a control gate to modulate current through the NW channel. In the literature, three types of gating techniques have been demonstrated for nanowires, as shown in figure 2.2[27].
Our aim is to realize a field-effect device with a simple device structure. Back gating is chosen primarily to demonstrate functional devices using CdSe NWs. A back gate is easy to fabricate and requires fewer steps as compared to top or coaxial gating. Therefore, we employ back gating technique to make our devices. However, it results in poor gate control as compared to the other two techniques. This happens because when the back gate voltage is applied, electric field lines are not localized to the device under test. In the future, we aim to improve device performance by using top/coaxial gating techniques.
2.1.2 Contacts to nanowires

For good FET performance, both source and drain metal-semiconductor junctions should form ohmic contacts with the channel (in our case, nanowires). Ideally, an ohmic contact has linear current-voltage characteristic and a very small resistance that is negligible compared with the resistance of the active region of a semiconductor device. From the theory of metal-semiconductor junctions, an ohmic contact can be formed between a metal and semiconductor by either highly doping the semiconductor so that electrons can tunnel through the barrier or by choosing a metal whose work function ($\phi_m$) is lower than a semiconductor, as shown in figure 2.3.

Heavy doping of CdSe nanowires to make ohmic contacts is currently not feasible by the Solution-Liquid-Solid (SLS) growth technique. Hence, we choose a metal whose work function is less than that of CdSe. Assuming that the CdSe is nominally undoped, the work function of CdSe is expected to be roughly $\phi_s \sim 5.5\text{eV}$ (refer to figure 2.3). Al has a work function $\phi_m = 4.5\text{eV}$. Hence, Al is expected to form an ohmic contact with CdSe NWs, assuming the absence of any traps (surface or interface states) at the metal-semiconductor interface.

Please note that, as discussed in Section 1.2.3, by assuming the bandgap of CdSe nanowires to be the same as that of bulk i.e. 1.75eV, we underestimate its value. Hence $\phi_s \sim 5.5\text{eV}$ (which is equal to the sum of electron affinity $\chi$ and $E_g/2$, as shown in the figure) is lower than the actual value, which is dependent upon the wire diameter. Once the metal has been chosen, the next concern is the process to make contacts to nanowire (single/network). Contacts to single and network of NWs requires different processing steps. We discuss them in detail now.
Figure 2.3. Figure showing metal (Al)-semiconductor (CdSe) junction. Note that there is no barrier for electrons at the junction, thereby forming an ohmic contact.

Contacts to a network of NWs:
NWs arrange randomly on the Si/SiO₂ substrate as shown in figure 2.4. They form a connected network and a current is observed to flow through the network, presumably in a percolative fashion.

As discussed in Section 1.2.1, the NWs are prepared in solution. The density of wires can be controlled by varying the concentration of NWs in the solution. To make contacts to a network of wires, a dense solution is ideal. Our CdSe NWs, on an average, are few microns in length, therefore source-drain contact pad with a separation of 3µms is considered sufficient for making contacts to NWs. Further, we choose interdigitated patterns, as shown in figure 2.5 to enhance the chance of
making contacts to NWs.

Figure 2.5. Mask design used for making contacts to a network of NWs by photolithography.

Contacts to single NWs:

We have attempted making electrical contacts to single NWs using Electron Beam Lithography (EBL). Devices were also made by using a dual-beam scanning elec-
tron microscope/focused ion beam (SEM/FIB) system (FEI Strata DB235) at the University of Texas at Austin. We discuss both the methods in this section.

Electron Beam Lithography (EBL): EBL is performed on an Amray 1400, 50 kV SEM (converted for EBL applications). To make contacts to single NWs, the first step is to locate a single NW with respect to some markers on the surface. The design (for EBL) is made so as to easily determine NW coordinates relative to markers. We used the mask design shown in Figure 2.7 for optical lithography.

Since the NWs are few µms in length, the markers have to be closely spaced. Our design has 8 markers of dimension 10×10µm² which are 5µms apart from the adjacent ones. 4 markers are connected to (100 × 100 µm²) contact pads and

Figure 2.6. Figure showing the Amray 1400, 50 kV SEM used for electron beam lithography. A student is also shown working on the Amray.
Figure 2.7. Mask design used for making contacts to single NWs by EBL.

through EBL, lines are drawn to make contacts from these pads to NWs. Markers also help in doing alignment, necessary for doing EBL using Amray.

We used the Hitachi S4500 FESEM (Field Emission Scanning Electron Microscope) for imaging NWs. Once the position of a nanowire with respect to a marker is determined, a design file is made using NPGS (Nanometer Patter Generating Software) and EBL is carried out to define electrical contacts to NWs.

Process to make a mask

- Mask design is made in L-Edit.
- Design is converted to the machine readable format (GDS) and then sorted using GDSvII and PGSORT, respectively.
- Design is printed on an emulsion plate by exposing it in Mann 3000. It is then developed in PD85 for 20-25s, rinsed in DI for 60s, fixed in 'fixer' for 2-3min and then rinsed in DI water.
- Chrome plate is made in GCA 3696 using the emulsion plate. It is then developed in AZ327 for 20-25s and rinsed in DI for 1 min. Chrome from the
plate is then etched in ‘chrome etchant’ for 90s and finally rinsed in DI for 1min.

- Chrome plate is finally air dried. Excess photoresist is removed by keeping mask in Drytech for 20min.

Focussed-Ion-Beam (FIB): Electrical contacts to single CdSe nanowires were made by writing 100nm wide Pt lines between NWs and Au contact pads. Pt electrodes were written with a 30 keV beam at 10pA beam current.

![Figure 2.8. Dual-beam scanning electron microscope/focused ion beam (SEM/FIB) system (FEI Strata DB235).](image)

The sample with NWs on the surface is viewed under FIB and upon locating a NW, lines are defined between the NW and the contact pads. Then, Pt metal is deposited on the line defined in the FIB system. Hence, unlike EBL, FIB doesn’t involve the use of MMA/PMMA to do lithography. It also cuts down an extra step of metal deposition and lift off as required in EBL.

However, one limitation of FIB is that *cross-talk* can take place between two Pt lines if closely spaced. As shown in figure 2.9, cross-talk results due to the Pt
ions that are deposited across the line defined by FIB. Because of cross-talk, even if a contact is made to a nanowire, conduction is mainly through the Pt ions and hence, a metallic behavior is observed. In order to ensure there is no cross-talk between Pt lines, contacts were defined on NWs with length more than 4µms.

2.1.3 Device physics

In this section we try to understand the device operation of CdSe NW FETs with the aid of band diagrams.

Using conventional MOSFET theory, we can characterize our nanowire FET in the following manner. As for a conventional metal-semiconductor interface [26], the CdSe nanowire bands bend (up for p-type; down for n-type) at the
interface, to bring the NW Fermi level in line with that of the metal contacts. When $V_g > 0$, the bands are lowered, which depletes the holes in p-type NW and suppresses conductivity, but leads to an accumulation of electrons in n-type NWs and enhances the conductivity. Conversely, $V_g < 0$ will raise the bands and increase the conductivity of p-type NWs and decrease the conductivity of the n-type NWs. Hence, we can determine the carrier type (n/p type) by observing the change in conductivity with changing gate bias. Apart from the carrier type, from gated measurements we can estimate the carrier mobility in the NWs. The carrier mobility $\mu$ in the NW is related to the transconductance $g_m$ of the FET by the relation [28]

$$\mu = \frac{g_m L^2}{CV_{sd}},$$

(2.1)

where $L$ is the gate length (equal to the NW length), $V_{sd}$ is the source-drain
bias, and C is the capacitance of the wire given by the following expression

\[ C = \frac{2\pi \varepsilon \epsilon_0 L}{\ln\left(\frac{2t_{ox}}{r}\right)}, \quad (2.2) \]

where \( \varepsilon \) is the dielectric constant of CdSe = 10.2, \( t_{ox} \) is the oxide thickness and \( r \) is the nanowire radius.

The transconductance \( g_m \) can be obtained from the \( I_{ds} \) vs \( V_{gs} \) plot by using the relation

\[ g_m = \frac{\partial I_{ds}}{\partial V_{gs}}|_{V_{ds}} \quad (2.3) \]

at a fixed \( V_{ds} \) in the linear region.

Hence, the carrier mobility in a NW can be roughly estimated.

2.2 Device Fabrication

The process flow for fabricating network and single nanowire FETs is shown in figures 2.11 and 2.12, respectively.

We start with a 4” oxidized p-type Si wafer. The oxide thickness is 225nm.

(a) Solvent Clean: The wafer is first cleaned in acetone and then in Iso-Propyl Alcohol (IPA) for 5 mins each. It is then blow dried in \( N_2 \).

(b) Wet etching in HF: The front surface is coated with 1813 photoresist to prevent the surface oxide from etching. The wafer is then etched in BHF until the back oxide is etched away (Note: The oxide is completely etched away once DI water stops sticking to the surface). Then the wafer is rinsed in DI water and blow dried in \( N_2 \).

(c) Back-gate metal deposition: Using the e-beam metal evaporator, 10/200nm thick Ti/Au is deposited on the back of the wafer, typically at a rate of 2/5 Å/s
at a chamber pressure less than $2 \times 10^{-6}$ torr. After metal deposition, photoresist is stripped off from the front surface by keeping the sample in acetone and IPA for 5 mins. (Sometimes, sample has to be kept in Drytek for 30s for complete removal of the photoresist).

At this stage, the fabrication step differs for a network or single NWs.

2.2.1 Contact to network of NWs

For the case of network of NWs,

(d) **Putting down Nanowires:** The solution containing NWs is dropped over the sample and air dried. The density of nanowires can be controlled by varying
a. Solvent clean  
b. Wet-etch in HF  
c. Back-gate metal deposition  
d. Source-Drain lithography  
e. Source-Drain metal deposition  
f. Put down nanowires  

If EBL, then  
g. Image wires  
h. EBL, metal deposition, lift off  

If FIB, then  
g. FIB

Figure 2.12. Process flow showing steps involved to fabricate single NW FETs.
the concentration of the solution. To make contacts with a network of NWs, a concentrated solution is preferred.

(e)**Source-Drain lithography:** A dehydration bake is done at 120°C for 5 min. Then, HMDS (Hexamethyldisilazane) followed by 5214 photoresist is spun over it at 5000 rpm for 30s each. Soft bake is done at 90°C for 60s. Contact lithography is then carried out on Karl Suss MJC contact aligner using the mask shown in figure 2.5.

The following recipe is used to do contact lithography in a Karl Suss MJB contact aligner.

- Edge bead Removal.
- Expose to UV light with dose of 125mJ/cm².
- Reverse Bake at 110°C for 60sec.
- Expose to UV light with dose of 250mJ/cm².
- Develop in AZ327 for 30sec, wash in DI water, observe the features under microscope and develop as necessary.

(f)**Source-Drain Metal Deposition:** 10/200 nm thick Ti/Au is then deposited on the sample typically at a rate of 2/5 Å/s respectively, by the e-beam evaporator at a chamber pressure lower than 2×10⁻⁶ torr. This is followed by lift off in acetone for few minutes and cleaning in IPA and DI water.

At this stage, the device is ready for measurements.

2.2.2 Contacts to single NWs

For the case of contacts to single NWs:

(d)**Source-Drain lithography:** Dehydration bake is done at 120°C for 5 min. Then, HMDS followed by 5214 is spun over it at 5000 rpm for 30s each. A soft bake is
done at 90°C for 60s. Contact lithography is then carried out on Karl Suss MJC contact aligner using the mask shown in Figure 2.7.

The following recipe is used to do contact lithography in Karl Suss MJB contact aligner.

- Edge bead Removal.
- Expose to UV light with dose of 125mJ/cm$^2$.
- Reverse Bake at 110°C for 60s.
- Expose to UV light with dose of 250mJ/cm$^2$.
- Develop in AZ327 for 30s, observe under microscope and develop as necessary.

The sample is then washed in DI water and blow dried.

(e)Source-Drain Metal Deposition: 5/50nm thick Ti/Au is then deposited on the sample typically at the rate 2/5 Å/s respectively, by the e-beam evaporator at
a chamber pressure lower than $2 \times 10^{-6}$ torr. This is followed by lift off in acetone for few minutes and cleaning in IPA and DI water.

(f) *Putting down NWs:* The solution containing NWs is then dropped over the sample and air dried. Typically, it takes few minutes for the solution to dry up. However, for good imaging under SEM, sample needs to be dried for couple of hours. The density of NWs can be controlled by varying the concentration of the solution. The more dilute the solution is the less is the number of NWs. refer to figure 2.14.

![Figure 2.14](image.png)

Figure 2.14. Figure showing NW networks formed upon drop-casting of a (a) dense solution, and (b) dilute solution of NWs.

Upon drying, NWs are observed to stick to the substrate; this is believed to be due to Van Der Waals forces [29]. Surfactants (or ligands) around the SLS-grown NWs also help in adhesion to the surface.

(Note: SEM/AFM images confirm that the NWs adhere well to the substrate even after doing process steps like lithography, developing, lift off etc.)
At this stage, the process flow for making single NW contacts with EBL and FIB differs.

For contacts with EBL:

(g) Imaging of nanowires:

As we discussed in Section 2.1.3, the position of the NWs is determined by imaging them under SEM. Images are taken of the NWs that can be found near the markers (Figure 2.15). Based on these images, a design file is made so as to make contact with optically defined source-drain contact pads by electron beam lithography (EBL).

(h) EBL: MMA (methyl methacrylate) is spun on the sample at 4500 rpm at 30s and is baked at 170°C for 2 min. Then, PMMA (polymethylmethacrylate)
is spun at 4500 rpm at 30s followed by baking at 170°C for 3 min. This gives a double layer resist thickness of 200nm. EBL is then carried out in the Amray with a beam current of 10pA (and working distance 10mm). This is followed by developing in (Methyl Isobutyl Ketone: Iso Propyl Alcohol) MIBK:IPA (3:1) for 40s and then washing in IPA. 40nm thick Al is deposited by the e-beam evaporator, typically at a rate of 2Å/s. This is followed by lift off in acetone for few minutes, and washing in IPA and DI water.

Figure 2.16 shows four electrical contacts made to a single NW which is 4µms in length.

![Figure 2.16. SEM image showing electrical contacts defined to a single NW by EBL.](image)

Several attempts have been made to make contacts to single NWs. However, since NWs tend to stick to each other, many times contacts were made to more than one nanowire as shown in the figure 2.17.
Locating nanowire under SEM
Contacts made by EBL to the nanowire imaged
Upon zooming, more nanowires are seen to be contacted

Figure 2.17. SEM images showing attempts made at making contacts to single NWs.
For contacts with FIB:

(g) FIB: The sample with nanowires on the surface is inserted into the chamber of the FIB system. NWs are located and a design file is made to define a line between NW and the contact pads. Then, Pt metal is deposited along the line defined in the chamber itself. Figure 2.9 shows contacts made to a nanowire by FIB.

At this stage, the device is ready for measurements. It was observed that devices (both single and network) lost their conductivity over time. Freshly prepared devices showed conduction between only those pads that are connected by NWs (confirmed by AFM/SEM). However, conductivity between pads was observed to reduce over time. Reasons for the loss of conduction are unclear, but it was observed that if the devices are coated with PMMA, they retained their conductivity. Hence, reproducible results were obtained on samples coated with PMMA. (Note: We believe possible surface reaction to be the reason for the loss of conductivity.)
CHAPTER 3

RESULTS AND DISCUSSIONS

In this chapter, we first report the electrical and photoconductivity measurements conducted on nanowire FETs and discuss them in detail. We then report the problems faced in making nanowire FETs and how we expect to solve them in the future. Finally, we mention some future applications of the NW based devices.

3.1 Current-Voltage Measurements

The basic measurement setup is shown in Figure 3.1.

The probe-station is a Cascade Summit 11861. The electrical probes are either ceramic or tungsten tipped. For our devices, the probe is placed on two metal pads - the source and drain contacts while the chuck on which the sample rests forms the back gate contact. These terminals are connected to an Agilent 4155B semiconductor parameter analyzer by guarded-triaxial cables with a current resolution of 50fA.
3.2 Nanowire FET Measurements

The CdSe NW field effect devices were first used for two terminal measurements by keeping the gate floating. A voltage bias is applied between source-drain contacts and the current measured between the same. Current conduction is observed between only those contact pads that are connected by NWs.

Figure 3.2 shows the typical current-voltage plot obtained for the case of (a) network and (b) single NWs. Measurements were done for ∼10 devices for the network of NWs while 2 for single NWs. While only few pAs of current flows for ±2.5V of applied bias for single NWs, 1000s of pAs of current flows for the same range of applied bias for network of NWs.

For some of the devices, we obtained asymmetric current-voltage curves as shown in Figure 3.3. This asymmetry can be attributed to the asymmetric contacts to the NWs (i.e. possibly the metal-semiconductor barrier heights are dif-
Figure 3.2. Current-Voltage plot for (a) network of nanowires (b) single nanowire. Measurements are done in dark, at room temperature.

Figure 3.3. Non-linear current-voltage plot obtained for some of the devices.
ferent for the two contacts to nanowires).

Photoconductivity measurements were done with visible light (source being the microscope lamp). For CdSe NWs, we observe pronounced photoconductivity even with visible light. In Figure 3.4, a typical current-voltage curve obtained in the presence of light is shown. Current amplification in the presence of light as compared to dark current is observed for all devices, though the amplification factor differs from device to device.

![Figure 3.4. Plot of $I_{ds}$ vs $V_{ds}$ in the presence of light for network of NWs.](image)

Figure 3.4 shows the change in current through the device as the intensity of light is slowly increased. Field effect characterization of the devices were done using back gating, as shown in the setup discussed in Section 3.1. For devices with a network of NWs, measurements done in the dark show modulation of channel current $I_{ds}$ by varying gate voltage $V_{gs}$ with channel turning off as gate bias is
made negative. Figure 3.5[a] shows $I_{ds}$ vs $V_{gs}$ for a network of NW FET, with $V_{ds}$ fixed at 1V. For the plot shown in Figure 3.5(a), turn on to turn off current

$\text{Ratio} = \frac{I_{\text{light}}}{I_{\text{dark}}} > 10^3$

$\text{Subthreshold slope} \approx 400 \text{mV/dec}$

Table 3.1 gives the measurement results for 10 different network of NWs FETs. As listed in the table, the nanowire FETs show on-off current ratios between $10^3$ and $10^6$ which are comparable to the best nanowire FETs demonstrated so far by other groups using VLS grown NWs. [30], [31]. Mobilities are low, an average value can be estimated to be $1 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ based on classical MOSFET theory.

Figure 3.5. Plot showing $I_{ds}$ vs $V_{gs}$ for (a) network (b) single NWs in dark and in presence of light. $V_{ds}$ is fixed at 1V.
TABLE 3.1
MEASUREMENT RESULTS FOR NETWORK OF
NANOWIRES FIELD-EFFECT TRANSISTORS.

<table>
<thead>
<tr>
<th>Device No.</th>
<th>$V_{sd}$(V)</th>
<th>$V_{th}$(V)</th>
<th>$I_{on}/I_{off}$</th>
<th>$g_m$(nS)</th>
<th>$\mu$ (cm$^2$V$^{-1}$s$^{-1}$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>-5</td>
<td>$10^4$</td>
<td>0.875</td>
<td>0.245</td>
</tr>
<tr>
<td>2</td>
<td>1</td>
<td>-6</td>
<td>$10^3$</td>
<td>6.495</td>
<td>1.82</td>
</tr>
<tr>
<td>3</td>
<td>1</td>
<td>-8</td>
<td>$10^4$</td>
<td>21</td>
<td>5.88</td>
</tr>
<tr>
<td>4</td>
<td>1</td>
<td>-10</td>
<td>$10^4$</td>
<td>1.465</td>
<td>0.41</td>
</tr>
<tr>
<td>5</td>
<td>1</td>
<td>-7</td>
<td>$10^5$</td>
<td>1.22</td>
<td>0.34</td>
</tr>
<tr>
<td>6</td>
<td>1</td>
<td>-4</td>
<td>$10^4$</td>
<td>0.0945</td>
<td>0.026</td>
</tr>
<tr>
<td>7</td>
<td>1</td>
<td>-5</td>
<td>$10^6$</td>
<td>11.1</td>
<td>3.1</td>
</tr>
<tr>
<td>8</td>
<td>1</td>
<td>-7</td>
<td>$10^3$</td>
<td>6.772</td>
<td>1.9</td>
</tr>
<tr>
<td>9</td>
<td>2</td>
<td>-5</td>
<td>$10^6$</td>
<td>37.3</td>
<td>5.22</td>
</tr>
<tr>
<td>10</td>
<td>2</td>
<td>-3</td>
<td>$10^3$</td>
<td>2.995</td>
<td>0.42</td>
</tr>
</tbody>
</table>

Figure 3.6 shows $I_{ds}$ vs $V_{gs}$ for different $V_{ds}$ for a network of NWs. As $V_{ds}$ is increased from 1V to 9V, the threshold voltage becomes more negative (increases from $\sim$-2V to $\sim$-8V). The subthreshold slope remains almost the same ($\sim$1V/dec). Measurements for single NW FETs were done on 2 devices. Table 3.2 gives the measurement results for both. For single NW devices, characteristics similar to that of network of NWs are observed. Channel current modulation with gate bias is observed with the channel turning off with a negative gate bias. Figure 3.5(b) shows $I_{ds}$ vs $V_{gs}$ for $V_{ds}$ fixed at 30V. We see a low subthreshold slope ($\sim$few V/dec) for our devices. Though devices don’t reach saturation in the on
Figure 3.6. Plot showing $I_{ds}$ vs $V_{gs}$ with varying $V_{ds}$ for a network of NWs.

**TABLE 3.2**

MEASUREMENT RESULTS FOR SINGLE NANOWIRES FIELD-EFFECT TRANSISTORS.

<table>
<thead>
<tr>
<th>Device No.</th>
<th>$V_{sd}$(V)</th>
<th>$V_{th}$(V)</th>
<th>$I_{on}/I_{off}$</th>
<th>$g_m$(pS)</th>
<th>$\mu$ (cm$^2$V$^{-1}$s$^{-1}$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>30</td>
<td>-30</td>
<td>10</td>
<td>0.0897</td>
<td>$9.5 \times 10^{-7}$</td>
</tr>
<tr>
<td>2</td>
<td>30</td>
<td>-10</td>
<td>$10^3$</td>
<td>0.0119</td>
<td>$1.26 \times 10^{-7}$</td>
</tr>
</tbody>
</table>

state, on-off current ratios can be roughly estimated to be $\sim 10$ and $10^3$ for the two devices.

Figure 3.5(a),(b) also show $I_{ds}$ vs $V_{gs}$ in the presence of optical illumination. Under optical excitation, for both network and single NW devices, we observe a weakening of gate control over the channel current. As the gate bias is varied from a positive to a negative value, the current increment ratio increases from $\sim 10$ to $10^6$ for network of NWs and from $\sim 10$ to $10^3$ for single NW devices.
Temperature dependent measurements were done on many devices (network FETs). Figure 3.7 shows $I_{ds}$ vs $V_{ds}$ for different temperatures while $I_{ds}$ vs $V_{gs}$ with varying temperatures is shown in Figure 3.8.

As shown in Figure 3.7, $I_{ds}$ increases from 3 nAs to 45nAs as temperature is increased from 40°C to 100°C. Please note that we have shown currents for only those temperatures that are consistent with device physics, as discussed later in the section.

![Figure 3.7. $I_{ds}$ vs $V_{ds}$ for three different temperatures. Increment of $I_{ds}$ with increasing temperature is observed.](image)

In Figure 3.8, the modulation of $I_{ds}$ with varying $V_{gs}$ with $V_{ds}$ fixed at 5V is shown. An increment in threshold voltage (roughly from -2V to more than -10V) is observed as the temperature is increased from -20°C to 100°C. The subthreshold slope shows a monotonic decrease with temperature. This is interesting, since
Figure 3.8. Plot showing temperature dependent $I_{ds}$ vs $V_{gs}$.

theoretically, it is expected to increase with increasing temperature [3]. For several devices, both single and networked, we have observed hysteresis as gate bias is swept from negative to positive voltages and vice-versa. Figure 3.9 shows a typical hysteresis curve for network NW FETs. The measurement is done (in dark) by sweeping the gate bias from -10V to 20V and then from -20V to 20V. Hysteresis is observed for both sweeping voltages.

Another observation during gated measurements is that the threshold voltage depends upon the starting voltage of the sweep, though subthreshold slope and on-off current ratios were independent of the starting voltage of the sweep. As is shown in figure 3.9, for the same device, the channel turns on with $V_{th} \sim -8V$ if starting voltage is -10V. But, it turns on at $\sim -15V$ if starting voltage is -20V.
3.3 Electrical Characterization

In this section, we discuss the results reported in the previous section.

3.3.1 Multiple and single nanowires

From Figure 3.2, it is clear that SLS grown NWs are very resistive. Assuming a linear curve, we can roughly estimate single NW resistance to be of the order of $10^{12}$ Ω which is very high as compared to resistance of other nanowires reported in literature as shown in table 3.3.
TABLE 3.3
COMPARISON OF RESISTANCES OF CdSe, Si AND Ge NANOWIRES.

<table>
<thead>
<tr>
<th>Type</th>
<th>Order of Current</th>
<th>Order of $V_a$</th>
<th>Order of R (in ohms)</th>
<th>Reference</th>
</tr>
</thead>
<tbody>
<tr>
<td>CdSe</td>
<td>pAs</td>
<td>10s of volts</td>
<td>$10^{12}$</td>
<td>Present Work</td>
</tr>
<tr>
<td>Si</td>
<td>100s of nAs</td>
<td>10s of volts</td>
<td>$10^8$</td>
<td>[32]</td>
</tr>
<tr>
<td>Ge</td>
<td>few nAs</td>
<td>10s of volts</td>
<td>$10^9$</td>
<td>[32]</td>
</tr>
</tbody>
</table>

We believe this is because during (SLS) growth we don’t dope the NWs. As a result, any carriers in the nanowires are either thermally generated or are due to the presence of impurities. But owing to a large bandgap, the number of thermal carriers is low (order of $10^3 \text{cm}^{-3}$)

$$n_i = \sqrt{N_c N_v} \exp(-\frac{E_g}{2kT}) \sim 10^3 \text{cm}^{-3}. \quad (3.1)$$

We expect current conduction to be mainly due to the presence of impurities. Impurity concentration, for a 3 $\mu$m long (L) wire with radius $r=10$ nms, resistance $R \sim 10^{12}$ $\Omega$ and mobility $\mu \sim 650 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$, can be roughly estimated to be $\sim 10^{12}\text{cm}^{-3}$ by using the bulk-like approximation.

$$n_d = \frac{L}{qR\mu A} = \frac{3 \times 10^{-4}}{1.6 \times 10^{-19} \times 10^{12} \times 650 \times \Pi(5 \times 10^{-7})^2} \sim 10^{12}\text{cm}^{-3}. \quad (3.2)$$

At this stage, an important concern is the effect of surface states on the transport. This is because for NWs, the surface to volume ratio is quite large as shown
from the following equations.

For a (cylindrical) nanowire with length $l$ and diameter $d$,

$$\frac{\text{Surface Area}}{\text{Volume}} = \frac{\pi dl}{\pi \frac{d^2}{4} l} = \frac{4}{d} \quad (3.3)$$

We now try to estimate the ratio of density of bonds on surface to that in volume. To simplify our calculations, we assume a cubic crystal structure with bond length $a \, \text{Å}$ as shown in figure 3.10

![Figure 3.10. Figure showing cylindrical nanowire with cubic crystal structure.](image)

Volume density of bonds can be estimated in the following manner:
Volume of each unit cell \((v_r) = a^3\),

Total volume \((V_r) = \pi \frac{d^2}{4} l\),

There are 12 bonds in a cubic unit cell, each bond shared between 4 unit cells. So, bonds per unit cell \((bc) = 12/4 = 3\).

Hence, volume density of bonds \((V_b) = \frac{V_r}{v_r} \times bc\)

\[
= \pi \frac{d^2 l}{a^3} \times 3 \tag{3.4}
\]

Surface density of bonds can be estimated in the following manner:

Area of each edge \((a_r) = a^2\),

Total surface area \((A_r) = \pi d l\),

On the surface, there are 4 bonds in a cell, each bond shared between 2 cells. So, bonds per crystal \((bc) = 4/2 = 2\).

Hence, surface density of bonds \((S_b) = \frac{A_r}{a_r} \times bc\)

\[
= \frac{\pi dl}{a^2} \times 2 \tag{3.5}
\]

Ratio of number of bonds on surface to that in volume can be roughly estimated as,

\[
\frac{S_b}{V_b} = \frac{8a}{3d}. \tag{3.6}
\]

Hence, the surface state density is expected to be high for NWs. Assuming \(a \sim 5 \text{ Å} \) and \(d \sim 100 \text{ Å}\), the ratio is 13% which is quite high. If electrically active, a large fraction of charge transfer can occur through the surface states. This can hinder the characterization of NWs. One way to determine the dominant mode of charge transfer (surface or NW) is by conducting absorption/emission spectra. Figure 1.8 shows the absorption/emission spectra for CdSe NWs. From
the figure, strong absorption is seen when the energy of incoming photons is more than 1.75 eV. Similarly, strong emission is observed for energies around 1.75eV. Since strong absorption and emission is observed near the bandgap of CdSe, we conclude that the transport of carriers is through the NWs and not through surface states (surface to conduction band).

We observed pronounced photoconductivity for CdSe NWs even with visible light, as shown in figure 3.4. As discussed above, we can assume transitions from valence to conduction band (neglecting surface states). CdSe is a direct semiconductor and visible light has sufficient energy to excite electrons from valence band to conduction band, thereby increasing the number of carriers and hence, current through NWs increases. This is the reason for the strong photoconductivity.

3.3.2 Field-effect characterization

Figure 3.5 shows the channel current modulation with gate bias for both network and single NW FETs. The plots are typical of a normally-on, n-type FET, with the channel turning off for negative gate bias. Hence, we conclude our NWs are unintentionally n-doped.

From tables 3.1 and 3.2, we observe that the transconductance of all devices (network and single) are low and threshold voltages are high. This performance can be attributed to the presence of a thick oxide layer ($t_{ox} \sim 225\text{nm}$). Further, the source-drain metal contacts are not perfectly ohmic, which also leads to poor device performance.

For a network NWs FETs, mobilities are of the order of few cm$^2$V$^{-1}$s$^{-1}$, while for single NW FET, they are of the order of $10^{-7}$cm$^2$V$^{-1}$s$^{-1}$ which is very low. These values have been obtained by using the classical device theory, as stated in
section 2.1.3. However, if we assume the mobility is of the order of $10^{-7}$ cm$^2$V$^{-1}$s$^{-1}$ (from Table 3.2), then to get the resistance of the order of $10^{12}$ ohms of the channel, we need a carrier density of $10^{22}$ cm$^{-3}$ (from equation 3.2) which is very high for a nanowire. We currently don’t clearly understand the reason for such low mobilities. One reason can be the classical theory approach to determine mobility value. Transport in CdSe nanowires is not well understood and classical transport assumption is not necessarily correct. Scattering can also be one of the reason for low mobilities. Surface roughness might be important since these NWs are of very small diameters.

Figure 3.6 shows $I_{ds}$ vs $V_{gs}$ for varying $V_{ds}$. The characteristics are similar to a short channel n-type device. This is because we observe (almost) parallel shift in the curves for different $V_{ds}$. This means that though the subthreshold slope is the same, the threshold voltage increases with increasing $V_{ds}$ [3]. This happens because for a short channel device, the threshold voltage is inversely proportional to the gate length and varying $V_{ds}$ changes the effective gate length. Increasing $V_{ds}$ decreases the effective gate length and therefore, threshold voltage increases. Subthreshold slope, on the other hand, depends strongly on temperature and increases with increasing temperature [3].

Figures 3.8 and 3.7 show temperature dependent measurements on NW FETs. As the temperature is increased, the number of thermal carriers in the channel (NWs) increase exponentially. Hence, the channel current $I_{ds}$ increases with increasing temperature. Further, more carriers in the channel require higher gate bias to turn off the channel and hence, threshold voltage also increases, as is also obtained from Figure 3.8. However, from the figure 3.8, subthreshold slope decreases as temperature is increased which is contrary to the theory according to
which subthreshold slope should increase with increasing temperature. The reason for this behaviour has not been investigated yet.

Figure 3.9 shows a typical hysteresis curve for a networked NW FET as the gate bias is swept from negative to positive voltages and vice-a-versa. Further, a shift in the threshold voltage is also observed as the starting voltage is changed. The reason for both, hysteresis and changing threshold voltage, is believed to be trapped charges in CdSe-SiO$_2$ interface. It can be reduced by reducing the gate thickness, which currently stands at 225nms.

3.4 Fabrication Issues: Problems and Solutions

In this section, we discuss the problems faced in fabricating NW FETs. We also suggest some solutions to those problems.

3.4.1 Misalignment during EBL

Position of the NWs are determined with respect to the markers. Based on this, a design file is made in NPGS. However, because of misalignment, many times contacts to single NWs could not be achieved. Some of the missed contacts are shown in figure 3.11.

Misalignment can be because of the following reasons:

- **Movement of NWs on the substrate due to processing**
  NWs, once dropped on the substrate, remain on the substrate. This is confirmed by the images taken before and after processing. However, movement of NWs on the substrate during processing is believed to be a possibility. This problem is intrinsic to NWs and hence, cannot be completely removed. However, its effect on doing EBL can be reduced by careful design of CAD file.

- **Bad alignment during EBL**
  On Amray (to do EBL), stage control knobs (X,Y) have a minimum resolu-
Figure 3.11. SEM image showing missed contacts to a nanowire made by EBL.

tion of 5µms each. Hence, a single turn of these knobs will move the stage by at least 5µms in the corresponding direction. Due to this, not always perfect alignment is possible in Amray. Its affect on making contacts to NWs can also be minimized by careful design of CAD file.

- **Stage stability during imaging and/or during exposure**
  This happens because of backlash and drift of the stage on which the sample rests. Stage stability is easily characterized by simply going to a high magnification, moving the stage, and measuring the drift versus time. For a given design, the requirement depends on the feature size and the writing time. For example, if a pattern consisting of 0.1µm lines takes 1 minute to write, a stage drift of 20 nm/minute would probably be acceptable. Alignment in Amray should be carried out once the drift is in acceptable range.

- **Error in determining the coordinates of the NWs**
  (Figure 3.12) Coordinates of the NWs are determined with respect to edges of the markers (metal pads) on the surface. If edges of the markers are not sharp, but rounded, then the NW coordinates cannot be accurately determined. This problem can be avoided by ensuring that the edges of the markers are sharp.

### 3.4.2 Imaging nanowires by SEM

As we discussed in Section 2.2.2, Hitachi S4500 FESEM is used to locate NWs. Owing to the dimension of the NWs (10 nm in diameter and few microns
in length), imaging of NWs requires the electron beam to be well conditioned.
Two important factors that must be considered are listed below:

- **Astigmatism**
  For good imaging (and also for lithography), the electron beam needs to be well rounded (in shape). Astigmatism is the condition in which the beam is elliptical in shape. For good imaging of NWs, it is required that astigmatism should be removed at high magnification (~100kx). If astigmatism is bad then NWs, even if present on the substrate, cannot be viewed under the microscope.

- **Charging**
  While imaging, it is commonly observed that the region being imaged gets charged up (Figure 3.14).

  The reasons for charging up are use of excessive beam current, high accelerating potential and also a large condenser spot or a huge final aperture. This may result in the introduction of excess charges in NWs and can also damage its surface. Charging is unavoidable, but can be reduced significantly if the amount of energy and the number of electrons hitting the surface is reduced. This is done by using a lower accelerating potential and lower beam current, with a smaller condenser spot. However, this can significantly reduce the resolution and may so happen that the feature being imaged is not visible clearly.
Figure 3.13. SEM image (a) before and (b) after EBL. More number of NWs visible after EBL. Astigmatism in the imaging before EBL is the primary reason for the difference.

Figure 3.14. SEM image showing charging in NW samples.
3.4.3 Locating single nanowires

For locating single NWs, a solution with appropriate concentration (which decides the density of NWs on the substrate) needs to be used, as mentioned in section 2.2. However, it is observed that NWs tend to stick to each other and hence, isolating a single NW poses a great challenge. Further, for increasing the chance to obtain single NWs, the solution has to be very dilute. It usually leads to wastage of pads (since there are no NWs in between the pads). Hence, currently, there is no proper procedure to image single NWs which are well distributed between all the pads.

3.4.4 Current conduction in devices

It was observed that current conduction between pads varied with time. While freshly prepared samples gave reasonable current conduction, but with time, conduction reduced and usually, gave no conduction (just noise) after a few days. Though reason for the loss of conduction is unclear, we expect possible surface reaction at NW surface which leads to loss of conduction. We coated the samples with PMMA, so as to avoid exposure of NW surface to air. Uncoated samples showed degradation of conduction with time while samples coated with PMMA gave reproducible properties even after long periods (months).
CHAPTER 4

CONCLUSIONS AND FUTURE WORK

We have reported the fabrication and characterization of single and network of CdSe nanowire (NW) field-effect transistors (FETs). CdSe NWs, grown by Solution-Liquid-Solid (SLS) technique are, on an average, 10 nms in diameter and few microns in length.

FETs, where NWs act as the channel, were fabricated by employing a backgating technique. Electrical contacts were defined to a network of NWs by photolithography while E-beam lithography (EBL) and Focussed Ion Beam (FIB) methods were employed to contact single NWs.

Measurements indicate that SLS grown CdSe NWs are very resistive, with current levels in few pAs for few volts of applied bias. It is believed to be due to the absence of any doping during growth technique. Pronounced photoconductivity is observed in the presence of visible light with current levels increasing from few pAs to 100s of pAs for single NWs and few nAs to few µAs for network of NWs. This was expected since CdSe is a direct bandgap material.

Field effect characterization indicates n-type unintentional doping of CdSe NWs. In dark, turn-on to turn-off current ratios between 10 and $10^3$ for single NWs and between $10^3$ and $10^6$ for network of NWs FETs were obtained.

Under optical illumination, current increment factors from 10 to $10^3$ as gate bias is changed from +40V to -30V was observed for single NW FETs while current
increment factors from 10 to $10^6$ was observed for network of NWs FETs as gate bias varies from +10V to -10V. Loss of gate control under optical illumination is observed for both single and network of NWs. Without even attempting for device optimization, our NW FETs show high photoconductivity which makes them suitable for NW based optical sensing.

In the future, we would attempt to improve device performance by using thin gate oxide and employing better gating techniques (like top/coaxial gating). Contacts to NWs can be made easier by aligning the NWs on the substrate. Nanowire alignment is being researched by many groups by techniques like applying electric field [33] or micro-fluidic means [34]. We intend to align CdSe NWs by applying electric field. Some preliminary work has been done, as shown in the figure 4.1.

Figure 4.1. Figure showing nanowires aligned between two electrodes on a glass substrate. AC field is applied between the two electrodes.
Further, we intend to explore quantum effects in branched nanowires. As stated in section 1.2.2, branched nanowires are expected to show confinement effects which are both size and shape dependent. A Y-branch switch (YBS) is one such quantum effect based device [35], [36]. Using heterostructures, YBS have been demonstrated [37], [38]. However, processing of such a device is tedious and limited by lithographic tools and etching. In the future, we aim to fabricate YBS from branched NWs which provides a natural alternative to fabricate YBS, as is shown in figure 4.2.

![Diagram showing the top-down and bottom-up approaches to fabricate YBS. As illustrated, bottom-up approach, where branched NWs are used to fabricate YBS, involves fewer processing steps than top-down approach, where heterostructures are used to fabricate YBS.](image-url)
BIBLIOGRAPHY


