DEFECTS IN EMERGING III-V MATERIALS FOR ELECTRONIC AND OPTOELECTRONIC APPLICATIONS

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Abstract

by

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Deep level traps in two emerging classes of devices, InGaAs/GaAsSb multiple quantum well (MQW) photodiodes for mid-IR detection and GaAs-based MOSFETs using InAlP native oxide and Al₂O₃ as gate dielectrics for microwave-frequency circuit applications, are studied using several characterization techniques, with an eye towards using this information in order to further improve device performance.

For the InGaAs/GaAsSb MQW photodiodes, several device structures, including lattice-matched MQWs, conventional layer-by-layer strain-compensated MQWs, and a strained MQW, were evaluated. Three samples with unstrained and strain-compensated structures have been characterized using low frequency noise spectroscopy (LFNS), random telegraph signal (RTS) characterization, and deep level transient spectroscopy (DLTS). Several deep levels were observed in these structures; some of the defect levels were found to be common to all structures, while others are unique to specific device structures. These distinctions can provide guidance for the design of improved MQW photodiodes. In addition, detailed DLTS study was used to identify the spatial location of
the identified defects; this study indicates that one of the traps is actually located in the transition layer outside the quantum well region, thereby highlighting the importance of considering the full device structure – and not just the “active” layers – during device design. Additionally, a novel quantum well photodiode with a strained active region was also investigated. This structure is attractive since it is promising for extending the detection range to longer wavelengths. Two new deep levels were found in this novel structure, and were found to be located in the strained quantum well region by using DLTS. This study has provided the first detailed investigation of the trapping/detrapping mechanisms at work in these photodiodes.

To facilitate the study of defects in GaAs-based MOSFETs, MOS capacitors incorporating two different gate oxides were investigated. InAlP oxide was first studied for the advantage of its easy integration to current GaAs FET fabrication process. Although high-performance devices have been obtained, an interface state density ($D_{it}$) in the range of $10^{12}$-$10^{13}$ eV$^{-1}$cm$^{-2}$ was typically extracted for these structures, imposing a practical limit on subthreshold performance of the devices. As an alternative to InAlP oxide, Al$_2$O$_3$ deposited by atomic layer deposition was also evaluated. A “buried channel” approach with an InGaP layer between the dielectric and channel was used to reduce the impact of defects on device performance. A range of surface pretreatments and post-deposition annealing treatments were investigated in order to optimize the interface quality. The $D_{it}$ was found to be somewhat lower than for InAlP oxide, on the order of $\sim 10^{12}$ eV$^{-1}$cm$^{-2}$. The lower interface state density, coupled with the larger dielectric constant of Al2O3 compared to InAlP oxides, suggests this is a promising path for improved microwave device performance.
CONTENTS

LIST OF FIGURES .......................................................................................................... iv

LIST OF TABLES ............................................................................................................. ix

ACKNOWLEDGMENTS .................................................................................................. x

CHAPTER 1. INTRODUCTION ......................................................................................... 1
  1.1 Deep level defects in semiconductors ............................................................... 1
  1.2 Methods of characterizing deep levels ............................................................ 3
  1.3 Dissertation overview .................................................................................... 4

CHAPTER 2. EXPERIMENTAL METHODS ................................................................ 6
  2.1 Deep level transient spectroscopy (DLTS) ....................................................... 6
    2.1.1 Capacitance transient ........................................................................... 6
    2.1.2 Quantitative analysis of capacitance transient ..................................... 10
    2.1.3 Conventional DLTS .......................................................................... 12
    2.1.4 Computer DLTS ................................................................................ 14
  2.2 Low frequency noise spectroscopy (LFNS) and Random Telegraph Signal (RTS) characterization ................................................................. 16
    2.2.1 Basic description of noise in devices ................................................... 16
    2.2.2 Mathematical description of low frequency and RTS noise ............... 21
  2.3 MOS Interface trap density characterization ................................................. 24
    2.3.1 Capacitance-voltage method .............................................................. 24
    2.3.2 Conductance method .......................................................................... 27

CHAPTER 3. DEEP LEVEL CHARACTERIZATION IN INGAAS/GAASSB QUANTUM WELL PHOTODIODES ........................................................................ 30
  3.1 Introduction on InGaAs/GaAsSb quantum well photodiodes ....................... 30
  3.2 Deep level characterization of In$_{0.53}$Ga$_{0.47}$As and GaAs$_{0.5}$Sb$_{0.5}$ homojunction and heterojunction test samples using LFNS and RTS ....... 32
  3.3 Deep level characterization of unstrained and strain-compensated InGaAs/GaAsSb multiple quantum well photodiodes ............................................. 40
    3.3.1 IV characteristics of unstrained and strain-compensated MQW photodiodes ................................................................................................. 46
    3.3.2 LFNS and RTS characterization of unstrained and strain-compensated MQW photodiodes ................................................................. 48
    3.3.3 Discussion of deep levels in unstrained and strain-compensated MQW photodiodes obtained from LFNS and RTS .................. 55
3.3.4 DLTS characterization of unstrained and strain-compensated InGaAs/GaAsSb quantum well photodiodes ..........................................................57

3.4 Deep level characterization of strained-well InGaAs/GaAsSb quantum well photodiode ........................................................................................................66

3.4.1 IV characteristics of the strained-well InGaAs/GaAsSb quantum well photodiode ...............................................................................................69

3.4.2 LFNS characterization of the strained-well InGaAs/GaAsSb quantum well photodiode .................................................................................70

3.4.3 DLTS characterization of the strained-well InGaAs/GaAsSb quantum well photodiode .................................................................................73

3.5 Summary of deep level characterization of InGaAs/GaAsSb photodiodes 77

CHAPTER 4. INTERFACE STATE CHARACTERIZATION IN GAAS-BASED MOS STRUCTURES USING INALP OXIDE AND AL₂O₃ AS GATE DIELECTRIC ...79

4.1 Brief review of GaAs FETs ....................................................................79

4.2 InAlP oxide as gate dielectric ................................................................81

4.2.1 Fabrication of MOS capacitors using InAlP oxide as gate oxide ....81

4.2.2 Current-voltage, capacitance-voltage and conductance measurements of MOS capacitors .................................................................84

4.3 Al₂O₃ as gate dielectric ........................................................................92

4.3.1 Fabrication of MOS capacitors using Al₂O₃ as gate oxide ..........92

4.3.2 Interface quality characterization using capacitance and conductance methods .................................................................95

CHAPTER 5. SUMMARY AND FUTURE WORK .........................................................106

BIBLIOGRAPHY .................................................................................................109
LIST OF FIGURES

Figure 2.1 Time evolution of trap occupancy and carrier distribution (outer figures) and resulting capacitance transient (central figure) for a p⁺n junction. Majority carrier (e⁺) trap is illustrated here. The dotted line, hollow circles and solid circles represent the trap level, empty trap and occupied trap, respectively. Redrawn after [12] ......................................................................................................................... 9

Figure 2.2 Capacitance transients following the bias pulse for majority carrier trap (upper) and minority carrier trap (lower) in a p⁺n junction. Redrawn after [6]............. 9

Figure 2.3 Implementation of a rate window by means of a double-boxcar integrator. The output corresponds to the (average) difference of the amplitudes at the sampling times t₁ and t₂. [12]......................................................................................................................... 13

Figure 2.4 Typical DLTS signal using double integrators. Each curve represents one temperature scan, and the two peaks represent two distinct deep traps. [6] ... 14

Figure 2.5 Block diagram for computer DLTS system..................................................... 16

Figure 2.6 Typical measured low frequency noise with (a) and without (b) generation-recombination noise. ....................................................................................... 17

Figure 2.7 Energy band diagram for a semiconductor with deep-level impurities........ 18

Figure 2.8 Carrier emission and capture process for donor- and acceptor-like deep levels in n-type material, illustrating processes associated with high- and low-current states. The size of the horizontal arrows represents the current density. .... 20

Figure 2.9 Experimental setups for LFNS (a) and RTS characterization (b). ............... 21

Figure 2.10 Measured low frequency noise plot of a GaAsSb homojunction pn diode at 276.6 K. 2 Lorentzians are seen superimposed on the 1/f background noise. 22

Figure 2.11 An illustration of semi-logarithmic histogram plot of the time durations [14]. ................................................................................................................................. 23

Figure 2.12 High frequency equivalent circuit of an idealized MOS capacitor. .......... 25

Figure 2.13 Equivalent circuits for conductance measurements for determining Dᵦ in MOS capacitance. (a) MOS capacitor with interface trap time constant
\( \tau_{iT} = \text{RitCit} \), (b) simplified circuit of (a), (c) circuit model typically assumed in LCR-based measurement configurations. [13] ........................................... 28

Figure 3.1 Heterostructure diagrams of the (a) \( \text{In}_{0.53}\text{Ga}_{0.47}\text{As} \) and (b) \( \text{GaAs}_{0.5}\text{Sb}_{0.5} \) homojunctions, and (c) \( \text{In}_{0.53}\text{Ga}_{0.47}\text{As}/\text{GaAs}_{0.5}\text{Sb}_{0.5} \) heterojunction................ 32

Figure 3.2 (a) Typical measured noise spectrum and Lorentzian fit to the measured current noise spectral density \( \langle S_i \rangle \) for a typical \( \text{InGaAs}/\text{GaAsSb} \) heterostructure diode at 375 K, showing superposition of 1/f noise and G-R noise. (b) The shift in measured spectra and associated Lorentzian signatures with temperature. ............................................................. 34

Figure 3.3 Arrhenius plot for all observed traps in both homojunction and heterojunction devices............................................................................................................. 34

Figure 3.4 (a) measured noise spectral density, \( \langle S_i \rangle \), measured at 5 mV, 12 mV, and 20 mV for \( \text{GaAsSb} \) homojunction and \( \text{InGaAs}/\text{GaAsSb} \) heterojunction diodes at 250 K. (b) \( S_i \) of typical \( \text{GaAsSb} \) homojunction devices measured as a function of bias voltage, extracted at 10 Hz. ........................................................................ 37

Figure 3.5 Extracted \( K_f \) of homojunctions and heterojunction devices vs. temperature, suggesting fundamental differences in defect density and distribution, possibly at heterointerfaces between materials. ......................................................... 37

Figure 3.6 Typical measured RTS noise of a \( \text{GaAsSb} \) homojunction measured at 245 K, with bias current of 0.331 mA/cm\(^2\) (upper) and 0.194 mA/cm\(^2\) (lower). Bias dependence indicates trap E5 is donor-like. .................................................. 38

Figure 3.7 Device structures of (a) PD1, lattice matched \( \text{In}_{0.53}\text{Ga}_{0.47}\text{As}/\text{GaAs}_{0.5}\text{Sb}_{0.5} \) MQW photodiode, (b) PD2, strain-compensated \( \text{In}_{0.45}\text{Ga}_{0.55}\text{As}/\text{GaAs}_{0.4}\text{Sb}_{0.6} \) MQW photodiode, and (c) PD3, strain-compensated \( \text{In}_{0.33}\text{Ga}_{0.67}\text{As}/\text{GaAs}_{0.25}\text{Sb}_{0.75} \) MQW photodiode................................................. 41

Figure 3.8 Band alignment and wave functions for (a) PD1, (b) PD2, and (c) PD3 type II quantum wells in this study. The effective band gap decreases as local strain increases....................................................... 43

Figure 3.9 Current-voltage characteristics for typical unstrained (PD1) and strain-compensated (PD2, PD3) photodetectors, measured at several temperatures. 47

Figure 3.10 Dark current density versus inverse temperature for unstrained (PD1) and strain-compensated (PD3) devices at -0.3 V bias. The activation energy extracted from the slope of the Arrhenius plot is 0.29 eV for both devices, suggests the presence of near-mid-gap traps. ......................................................... 48

Figure 3.11 (a) Measurement and Lorentzian fit to the measured current noise spectral density \( \langle S_i \rangle \) of a strain-compensated device (PD3) at 201 K, showing superposition of 1/f noise, G-R noise and white noise, (b) The measured
Lorentzian peak shifts in frequency with temperature, indicating the carrier lifetime decreases with increasing temperature. ............................................. 49

Figure 3.12 Measurement and Lorentzian fit to the measured f*PSD of PD1 for (a) $E_{a1}$, (b) $E_{b1}$ and (c) $E_{c1}$. ................................................................. 51

Figure 3.13 Measurement and Lorentzian fit to the measured f*PSD of PD2 for (a) $E_{a2}$, (b) $E_{b2}$ and (c) $E_{c2}$. Notice that $E_{a2}$ and $E_{b2}$ are observed in the same noise spectra. ......................................................... 52

Figure 3.14 Measurement and Lorentzian fit to the measured f*PSD of PD3 for (a) $E_{a3}$, (b) $E_{b3}$ and (c) $E_{c3}$. ................................................................. 52

Figure 3.15 Arrhenius summary of traps found in three unstrained and strain-compensated MQW photodiodes using LFNS. ............................................. 53

Figure 3.16 Measured RTS noise of PD1 MQW photodiodes measured at 133 K ((a) and (b)) and 194 K ((c) and (d)) for $E_{a1}$ and $E_{b1}$, respectively. The bias dependence of low- and high-current states probability indicates trap $E_{a1}$ is donor-like and $E_{b1}$ is acceptor-like. ................................................................. 55

Figure 3.17 Measured and fitted capacitance transient for a typical strain-compensated MQW photodiode (PD3) at several temperatures........................................... 58

Figure 3.18 Arrhenius plot for traps found in unstrained and strain-compensated devices using both LFNS and DLTS. Traps in the same circles are suspected to share a common origin. ................................................................................. 60

Figure 3.19 Trap profile for $E_{a1,DLTS}$ (0.13 eV) in PD1. (a) CV characteristics, (b) carrier density profile with the corresponding the bias condition, (c) trap density as a function of bias. ...................................................................................... 63

Figure 3.20 Trap profile for $E_{a2,DLTS}$ (0.13 eV) in PD2. (a) CV characteristics, (b) carrier density profile with the corresponding the bias condition, (c) trap density as a function of bias. ...................................................................................... 64

Figure 3.21 Trap profile for $E_{a3,DLTS}$ (0.11 eV) in PD3. (a) CV characteristics, (b) carrier density profile with the corresponding the bias condition, (c) trap density as a function of bias. ...................................................................................... 65

Figure 3.22 (a) Schematic illustration of the concept for photodiodes incorporating strained MQW and compensation barrier layer that achieves zero net strain. (b) The impact of different strain on absorption wavelength. [36] ......................... 68

Figure 3.23 MBE grown quantum well photodiode heterostructure (PD4) based on the conceptual structure of Figure 3.22. 20 periods of barrier/QW/barrier structure are incorporated in the device as active region. ............................................. 68
Figure 3.24 Energy band diagram and wavefunctions for the strained type II quantum wells. ................................................................. 69

Figure 3.25 I-V characteristics of PD4. ................................................................. 70

Figure 3.26 Noise spectra for traps in novel structure. The left column shows the Lorentzian peak corresponding to the trap at 0.15 eV, and the right column shows the one at 0.26 eV. ........................................................................ 71

Figure 3.27 Traps found in the strain-well photodiodes PD4 using LFNS. ............... 72

Figure 3.28 Capacitance transient evolution with temperature for the 0.12 eV hole trap E_{1, PD4, DLTS} in PD4................................................................. 74

Figure 3.29 Hole trap found in PD4 by DLTS comparing to LFNS results. ............... 74

Figure 3.30 Trap profile for 0.12 eV trap E_{1, PD4, DLTS} in PD4. .......................... 76

Figure 4.1 Device structure of Y110 (left) and Y111 (right) wafers. ...................... 82

Figure 4.2 Schematic cross section of a MOS capacitor on the Y111 heterostructure... 83

Figure 4.3 Typical I-V characteristics measured for 40 µm * 40 µm capacitors with structures Y110 and Y111, oxidized for 16 minutes at 440 °C. ......................... 84

Figure 4.4 I-V characteristics for Y111 capacitors with oxidation times ranging from 14 minutes to 21 minutes................................................................. 85

Figure 4.5 Measured (solid line) and theoretical (dashed line) capacitance-voltage characteristics for MOS capacitors fabricated on the Y111 structure, for full oxidation (16 minutes oxidation time). ........................................... 86

Figure 4.6 Measured (solid line) and theoretical (dashed line) capacitance-voltage characteristics for MOS capacitors fabricated on the Y110 structure, for full oxidation (16 minutes oxidation time). ........................................... 87

Figure 4.7 D_{it} of Y111 structure extracted using the Terman method...................... 88

Figure 4.8 D_{it} of Y110 structure extracted using the Terman method..................... 88

Figure 4.9 Conductance map for Y111 MOS capacitor measured at 150 °C (a) and at 25 °C (b). D_{it} extracted from the conductance peaks is shown in (c). ................. 90

Figure 4.10 Conductance map for Y110 MOS capacitor measured at 150 °C (a) and at 25 °C (b). D_{it} extracted from the conductance peak is shown in (c)................. 91

Figure 4.11 Device structure of X1 wafers.............................................................. 93

Figure 4.12 Schematic cross section of a MOS capacitor on the X1 structure........... 94
Figure 4.13 Measured and theoretical C-V for MOS capacitors on structure X1 with several pre- and post-treatments. (a). no special treatment. (b). 20 mins (NH₄)₂S soaking. (c). 500 °C 30 s nitrogen PDA. (d). 20 mins (NH₄)₂S soaking + 500 °C 30 s nitrogen PDA. ............................................................. 96

Figure 4.14 I-V characteristics of four test samples ......................................................................... 97

Figure 4.15 C-V characteristics of PDA test samples based on the Taguchi method
(continued on next page)............................................................................................................. 99

Figure 4.16 C-V characteristics of PDA test samples based on the Taguchi method. ... 100

Figure 4.17 Dᵥ distribution for sample #1, #12 and #15 as determined from the Terman method......................................................................................................................... 102

Figure 4.18 Conductance map for test samples (a) #1, (b) #12, and (c) #15. Dᵥ extracted from the conductance peaks is shown in (d)................................................................. 104
LIST OF TABLES

Table 3.1 Summary of deep level characteristics in test samples................................. 39
Table 3.2 Summary of MQW trap parameters................................................................. 66
Table 3.3 Summary of strained-well quantum well photodiode (PD4) trap parameters .. 77
Table 4.1 DOE for PDA test based on the Taguchi method............................................. 98
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1.1 Deep level defects in semiconductors

Since all real-world semiconductors contain impurities and crystalline defects, it is important to understand them and their effect on device performance. In general terms, the existence of defects typically manifests itself as the presence of electronic states within the band gap. Such defect-related states in semiconductors can be broadly divided into two categories: shallow states and deep level states. Shallow states are located near band edges, and are often intentionally generated by incorporating dopant atoms in the material; for example, in GaAs if Si is incorporated at a Ga site, the extra valence electron is easily ionized, leading to the formation of n-type material. Likewise, replacing gallium with zinc acts as an acceptor to form p-type material. In contrast, deep level states are characterized by having energy states located far from the band edges (typically \( \gg kT/q \)), and these levels can be caused either by foreign atoms (either substitutional or interstitial defects) or by crystalline defects (e.g. self-interstitials, vacancies, and dislocations). The terms “trap”, “state”, and “level” are also used rather loosely and interchangeably in the literature to refer to a state within the band gap which can capture or emit carriers.

There are some additional sub-categories of deep level defects, including deep traps and generation-recombination centers. This diversity of categories and labels can
lead to confusion. Generally, we can quantitatively define these defects by comparing the carrier capture and emission rates. A deep trap has a carrier capture rate that exceeds its emission rate, and it can be an electron trap or a hole trap depending on the carrier captured. If both the electron and hole capture rates are comparable, then the deep level defect is called a recombination center. In a similar way, a generation center is defined as a state for which both electron and hole emission rates are comparable.

Deep levels can have a strong influence on device and circuit performance, even at low concentrations. Perhaps counterintuitively, the impact can be either deleterious or advantageous; in some special cases, deep levels are even necessary for the operation of a device or circuit. For example, one of the most extensively studied deep levels in GaAs is EL2, which is essential for making semi-insulating GaAs for integrated circuit substrates, since the Fermi level is pinned near the midgap by EL2. Nevertheless, deep levels are undesired in most cases, since the defects will interact with free electrons and holes, altering the device performance. For example, recombination centers in a photodetector can capture the photogenerated free carriers, reducing the quantum efficiency and responsivity of the device, while simultaneously inducing significant excess noise. Likewise, the DC, RF, and noise performance of metal–semiconductor field effect transistors (MESFETs), high electron-mobility transistors (HEMTs), and pseudomorphic high-electron-mobility transistors (PHEMTs) can also be degraded by the presence of deep level defects. For example, undesirable electrical properties such as transconductance dispersion [2], kink effect [3], hysteresis effects [4], and drain current collapse [5], have been observed and attributed to the presence of deep levels within devices or along device surfaces and interfaces. These effects promise to become ever
more significant as the industry moves aggressively to smaller feature sizes, and higher level of functional.

Therefore, it is essential to control (and typically minimize) the formation of deep levels during both material growth and device fabrication. To do this most effectively requires a fundamental understanding of the nature of deep levels, as well as their dependence on material growth conditions, structural details (such as layer thickness, composition and strain), and device fabrication and processing conditions. Assessing these factors requires the ability to quantitatively characterize deep levels within materials and devices.

1.2 Methods of characterizing deep levels

Several techniques have been developed to evaluate deep level defects. Among the most powerful is deep level transient spectroscopy (DLTS) [6] and its variations such as CTS (current transient spectroscopy) [7] and DDLTS (Double-correlated DLTS) [8]. Additional techniques that are often helpful also include low frequency noise spectroscopy (LFNS) [9], random telegraph signal (RTS) measurement [10], and admittance spectroscopy [11]. Among these methods, DLTS offers very high sensitivity and the ability to obtain detailed quantitative information about the traps that are present, including energy level, type of trap, trap density, spatial distribution, and capture cross section. However, in order to directly apply DLTS, a pn junction or similar bipolar test structure is required. Variations (such as CTS) seek to relax these constraints, but at the cost of increased complexity and loss of generality. LFNS and RTS are advantageous in some cases because they are also very sensitive, are often faster than DLTS in terms of
measurement time, and can be applied to non-junction devices. However, this comes at the expense of not being able to fully resolve the full quantitative details of the nature of the traps. For the specific case of interface traps, such as states in oxide/semiconductor interfaces, the most frequently used methods are based on capacitance-voltage measurement and conductance spectroscopy. In this work, all of these methods are employed for characterizing deep level defects in a range of compound semiconductor devices.

1.3 Dissertation overview

This work focuses on the characterization of deep levels in two promising device technologies: InP-based MQW photodiodes for mid-IR detection, and GaAs-based MOSFET structure with either InAlP oxide or ALD grown Al₂O₃ as the gate dielectric.

The dissertation is organized as follows: The fundamentals of several deep level characterization techniques are briefly introduced in Chapter 2, including DLTS, LFNS, RTS, and capacitance and conductance methods. Chapter 3 then presents details of deep level measurements performed on InP-based MQW mid-IR photodiodes. Test samples, lattice-matched, layer-by-layer strain-compensated, and strained MQW photodiodes have been measured using LFNS, RTS and DLTS, to help distinguish material-related defects. Traps have been found to have strong relationship with material composition, strain and the details of the epitaxial structures. Besides the identification and extraction of the parameters of deep levels, it will also be shown that the deep levels correlate directly to device performance as observed through the current-voltage characteristics of the devices.
The application of these techniques to GaAs MOSFETs using InAlP oxide or ALD grown Al$_2$O$_3$ as gate dielectric is discussed in Chapter 4. In this section, fabrication and defect characterization of MOS capacitors is described. The properties of interface traps have been evaluated using both capacitance and conductance methods. It will be shown that for InAlP oxide, of oxide-semiconductor interface can be as high as $10^{13}$ eV$^{-1}$cm$^{-2}$, which is about an order of magnitude higher than the previous best-case report of $8 \times 10^{11}$ eV$^{-1}$cm$^{-2}$ [1], while for Al$_2$O$_3$, the $D_{it}$ is around $\sim 10^{12}$ eV$^{-1}$cm$^{-2}$ by using proper surface treatment and annealing process, highlighting the importance of structure design and processing conditions for obtaining low defect densities.

Chapter 5 summarizes the work of defect characterization on all these devices, and also shows a future direction for possible deep level characterization of MQW photodiodes and GaAs MOSFETs.
A discussion of the key deep level characterization techniques used in this work, including DLTS, LFNS, RTS and capacitance and conductance method, is presented in this chapter.

2.1 Deep level transient spectroscopy (DLTS)

2.1.1 Capacitance transient

The underlying mechanism of DLTS relies on the use of depletion width as a measure of trap states and their occupancy in the depletion region of a junction. In DLTS, the depletion capacitance (and thus depletion width and trap occupancy) is monitored in response to changes in bias conditions. For example, in an asymmetric p⁺n junction, the depletion width $W$ (including the effect of deep levels) is related to the applied reverse bias $V$ through:

$$W = \sqrt{\frac{2\varepsilon(V_{bi}-V)}{q(N_{D}-n_{T}(t))}}$$  \hspace{1cm} (2.1)$$

where $\varepsilon$ is the dielectric constant of the material, $V_{bi}$ is the built-in voltage, $N_{D}$ is the doping carrier density for n-type material, and $n_{T}(t)$ is the occupied defect density
(assumed to be electron traps for \( n_T > 0 \)) at time \( t \). The corresponding depletion capacitance is given by

\[
C(t) = \frac{eA}{W} = A \sqrt{\frac{q\varepsilon(N_D - n_T(t))}{2(V_{bi} - V)}}
\] (2.2)

where \( A \) is the device area.

Equation (2.2) provides the relationship between capacitance and the occupied defect density. The DLTS technique is then based on quantitative analysis of measured capacitance transients in diode device structures. Thus an understanding of capacitance transients is critical to appreciate and successfully apply the DLTS technique. By analyzing in detail the time- and temperature-dependence of capacitance transients in response to step changes in bias voltage, information about defect states can be extracted.

To begin discussing capacitance transients, we consider two types of deep traps: majority carrier traps and minority carrier traps [6, 12]. A majority carrier trap (e.g., electron trap in n type material) and minority carrier trap (e.g., hole trap in n type material) have subtle differences in the effect on the junction capacitance. Figure 2.1 illustrates the response of a p⁺n diode to a bias pulse, showing the trap occupancy in the space charge region and the resulting capacitance transient, taking a majority carrier trap as an example. In this example, initially the junction is under reverse bias to establish a wide space charge region, and deep traps in the space charge region are empty of carriers because the Fermi level is below the energy of the deep level. This situation is illustrated in “Step 1” in Figure 2.1. A short pulse to zero volts is then applied, which reduces the width of the space charge region and introduces only majority carriers (electrons, in this
case) into the region that had previously been depleted. The traps then capture these majority carriers, as shown in “Step 2”. Due to the reduced space charge width, the capacitance in this period is larger, as shown in the central figure. Because the traps are filled during this interval, it is often called a “filling pulse”. The difference between the depletion regions in Step 1 and Step 2 is the region where traps are being observed. After the filling pulse, the diode bias is returned to the initial reverse bias condition. The junction capacitance will rapidly reduce due to expansion of the space charge region, but at a somewhat smaller capacitance than the steady-state value. This reduction in capacitance below the steady-state value is because the space charge region width is larger in order to compensate for the majority carriers captured by the deep traps during the filling pulse. This situation is depicted in Figure 2.1 “Step 3”. The trapped charges then gradually escape to the conduction band and are swept away from the junction region by the applied potential (shown in “Step 4”), resulting in the space charge region shrinking until it returns to the steady-state condition. The sequence described above applies to characterization of majority carrier traps. For minority carrier traps (not shown here), an injection pulse, which drives the diode slightly into forward bias and injects both majority and minority carriers into the space charge region, is used in place of the zero-bias filling pulse. In this case--if minority carrier traps are present--the junction capacitance immediately after the bias is returned to reverse will be slightly larger than the steady state value. Then, as minority carriers are re-emitted from the traps the capacitance gradually decreases to the steady-state value. This is summarized in Figure 2.2, which shows a comparison of the pulsed-bias capacitance transients associated with both majority and minority carrier traps.
Figure 2.1 Time evolution of trap occupancy and carrier distribution (outer figures) and resulting capacitance transient (central figure) for a p+n junction. Majority carrier (e\textsuperscript{+}) trap is illustrated here. The dotted line, hollow circles and solid circles represent the trap level, empty trap and occupied trap, respectively. Redrawn after [12].

Figure 2.2 Capacitance transients following the bias pulse for majority carrier trap (upper) and minority carrier trap (lower) in a p+n junction. Redrawn after [6].
2.1.2 Quantitative analysis of capacitance transient

To use DLTS to quantify the characteristics of deep levels, a mathematical model is needed. The conventional approach to modeling this is to observe that during the carrier emission process, the time dependence of occupied (electron) trap density \( n_T(t) \) can be expressed as [13]

\[
    n_T(t) = n_T(0) \exp\left(\frac{-t}{\tau_e}\right) \approx N_T \exp\left(\frac{-t}{\tau_e}\right)
\]  

(2.3)

where \( n_T(0) \) is the occupied trap density right after the pulse, \( N_T \) is the total trap density, and \( \tau_e \) is the emission time constant of the electron trap. For the approximation shown here, it is assumed that the filling pulse is of sufficient duration that all the traps in the observation region are occupied by the end of the filling pulse, and that the occupancy is well described by Boltzmann statistics.

By Taylor expansion of Equation (2.2), the capacitance transient can then be written as

\[
    C(t) = C_0 \sqrt{1 - \frac{n_T(t)}{N_{net}}} \approx C_0 \left(1 - \frac{n_T(t)}{2N_{net}}\right) \approx C_0 \left[1 - \frac{N_T}{2N_{net}} \exp\left(\frac{-t}{\tau_e}\right)\right]
\]  

(2.4)

where \( C_0 \) is the steady state capacitance at reverse bias \( V \), and \( N_{net} \) is the net shallow doping concentration, for example, \((N_D - N_A)\) in n type materials. From this expression and measured \( C(t) \) transients, the trap parameters, such as \( \tau_e \) and \( N_T \), can be extracted using numerical methods such as least-squares fitting.

To extract the trap energy, additional information is needed; the usual approach is to extract \( \tau_e \) over a range of temperatures, and use the \( \tau_e \) dependence to calculate the trap
energy. Since carrier emission from a trap is typically governed by thermionic emission, the emission time constant $\tau_e$ will have an exponential dependence on temperature, as shown in Equation (2.5) [13],

$$\tau_e = \exp\left(\frac{(E_c - E_T)/kT}{\sigma_n v_{th} N_c}\right)$$  \hspace{1cm} (2.5)

where $\sigma_n$ is the electron capture cross section, $v_{th}$ is the thermal velocity, $v_{th} = \left(\frac{3kT}{m_e}\right)^{\frac{1}{2}}$, and the effective density of states in the conduction band is $N_c = 2\left(\frac{2\pi m_e kT}{\hbar^2}\right)^{\frac{3}{2}}$. Combining these expressions for $v_{th}$, and $N_c$ with Equation (2.5) results in

$$\tau_e T^2 = \frac{\exp((E_c - E_T)/kT)}{\gamma_n \sigma_n}$$  \hspace{1cm} (2.6)

where $\gamma_n = (v_{th}/T^{1/2})(N_c/T^{3/2}) = 3.25 \times 10^{21} (m_e/m_0) \text{ cm}^{-2} \text{s}^{-1} \text{K}^{-2}$.

From this expression, one can see that an Arrhenius plot of $\ln(\tau_e T^2)$ versus $1/T$ permits extraction of the trap energy level from the slope, which is $(E_c - E_T)/k$, and the capture cross section $\sigma_n$ from the y axis intercept.

From this basic understanding, one can appreciate – at least conceptually – the ability of DLTS to provide detailed information about defect levels in semiconductors. Experimentally, there are several ways to extract this information from test devices. Two of these are discussed here: the classic “conventional” DLTS as described originally by Lang [6], and computer DLTS, a variant of which was used for the investigation of deep levels in InP-based MQW photodiodes in chapter 3.
2.1.3 Conventional DLTS

As described previously, deep level transient spectroscopy (DLTS) is based on capacitance transient measurement, and was first introduced by Lang in 1974 [6].

Conventional DLTS is based on the “rate window” concept, which is conventionally implemented using a dual-gated integrator. One first selects an emission rate window such that the change in a capacitance will exhibit a peak when the deep level emission rate falls within the window. As one varies the sample temperature, the peak occurs at the temperature where the carrier emission rate is at the center of the rate window, as illustrated in Figure 2.3. This simplified explanation implicitly assumes that the carrier emission is thermally activated and thus depends exponentially on temperature. One temperature scan of this type contributes to one data point in the Arrhenius plot; the full plot is formed by combining data taken with numerous temperature scans and rate windows.
A series of rate windows are thus chosen for the capacitance transient measurement described above, and one can construct a plot of the form shown in Figure 2.4 (five temperature scans in this case). From this one can derive the emission rate at the corresponding peak signal temperature. The emission time constant can be written as [6]

$$\tau = \frac{(t_1 - t_2)}{ln(t_1/t_2)} \quad (2.7)$$

After a series of $\tau$ are measured, an Arrhenius plot following Equation (2.6) can be generated, and from this the activation energy, etc., can be extracted.
Figure 2.4 Typical DLTS signal using double integrators. Each curve represents one temperature scan, and the two peaks represent two distinct deep traps. [6]

2.1.4 Computer DLTS

Improvements in computerized data collection and processing have made signal processing approaches (generically referred to as computer DLTS) feasible. In this method, the complete capacitance transient signal is digitized and analyzed numerically in a computer, and thus only one temperature scan is required to collect the complete data set [13]. The entire C-t curve is composed of typically several hundreds to thousands of data points. Since all of the trap parameters (and potentially contributions from multiple trap levels) are included in the capacitance transient, one can extract those parameters from the entire unfiltered C-t curve. Extractions with closely spaced (in energy) traps or continuous distributions are not straightforward with the conventional DLTS method, since the boxcar integrator heavily filters the information from the capacitance waveform, and may in some cases lead to errors in interpretation. In computer DLTS, however, one
selects a mathematical model for the capacitance transient, generally based on expectations from the device physics or other considerations. The parameters of this model can then be extracted using the measured data directly. In this way, the presence of multiple traps, continuous trap distribution (vs. discrete levels), etc., can be handled in a straightforward and direct way. This is the approach that has been pursued in the work shown here.

For extracting the model parameters, least-squares fitting is used to extract the trap parameters. As an example of this approach, suppose there are several discrete traps in the semiconductor, so the capacitance transient can be expressed as the sum of multiple exponential functions [13]

\[ C(t) = C_0 + \sum_{i=1}^{N} \Delta C_i \exp\left(-t/\tau_i\right). \quad (2.8) \]

The values of \( C_0, \Delta C_i, \tau_i \) are then extracted by least-squares fitting to the measured \( C(t) \) at each temperature.

After the extraction of each time constant \( \tau_i \) in a range of measurement temperatures, Arrhenius plots can be constructed to resolve the trap energies and capture cross sections following Equation (2.6).

The block diagram for our computer DLTS is shown in Figure 2.5. The device under test (DUT) is mounted in the cryostat, so the device temperature can be precisely controlled by a Lakeshore temperature controller. The input signal is provided by a pulse generator, and we can change all parameters of the pulse, including period, pulse width, pulse height, and steady state bias. The device output is then connected to a high-speed
capacitance meter, and the capacitance data can be stored in a computer through a data acquisition (DAQ) board.

![Diagram of computer DLTS system]

**Figure 2.5** Block diagram for computer DLTS system.

2.2 Low frequency noise spectroscopy (LFNS) and Random Telegraph Signal (RTS) characterization

As alternatives to DLTS, low frequency noise spectroscopy (LFNS) and random telegraph signal (RTS) measurement can also provide information about defects in semiconductor materials and devices. In this section the phenomenology and experimental approaches associated with these two closely-related methods are described.

2.2.1 Basic description of noise in devices

Electrical noise is often a limit to the performance of a device, and thus is one of the most important figures of merit. For our purposes here, however, it can also provide a
window into the defects within the material or device. Noise in devices generally consists of both white noise and low frequency noise [14]. It is frequently observed that the power spectral density (PSD) is dependent on frequency in the low frequency region – typically below a few MHz – and then becomes frequency independent at higher frequencies. The white noise “floor” is typically limited by thermal and shot noise [9]. The “excess noise” above the noise floor in the low frequency region is called low frequency noise (LFN).

![Figure 2.6 Typical measured low frequency noise with (a) and without (b) generation-recombination noise.](image)

LFN includes 1/f noise (or flicker noise) – which has a PSD that is typically inversely proportional to frequency – and generation-recombination (GR) noise, which appears as a Lorentzian superimposed on the 1/f noise. Figures 2.6(a) and (b) show examples of measured low frequency noise without and with GR noise, respectively. While the origin of 1/f noise is a topic of ongoing philosophical debate with some researchers advocating carrier number fluctuation as the root cause, and others advocating carrier mobility fluctuation as the origin, generation-recombination (GR)
noise has its origins well defined in the processes associated with carriers making transitions to and from discrete energy states in the bandgap. These transitions, which are illustrated in Figure 2.7, can have the following four forms [14]: (1) free electron and free hole recombine; (2) free electron and free hole are generated; (3) free electron captured or emitted by electron trap; (4) free hole captured or emitted by hole trap. Since these processes are discrete, random events, they generate noise with frequency signatures related to the underlying physical processes. As a consequence of the close relationship between the noise generated and the properties of the deep level state that makes it possible, low frequency noise can be used to characterize deep level defects in semiconductors.

Figure 2.7 Energy band diagram for a semiconductor with deep-level impurities

As an alternative to frequency-domain representations, these random processes can also in many cases be observed in the time domain. One particularly useful class of time domain signals for defect analysis is RTS noise. In RTS noise, the device current is found to switch between two or more discrete states under a given operating condition, corresponding to random carrier capture and emission from deep levels. For a device
exhibiting 2-level RTS, the time duration of the high- and low-current state ($\tau_h$ and $\tau_l$, respectively) typically follow Poisson distributions. Poisson-governed processes of this type produce Lorentzian frequency-domain PSDs as described previously; the harmonic mean of these time constants ($1/\tau=1/\tau_h+1/\tau_l$) corresponds directly to the time constant that is extracted using the frequency-domain techniques described above. However, an important and useful property of RTS noise is that it can be used to identify the nature of each level, due to the fact that it allows separation of the capture and emission processes since statistics on $\tau_h$ and $\tau_l$ are available separately. Figure 2.8 illustrates the process of carrier capture and emission that correspond to each current state for a 2-level fluctuation. For bulk resistive samples, the high- and low-current states represent the neutral and charged states (positively charged for a donor-like deep level, and negatively charged for an acceptor-like deep level), respectively, since the Coulomb scattering – and thus the resistance along the current path – increases when the deep level is in charged state [10]. Because the capture time constant is inversely proportional to free carrier concentration as indicated by $\tau_c = \frac{1}{n\sigma_n v_{th}}$ [13], RTS noise can be used to distinguish the capture and emission processes by evaluating the bias dependence. This then allows unambiguous determination of the nature (i.e., acceptor-like or donor-like) of the observed deep levels. More specifically, if the low-current state duration changes with bias, the deep level is recognized as a donor-like state, while if the on-state is bias dependent, then the deep level is acceptor-like. The preceding analysis is based on the assumption of n-type bulk conductivity; similar arguments with the opposite signs apply for p-type samples.
Figure 2.8 Carrier emission and capture process for donor- and acceptor-like deep levels in n-type material, illustrating processes associated with high- and low-current states. The size of the horizontal arrows represents the current density.

Figure 2.9 shows the experimental configurations used for both LFNS and RTS noise measurements. The devices under test are biased using a battery-powered divider network, and the bias circuit is shielded to prevent electromagnetic interference (EMI) from external sources. Both voltage and current (transimpedance) low noise amplifier (LNA) are used for measurement convenience. A dynamic signal analyzer (SR 785) and digital storage oscilloscope are used for recording the noise spectra and time-domain RTS signals, respectively.
2.2.2 Mathematical description of low frequency and RTS noise

The current spectral density of low frequency noise can be expressed as [9]

\[ S_I = \sum \frac{A_i}{1 + (2\pi f \tau_{0i})^2} + \frac{B}{f} + C \quad (2.9) \]

The three terms represent GR noise, 1/f noise, and white noise, respectively. The GR term consists of a series of Lorentzian peaks in the current noise. In Equation (2.9), \( S_I \) is the current spectral density, and \( \tau_{0i} \) is the time constant of each GR center. Figure 2.10 shows a typical measured low frequency noise PSD for a GaAsSb homojunction pn diode. As can be seen, several distinct humps are superimposed on the overall 1/f background. By making a least-squares fit to equation (2.9), the time constants \( \tau_{0i} \) corresponding to each Lorentzian (2 Lorentzians in Figure 2.10) can be extracted. Similar measurements taken as a function of temperature allow each \( \tau_{0i} \)’s temperature dependence to be found. Once each \( \tau_{0i} \) is extracted as a function of temperature, one can...
make an Arrhenius plot to extract the trap energy level, in exactly the same way as for DLTS.

![Arrhenius plot](image)

Figure 2.10 Measured low frequency noise plot of a GaAsSb homojunction pn diode at 276.6 K. 2 Lorentzians are seen superimposed on the 1/f background noise.

The extraction of time constants from RTS signals is somewhat less direct than in LFN. However, by statistical analysis of the carrier transition probability in each energy state (high current state and low current state), it is found that the transitions follow a Poisson distribution [15],

$$p(t) = \frac{1}{\tau} \exp\left(-\frac{t}{\tau}\right)$$  \hspace{1cm} (2.10)

where $\tau$ is the time constant of high (or low) current state, and $p(t)$ is the probability density of the trap state being in the high (or low) current state at time $t$ and making transition to the low (or high) current state at time $t+dt$. Consequently, if we collect an
RTS pulse train (typically containing ~100 transitions), a semi-logarithmic histogram of counts versus discrete time intervals can be constructed (as illustrated in Figure 2.11), and from this the time constant $\tau$ can be extracted from the slope of the histogram.

Figure 2.11 An illustration of semi-logarithmic histogram plot of the time durations [14].

The expression for the PSD of RTS noise can also be derived, and can be shown to be a Lorentzian function [14],

$$S_l(f) = \frac{4(\Delta I)^2}{(\tau_l+\tau_h)((1/\tau_l+1/\tau_h)^2+(2\pi f)^2)}$$

(2.11)

where $\Delta I$ is the amplitude of the RTS, and $\tau_l$ and $\tau_h$ are the time constants associated with the low current and high current states, respectively. It can be seen that Equation (2.11) is essentially the same as the Lorentzian part in Equation (2.9), which is expected since both expressions originate from the same underlying physical processes.
2.3 MOS Interface trap density characterization

As discussed, DLTS, LFNS, and RTS techniques are very sensitive techniques for detecting and analyzing bulk material defects. For field-effect devices such as MOSFETs, defects at the oxide/semiconductor interface can play an important role. These defects are attributed to dangling bonds or the material imperfections at the insulator/semiconductor interface. As these interface states charge and discharge, they have a strong influence on the device operation since they are electrostatically coupled to the underlying semiconductor channel. Typical effects include elevated trap-assistant tunneling current, reduced effective breakdown field of the gate dielectric, dynamic shifts in the threshold voltage, hysteresis effects in the DC characteristics, and degraded noise performance [13]. It should also be noted that unlike bulk defects that typically exhibit discrete energy levels, the interface trap density (D\textsubscript{it}) versus energy within the gap typically exhibits a U-shaped distribution, with a minimum near midgap and sharp increases towards each band edge. Capacitance-voltage measurement and conductance spectroscopy are two of the most reliable and commonly adopted D\textsubscript{it} extraction techniques. Conventional DLTS is difficult to apply directly to MOS structures since the insulating oxide prevents filling and injection pulses from filling states as needed. More advanced techniques (e.g. CTS) have been developed, but C-V and conductance approaches dominate due to their easier interpretation. These methods will be briefly discussed in the following sections, and will be implemented in Chapter 4.

2.3.1 Capacitance-voltage method

There are many approaches to use C-V characteristics to determine D\textsubscript{it} [17]. Each has strengths and weaknesses, depending on the device being measured. For III-V
channel MOSFETs, the Terman method or the high frequency C-V method is commonly applied because it can be tailored to address conditions typical of III-V devices [13, 18, 19].

In the Terman method, capacitance is measured as a function of gate bias with a frequency fixed at a sufficiently high value that the interface traps can be assumed not to respond. Although the interface traps do not follow the applied ac gate voltage, they do follow the slowly changing dc gate bias, and cause the high frequency C-V curve to stretch out along the gate bias axis in order to maintain charge neutrality. The capacitance at high frequency, $C_{HF}$, is given by (2.12)

$$C_{HF} = \frac{C_s C_{ox}}{C_s + C_{ox}} \quad (2.12)$$

where $C_s$ is the capacitance of semiconductor space charge region, and $C_{ox}$ is the oxide capacitance. The corresponding equivalent circuit is shown in Figure 2.12, which neglects the effect of series resistance and $D_{it}$.

Figure 2.12 High frequency equivalent circuit of an idealized MOS capacitor.
Since interface states do not respond to the ac signal, the measured $C_{HF}$ can be used as a probe of the band bending in the device under bias; an ideal MOS capacitor and one with defects present will exhibit the same $C_{HF}$ only if the band bending is the same in both structures. Thus, by knowing the semiconductor band bending, $\psi_s$, for a given $C_{HF}$ in an ideal MOS capacitor and the measured gate bias dependence of $C_{HF}$ in the non-ideal device being tested, the relationship between $\psi_s$ and $V_G$ can be constructed, and from this relationship the $D_{it}$ can be found: \(^{[19]}\)

$$D_{it}(\psi_s) = C_{ox} \left[ \left( \frac{d\psi_s}{dV_G} \right)^{-1} - 1 \right] / q^2 - C_s(\psi_s)/q^2$$

(2.13)

However, there are some practical considerations and potential error sources associated with this approach. In the Terman method, it is explicitly assumed that the interface traps do not follow the ac gate voltage. While this is an excellent approximation for midgap traps in Si and large bandgap channel materials like GaAs, it does not necessarily apply for materials with smaller bandgaps (e.g., InAs). In addition for devices with continuously distributed interface states (as opposed to discrete levels), one should consider that as the Fermi level approaches the band edge, the time constants of the interface traps become much shorter, and may respond to the ac voltage. Thus, only $D_{it}$ that lie well away from the band edges (i.e., over a portion of the bandgap near midgap) can be extracted with small error. As a rough rule of thumb, one can show that for a typical measurement frequency of 1 MHz, traps more than 0.21 eV away from the band edge will not follow the ac voltage (which means the characteristic frequencies of those traps are lower than 1 MHz), assuming the capture cross section is on the order of $10^{-15}$ cm$^{-2}$.
2.3.2 Conductance method

An alternative to C-V approaches such as the Terman method is the conductance method [19]. The conductance method is one of the most sensitive methods used to measure $D_{it}$, and is based on the fact that the conductance represents the energy loss due to carrier capture and emission from interface traps. It is performed by measuring the equivalent parallel conductance, $G_p$, of a MOS capacitor as a function of bias voltage and frequency, and using this information to infer the interface state density.

The equivalent circuit of a MOS capacitor used in the conductance method is shown in Figure 2.13(a). It consists of an oxide capacitance $C_{ox}$, a series semiconductor space charge capacitance $C_s$, an interface trap capacitance $C_{it}$, which is due to the trapped charge at the interface, and an interface resistance $R_{it}$, which arises from the lossy process of carrier capture and emission. For analysis, the simplified equivalent circuit shown in Figure 2.13(b) is used, where $G_p$ can be expressed as [19]

$$\frac{G_p}{\omega} = \frac{qD_{it}}{2\omega\tau_{it}} \ln[1 + (\omega\tau_{it})^2]$$  \hspace{1cm} (2.14)

In this expression, $\tau_{it}$ is the effective time constant of the (possibly distributed) interface states, and $\omega$ is the angular frequency. The expression has its maximum at $\omega = 1.98/\tau_{it}$, and $D_{it} = 2.5G_p/Aq\omega$ at this maximum. Thus $D_{it}$ is determined from the peak of the $G_p/\omega$ versus frequency plot for an interface trap with time constant of $\tau_{it}$.

In practice, $G_p$ is usually obtained experimentally by using an LCR meter, typically in the form of a parallel $C_m$ and $G_m$, as shown in Figure 2.13 (c). Hence $G_p$ is
calculated from the measured $C_m$ and $G_m$ by removing the effects of $C_{ox}$ from the circuit in Figure 2.13(c). This results in the following expression for $G_p$: [19]

$$\frac{G_p}{\omega} = \frac{\omega G_m C_{ox}}{G_m^2 + \omega^2 (C_{ox} - C_m)^2}$$

(2.15)

where $C_m$ and $G_m$ are the measured capacitance and conductance, respectively.

Figure 2.13 Equivalent circuits for conductance measurements for determining $D_{it}$ in MOS capacitance. (a) MOS capacitor with interface trap time constant $\tau_{it} = R_{it} C_{it}$, (b) simplified circuit of (a), (c) circuit model typically assumed in LCR-based measurement configurations. [13]

In order to extract the trap energy level information needed for constructing a $D_{it}$ versus energy relationship, the measurement frequency $f$ can be related to a corresponding level in the bandgap by using Equation (2.5) in conjunction with $\tau = 1/2\pi f$. As can be seen in Equation (2.5), the characteristic frequency depends exponentially on the trap energy within the bandgap; the further the trap is away from the band edge, the slower it emits a trapped charge.
It should be noted, however, that in Equation (2.5), although all other parameters are well known, the capture cross section can vary with trap energy level for continuously distributed states. For the analysis in Chapter 4, a constant $\sigma$ is assumed for simplicity. This assumption of course will lead to some errors in the extracted energy levels, but due to the strong exponential dependence on trap energy, the inverse proportionality to $\sigma$ is comparatively mild. For the devices evaluated here, strong Fermi-level pinning is observed, preventing the use of flat-band extraction approaches [13, 19] that are popular for Si-based devices.
3.1 Introduction on InGaAs/GaAsSb quantum well photodiodes

Mid infrared (2 µm – 5 µm) detection has been an active research area for several decades, since it has many important applications such as missile tracking and night vision. Mercury cadmium telluride (HgCdTe) is the dominant material used for mid-IR sensors today, since it is extremely versatile from the perspective of bandgap tailoring, and has demonstrated excellent performance at low temperatures [20-22]. However, HgCdTe suffers from material non-uniformity, which increases the cost of HgCdTe photodetectors due to reduced yield [23]; and the requirement for low temperature operation increases overall system cost. On the other hand, InP-based multiple quantum well (MQW) photodetectors, particularly type II InGaAs/GaAsSb MQW structures, have been demonstrated as promising candidates for mid-IR detection [24-27]. The maturity of InP-based epitaxial growth and fabrication, combined with the ability to tailor device response through the use of unstrained or strained heterostructures makes InP-based photodetectors potentially attractive. However, the device performance can be limited by excess dark current due to the presence of defects and deep levels located in the bulk material, at heterointerfaces between materials, or along surfaces [26, 28-29]; these
defects can be formed either during growth or induced during fabrication. Thus a detailed understanding of these defects is important for optimizing device performance.

Because the available literature on defects in InGaAs/GaAsSb heterostructure is extremely limited, and MQW photodiodes have quite complicated epitaxial structures compare to simple PIN photodiodes, considerable care is required in the design of the experimental study so that reliable conclusions can be drawn and the data is applicable to device structures of practical interest. To facilitate this, the study was performed in two stages. First, simple test structures consisting of InGaAs and GaAsSb homojunctions, as well as single InGaAs/GaAsSb heterojunctions were characterized using the techniques described in Chapter 2 (specifically DLTS, LFNS and RTS), to identify mature bulk and interfacial defects. These simpler structures allow for simpler interpretation of the measurement results, and provide a baseline against which more complex device structures can be compared. As a second step, we designed full MQW photodiodes in co-operation with our collaborators at the University of Virginia for desired detection wavelength, and measured and interpreted the deep levels in those devices. In this analysis, the results from the simplified structures allowed the defect-related deep levels in these more complicated device structures be determined with improved certainty. Finally, a novel strained-layer MQW photodiode, which is designed to have the ability to detect longer wavelengths, is also investigated in terms of defect properties.

In this chapter, the results of low-frequency noise spectroscopy (LFNS) and random telegraph signal (RTS) characterization, as well as DLTS, on test samples of InGaAs and GaAsSb homojunctions and heterojunctions, InGaAs/GaAsSb MQW photodiodes, and a novel InGaAs/GaAsSb photodiode are described. We will show that
by comparing the results obtained with several carefully selected test structures in a step-by-step approach, a series of deep levels have been identified, and their location in the bulk and at material interfaces has been determined.

3.2 Deep level characterization of In$_{0.53}$Ga$_{0.47}$As and GaAs$_{0.5}$Sb$_{0.5}$ homojunction and heterojunction test samples using LFNS and RTS

In order to investigate deep levels in both bulk materials and at heterointerfaces, $p^+n$ diodes were fabricated on three epitaxial structures of In$_{0.53}$Ga$_{0.47}$As and GaAs$_{0.5}$Sb$_{0.5}$.

The wafers were grown by IntelliEpi, Inc. by molecular beam epitaxy (MBE; the structures are shown schematically in Figure 3.1. Samples (a) and (b) are In$_{0.53}$Ga$_{0.47}$As and GaAs$_{0.5}$Sb$_{0.5}$ homojunctions, respectively, and are used to measure bulk deep levels, while sample (c) is an In$_{0.53}$Ga$_{0.47}$As/GaAs$_{0.5}$Sb$_{0.5}$ heterojunction and thus may contain both bulk and interfacial deep levels. The doping concentration of the lightly doped $n^-$ region in all three structures is estimated to be $5 \times 10^{15}$ cm$^{-3}$ from conventional capacitance-voltage (CV) measurements.

![Figure 3.1 Heterostructure diagrams of the (a) In$_{0.53}$Ga$_{0.47}$As and (b) GaAs$_{0.5}$Sb$_{0.5}$ homojunctions, and (c) In$_{0.53}$Ga$_{0.47}$As/GaAs$_{0.5}$Sb$_{0.5}$ heterojunction.](image-url)
For the low-frequency noise characterization, InGaAs and GaAsSb homojunctions and InGaAs/GaAsSb heterojunction devices with areas of $2.54 \times 10^{-4}$ cm$^2$ and $1.33 \times 10^{-4}$ cm$^2$ were measured over the temperature range of 100 K to 400 K. The carrier lifetimes associated with G-R centers in these devices were extracted by fitting the measured noise spectra to the sum of $1/f$, thermal noise, and G-R Lorentzians, and discrete energy levels for the G-R centers were then obtained from Arrhenius plots. Figure 3.2(a) shows a typical fitting to the noise spectra, while Fig. 3.2(b) illustrates a typical temperature dependence observed. Since the applied bias is small, the device can be assumed to be linear, and thus the current spectral density, $S_I$, can be obtained from the more easily measured voltage spectral density, $S_V$, through $S_I = S_V / R^2$, where $R$ is the small-signal differential resistance of the device under test [30]. For each trap level identified, the applied bias was adjusted to provide a clear Lorenztian signature and the resulting current density was recorded, as shown in Table 3.1; the different current densities largely reflect differing trap densities and cross-sections. During the temperature scan, the current density was held constant for each deep level, to ensure that the probability of carrier interaction with the deep level did not vary with temperature. The applied voltages corresponding to the current densities reported here were typically $\sim 100$ mV.
Figure 3.2 (a) Typical measured noise spectrum and Lorentzian fit to the measured current noise spectral density ($S_I$) for a typical InGaAs/GaAsSb heterostructure diode at 375 K, showing superposition of 1/f noise and G-R noise. (b) The shift in measured spectra and associated Lorentzian signatures with temperature.

Figure 3.3 Arrhenius plot for all observed traps in both homojunction and heterojunction devices.
Figure 3.3 shows a summary of all of the deep levels observed in the three structures using LFNS. For the InGaAs homojunctions, a single deep level (E1) at 0.11 eV with capture cross section of $2.02 \times 10^{-18} \text{ cm}^2$ was extracted, while for typical GaAsSb homojunction devices four deep levels (at 0.11 eV (E2), 0.20–0.22 eV (E3), 0.29 eV (E4), and 0.40 eV (E5)) were found within each device, with corresponding capture cross sections of $7.47 \times 10^{-18} \text{ cm}^2$, $1.08 \times 10^{-17} \text{ cm}^2$, $1.78 \times 10^{-17} \text{ cm}^2$, and $1.70 \times 10^{-17} \text{ cm}^2$, respectively. The strikingly similar energy levels of E1 and E2 suggest they may have a common origin, such as a trap related with gallium or arsenic site. Electron traps at 0.22 eV and 0.38–0.41 eV have previously been reported for bulk GaAsSb [31], so E3 and E5 are likely to be these previously-reported traps. The huge difference between InGaAs and GaAsSb homojunctions in terms of defects is actually not surprising, since the MBE growth of InGaAs is considerably more mature than that for GaAsSb.

For the InGaAs/GaAsSb heterojunction, five deep levels were observed in typical devices by the same methodology. The traps are located at 0.13 eV (E6), 0.21 eV (E7), 0.37 eV (E8), 0.39 eV (E9), and 0.66 eV (E10), with corresponding capture cross sections of $1.14 \times 10^{-16} \text{ cm}^2$, $1.57 \times 10^{-16} \text{ cm}^2$, $2.07 \times 10^{-13} \text{ cm}^2$, $3.55 \times 10^{-16} \text{ cm}^2$, and $5.35 \times 10^{-14} \text{ cm}^2$, respectively. Comparing these deep levels with those found in homojunction devices, it is found that E7 and E9 likely correspond to the same GaAsSb bulk levels as E3 and E5, respectively, as observed in the homojunctions. We also note that traps E1 and E2 (corresponding to InGaAs and GaAsSb homojunctions, respectively) overlap in energy. These two levels are thus not individually resolvable in the heterojunction devices, but we observe trap E6 at essentially the same energy. This overlap may contribute to the observed increase in apparent trap cross-section for E6 relative to either E1 or E2. E8 and
E10, however, are likely to be interface-related, since they appear only in heterojunction devices. A hole trap at \( E_v + 0.67 \) eV was previously observed in both InGaAs/GaAs and GaAsSb/GaAs interfaces, and was ascribed to interface misfit dislocations [32]; thus E10 may be due to misfit dislocations that arise from interface imperfection. All the parameters of these discrete deep levels are summarized in Table 3.1.

To arrive at a more comprehensive understanding of the measured low frequency noise, a bias-dependent study of the noise spectrum \( S_\nu \), as a function of temperature was also performed. One striking observation is that, for comparable bias conditions, the measured noise level in heterostructure devices was typically several orders of magnitude larger than that for homojunction devices; a typical example is shown in Figure 3.4 (a). These measured noise spectra were analyzed by fitting the 1/f region to the form \( S_\nu = K_f V^m / f^\beta \) to obtain the voltage dependence coefficient \( m \) (Figure 3.4(b)) and the noise magnitude coefficient \( K_f \), where \( K_f \) is mathematically identical to \( \alpha / N \) in Hooge’s empirical equation [33] for the case of \( m \approx 2, \beta \approx 1 \) (as was observed in the devices evaluated). The observed trend in \( K_f \) vs. temperature for all three device types investigated is shown in Figure 3.5. It is clear that the trend in \( K_f \) is substantially different among InGaAs, GaAsSb, and heterojunction devices. This difference suggests that energetically-distributed interface states exist at the heterointerfaces of the heterojunction devices, since the superposition of a large number of Lorentzians over an energy range in the bandgap can appear in measurements as an increased broadband noise level, leading to an elevated 1/f noise level [14]. This is consistent with the view of 1/f noise arising from carrier number fluctuation due to carrier capture and emission from deep levels [14].
Figure 3.4 (a) measured noise spectral density, $S_v$, measured at 5 mV, 12 mV, and 20 mV for GaAsSb homojunction and InGaAs/GaAsSb heterojunction diodes at 250 K. (b) $S_v$ of typical GaAsSb homojunction devices measured as a function of bias voltage, extracted at 10 Hz.

Figure 3.5 Extracted $K_f$ of homojunctions and heterojunction devices vs. temperature, suggesting fundamental differences in defect density and distribution, possibly at heterointerfaces between materials.
To further elucidate the nature of these bulk traps, RTS noise was evaluated as a function of temperature and bias. As an example, for trap E5 in GaAsSb it was observed that the duration of the low-current state decreases with increasing bias, as shown in Figure 3.6. Thus the lower current state corresponds to the charged state of this deep level, and the response time is dominated by the carrier capture process, according to the discussion in section 2.2.1. Thus E5 can be identified as a positively-charged center during the carrier capture, which is a donor-like deep level.

![Figure 3.6 Typical measured RTS noise of a GaAsSb homojunction measured at 245 K, with bias current of 0.331 mA/cm$^2$ (upper) and 0.194 mA/cm$^2$ (lower). Bias dependence indicates trap E5 is donor-like.](image)

Except for levels E1 and E2, whose relatively shallow position in energy prevented them from being conclusively observed in RTS, the types of all of the other observed deep levels have been identified following the same strategy as described above, and the results are summarized in Table 3.1. This RTS study also confirms conclusions
drawn previously from the LFNS characterization. For example, E3 and E7 were suspected to be the same level from the LFNS study; from the RTS measurements they are also both identified as acceptor-like deep levels, bolstering this interpretation. Similarly, E5 and E9 are both donor-like deep levels, which is consistent with the previously-noted similarity between their energy levels.

TABLE 3.1

SUMMARY OF DEEP LEVEL CHARACTERISTICS IN TEST SAMPLES.

<table>
<thead>
<tr>
<th>Sample</th>
<th>Trap</th>
<th>$E_A$ (eV)</th>
<th>$\sigma_n$ (cm$^2$)</th>
<th>Trap type</th>
<th>Current density (mA/cm$^2$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>In$<em>{0.53}$Ga$</em>{0.47}$As</td>
<td>E1</td>
<td>0.11</td>
<td>2.02×10$^{-18}$</td>
<td>—</td>
<td>0.6</td>
</tr>
<tr>
<td>Ga$<em>{0.5}$As$</em>{0.5}$Sb</td>
<td>E2</td>
<td>0.11</td>
<td>7.47×10$^{-18}$</td>
<td>—</td>
<td>6.7</td>
</tr>
<tr>
<td></td>
<td>E3</td>
<td>0.20–0.22</td>
<td>1.08×10$^{-17}$</td>
<td>A-like *</td>
<td>6.7</td>
</tr>
<tr>
<td></td>
<td>E4</td>
<td>0.29</td>
<td>1.78×10$^{-17}$</td>
<td>A-like</td>
<td>6.7</td>
</tr>
<tr>
<td></td>
<td>E5</td>
<td>0.40</td>
<td>1.70×10$^{-17}$</td>
<td>D-like **</td>
<td>6.7</td>
</tr>
<tr>
<td>In$<em>{0.53}$Ga$</em>{0.47}$As/</td>
<td>E6</td>
<td>0.13</td>
<td>1.14×10$^{-16}$</td>
<td>D-like</td>
<td>0.75</td>
</tr>
<tr>
<td>GaAs$<em>{0.5}$Sb$</em>{0.5}$</td>
<td>E7</td>
<td>0.21</td>
<td>1.57×10$^{-16}$</td>
<td>A-like</td>
<td>0.75</td>
</tr>
<tr>
<td></td>
<td>E8</td>
<td>0.37</td>
<td>2.07×10$^{-13}$</td>
<td>A-like</td>
<td>0.75</td>
</tr>
<tr>
<td></td>
<td>E9</td>
<td>0.39</td>
<td>3.55×10$^{-16}$</td>
<td>D-like</td>
<td>0.45</td>
</tr>
<tr>
<td></td>
<td>E10</td>
<td>0.66</td>
<td>5.35×10$^{-14}$</td>
<td>A-like</td>
<td>0.75</td>
</tr>
</tbody>
</table>

* Acceptor-like
** Donor-like
3.3 Deep level characterization of unstrained and strain-compensated InGaAs/GaAsSb multiple quantum well photodiodes

In addition to the single-junction test structures described and analyzed in the preceding sections, complete MQW photodiodes have also been characterized in order to determine the defects present in real devices. A significant technological advantage of type-II InGaAs/GaAsSb quantum well photodiodes is that the band alignment of the two adjacent materials within the MQW structure can be easily tuned by changing the ternary material composition. This allows the effective band gap of the superlattice structure can be changed over a wide range, and corresponds to the ability to vary the detection wavelength range. However, changing the composition also alters the lattice constant, and as the lattice constant changes more strain (either tensile or compressive) can be introduced within the type II quantum wells. The presence of this strain can in general also induce additional defects or change the properties of the native deep levels. Consequently, for this study three InGaAs/GaAsSb MQW photodiodes with lattice-matched and strain-compensated active regions were fabricated to investigate the deep levels that are present in the superlattice structures, and to identify any effects induced by strain. The three photodiodes structures were grown by IQE, Inc. by MBE; the epitaxial structures are shown schematically in Figure 3.7. Device PD1 (Figure 3.7 (a)) consists of 100 pairs of lattice-matched In$_{0.53}$Ga$_{0.47}$As/GaAs$_{0.5}$Sb$_{0.5}$ in a superlattice, device PD2 (Figure 3.7 (b)) contains 100 pairs of strain-compensated In$_{0.45}$Ga$_{0.55}$As/GaAs$_{0.4}$Sb$_{0.6}$ in a superlattice, and device PD3 (Figure 3.7 (c)) contains 100 pairs of strain-compensated In$_{0.33}$Ga$_{0.67}$As/GaAs$_{0.25}$Sb$_{0.75}$ in a superlattice. The three devices have progressively increasing amounts of local strain. For PD1, since it is a lattice-matched structure, the
local strain is zero; for PD2, the InGaAs layer has 0.56% tensile strain, and the GaAsSb layer contains 0.78% compressive strain; for PD3, the InGaAs layer has 1.33% tensile strain, and the GaAsSb layer has 1.86% compressive strain. In all cases, the actual lattice constant was maintained that of InP (all layers are pseudomorphic without relaxation). Thus the net strain of the three superlattice structures are kept at zero so that the device active region can be grown thick for better optical absorption without lattice relaxation.

<table>
<thead>
<tr>
<th></th>
<th>500 nm p-InP</th>
<th>500 nm p-InP</th>
<th>500 nm p-InP</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>25 nm U.I.D. In$<em>{0.53}$Ga$</em>{0.47}$As</td>
<td>25 nm U.I.D. In$<em>{0.53}$Ga$</em>{0.47}$As</td>
<td>25 nm U.I.D. In$<em>{0.53}$Ga$</em>{0.47}$As</td>
</tr>
<tr>
<td></td>
<td>100 pairs 7nm In$<em>{0.53}$Ga$</em>{0.47}$As/GaAs$<em>{0.5}$Sb$</em>{0.5}$ QWs</td>
<td>100 pairs 7nm In$<em>{0.45}$Ga$</em>{0.55}$As/GaAs$<em>{0.4}$Sb$</em>{0.6}$ QWs</td>
<td>100 pairs 7nm In$<em>{0.35}$Ga$</em>{0.65}$As/GaAs$<em>{0.25}$Sb$</em>{0.75}$ QWs</td>
</tr>
<tr>
<td></td>
<td>50 nm U.I.D. In$<em>{0.53}$Ga$</em>{0.47}$As</td>
<td>50 nm U.I.D. InP</td>
<td>50 nm U.I.D. InP</td>
</tr>
<tr>
<td></td>
<td>500 nm n-InP</td>
<td>500 nm n-InP</td>
<td>500 nm n-InP</td>
</tr>
<tr>
<td></td>
<td>Substrate n-InP</td>
<td>Substrate n-InP</td>
<td>Substrate n-InP</td>
</tr>
</tbody>
</table>

Figure 3.7 Device structures of (a) PD1, lattice matched In$_{0.53}$Ga$_{0.47}$As/GaAs$_{0.5}$Sb$_{0.5}$ MQW photodiode, (b) PD2, strain-compensated In$_{0.45}$Ga$_{0.55}$As/GaAs$_{0.4}$Sb$_{0.6}$ MQW photodiode, and (c) PD3, strain-compensated In$_{0.35}$Ga$_{0.65}$As/GaAs$_{0.25}$Sb$_{0.75}$ MQW photodiode.

Energy band diagrams, along with electron and heavy-hole wavefunction amplitudes for each of the device structures, were calculated from self-consistent solutions to Poisson and Schrödinger equations [35] and are shown in Figure 3.8. The effective band gap of the superlattice, which is the energy gap between the ground states of the electrons and holes, are 0.48 eV, 0.41 eV and 0.37 eV for lattice matched and two
strain-compensated devices, respectively. To note that the band gaps calculated are based on the properties of relaxed ternary materials.
Figure 3.8 Band alignment and wave functions for (a) PD1, (b) PD2, and (c) PD3 type II quantum wells in this study. The effective band gap decreases as local strain increases. (pages 43-45)
InGaAs and GaAsSb samples have been studied to determine their band gap energies. The figure shows two plots:

(a) In$_{0.53}$Ga$_{0.47}$As and GaAs$_{0.5}$Sb$_{0.5}$, with $E_{g,\text{eff}} = 0.48$ eV.

(b) In$_{0.45}$Ga$_{0.55}$As and GaAs$_{0.4}$Sb$_{0.6}$, with $E_{g,\text{eff}} = 0.41$ eV.
$E_g,_{\text{eff}} = 0.37 \text{ eV}$

In$_{0.33}$Ga$_{0.67}$As

GaAs$_{0.25}$Sb$_{0.75}$
3.3.1 IV characteristics of unstrained and strain-compensated MQW photodiodes

In order to assess the performance of these structures, the dark current-voltage characteristics of PD1, PD2, and PD3 were measured as a function of temperature; the results are shown in Figure 3.9. It can be seen that the breakdown behavior and overall temperature dependence of PD2 is markedly different from PD1 and PD3. This effect is likely due to the fact that the PD2 sample did not incorporate SiO$_2$ sidewall passivation, and thus leads to mesa surface leakage current that does not depend strongly on temperature. In the reverse bias region of PD1 and PD3, the temperature dependence indicates that the dark current is dominated by generation-recombination current at low voltage (< -15 V), while the tunneling current starts to be significant at higher voltage (> -15 V) [34]. For G-R dominated dark current, $I_{G-R} \propto \exp(-\Delta E_T/kT)$, where $\Delta E_T$ is the trap energy level in the band gap. Figure 3.10 shows the measured dark current density at -0.3 V plotted against inverse temperature. It can be seen that the activation energies extracted from an Arrhenius fit of the data over the temperature range from 215 K to 315 K are 0.29 eV for both PD1 and PD3 photodiodes; this energy is far from the effective band edge of the MQW structure as simulated previously. This suggests that carrier generation through near-mid-gap traps in the photodiodes contributes to the dark current. However, it should be noted that activation energy extracted in this way is an effective activation energy, which can be the average energy of several traps, especially when a limited temperature range is used for the extraction. Consequently, more detailed deep level characterizations are necessary to more clearly resolve the distribution in energy of the defect levels.
Figure 3.9 Current-voltage characteristics for typical unstrained (PD1) and strain-compensated (PD2, PD3) photodetectors, measured at several temperatures.
3.3.2 LFNS and RTS characterization of unstrained and strain-compensated MQW photodiodes

To more fully characterize the deep levels whose existence can be inferred from the dark I-V characteristics, LFNS was applied to both unstrained and strain-compensated MQW photodiodes. Devices with areas between $5 \times 10^{-4}$ cm$^2$ and $2 \times 10^{-3}$ cm$^2$ were measured over a temperature range from 100 K to 300 K, with a typical (forward) bias voltage of ~100 mV. From the measured noise spectra, carrier lifetimes of each deep level were extracted from the corresponding G-R noise peaks. Figure 3.11(a) is an example of a fit to the measured MQW photodiode noise spectra for PD3, including 1/f noise, Lorentzian, and white noise; Figure 3.11(b) shows the Lorentzian peak’s evolution with temperature.
Figure 3.11 (a) Measurement and Lorentzian fit to the measured current noise spectral density ($S_I$) of a strain-compensated device (PD3) at 201 K, showing superposition of $1/f$ noise, G-R noise and white noise, (b) The measured Lorentzian peak shifts in frequency with temperature, indicating the carrier lifetime decreases with increasing temperature.
To accentuate the Lorentzian component in the measured noise spectra, $f \times \text{PSD}$ was plotted vs. temperature and frequency to suppress the $1/f$ noise background [9]. Then from Equation (3.1), we obtain:

$$2\pi f S_v = \sum A_i (2\pi f \tau_{0i})/(1 + (2\pi f \tau_{0i})^2) + 2\pi B + 2\pi f C$$

(3.1)

Examples of these frequency-weighted spectra are shown in Figure 3.12, Figure 3.13 and Figure 3.14 for PD1, PD2 and PD3, respectively. Following this strategy, three traps have been extracted from the noise peak for each device. For PD1, the three traps have activation energies of 0.14 eV ($E_{a1}$), 0.34 eV ($E_{b1}$) and 0.43 eV ($E_{c1}$), with capture cross sections of $4.33 \times 10^{-17}$ cm$^2$, $2.12 \times 10^{-14}$ cm$^2$ and $1.13 \times 10^{-14}$ cm$^2$, respectively. For PD2, the activation energies were found to be 0.15 eV ($E_{a2}$), 0.21 eV ($E_{b2}$) and 0.45 eV ($E_{c2}$), with capture cross sections of $6.51 \times 10^{-17}$ cm$^2$, $2.04 \times 10^{-16}$ cm$^2$ and $5.5 \times 10^{-15}$ cm$^2$, respectively. For PD3, the activation energies were found to be 0.12 eV ($E_{a3}$), 0.33 eV ($E_{b3}$) and 0.43 eV ($E_{c3}$), with capture cross sections of $2.14 \times 10^{-18}$ cm$^2$, $2.83 \times 10^{-15}$ cm$^2$ and $3.75 \times 10^{-15}$ cm$^2$, respectively. These traps are summarized on the Arrhenius plot shown in Figure 3.15. For these energy and cross-section estimations, the cross-sections have been assumed to be constant over the temperature range evaluated for each trap. Since the temperature dependence of capture cross section is typically governed by

$$\frac{\sigma}{\sigma_0} = \exp\left(\frac{E_{\text{barrier}}}{kT}\right)$$

[12], where $E_{\text{barrier}}$ is the energy barrier for capturing carriers, and each trap is measured over a temperature range of approximately 50 K, the capture cross section is expected to exhibit only mild variation over the measurement conditions used for the energy and cross-section estimates. It can be seen that the three devices all have traps at ~0.12 eV – 0.15 eV ($E_{a1}$, $E_{a2}$ and $E_{a3}$) and ~0.43 eV – 0.45 eV ($E_{c1}$, $E_{c2}$ and
$E_{c3}$), and PD1 and PD3 exhibit a similar trap at ~0.33 eV – 0.34 eV ($E_{b1}$ and $E_{b3}$). This suggests that the activation energies associated with deep levels were largely unchanged by the local strain, but the cross-sections of the defects were noticeably affected; the corresponding defects have cross-sections that differ by approximately one order of magnitude between unstrained and strain-compensated devices. For the trap at 0.21 eV ($E_{b2}$) in PD2, a large discrepancy can be observed with $E_{b1}$ and $E_{b3}$ in both energy level and capture cross sections. This suggests that $E_{b2}$ is a new defect not present in PD1 and PD3, instead of the same $E_{b1}$ and $E_{b3}$.

Figure 3.12 Measurement and Lorentzian fit to the measured $f^*PSD$ of PD1 for (a) $E_{a1}$, (b) $E_{b1}$ and (c) $E_{c1}$. 
Figure 3.13 Measurement and Lorentzian fit to the measured f*PSD of PD2 for (a) $E_{a2}$, (b) $E_{b2}$ and (c) $E_{c2}$. Notice that $E_{a2}$ and $E_{b2}$ are observed in the same noise spectra.

Figure 3.14 Measurement and Lorentzian fit to the measured f*PSD of PD3 for (a) $E_{a3}$, (b) $E_{b3}$ and (c) $E_{c3}$. 
It should be noted that the activation energies extracted from LFNS are similar to, but distinct from, the estimate obtained from the temperature-dependent dark I-V characteristics (for PD1 and PD3). This confirms that the 0.29 eV activation energy extracted from the temperature dependence of the dark current reflects an average over multiple discrete trapping levels. The densities of the observed traps are not readily extracted from noise measurements of MQW photodiodes due to the complexity of the structure and the sensitivity of the Lorentzian amplitudes to the applied bias conditions. However, since the dark current performance is strongly related with deep levels, it can be expected that the trap densities in these device are significant.

RTS measurements were also performed, to obtain the type (i.e., acceptor-like or donor-like) of these identified deep levels. Several RTS noise signatures have been
observed in the photodiodes, with the exception of PD2 for which no clear RTS could be discovered. Figure 3.16 shows typical bias-dependent RTS corresponding to traps $E_{a1}$ and $E_{b1}$. To isolate each trap, the temperature was selected to maximize that trap response; $T=133$ K for $E_{a1}$ and $T=194$ K for $E_{b1}$, respectively. It can be seen from Figure 3.16 (a) and Figure 3.16 (b) that the probability of being in the low current state changes in an inverse relationship to the applied bias (i.e., at lower bias current the off state is more likely than at high bias current). This indicates that carrier capture is the dominating process in the low current state [15-16]. Thus $E_{a1}$ is positively charged during carrier capture, a donor-like signature. On the other hand, Figure 3.16 (c) and Figure 3.16 (d) show typical measured RTS signature at 194 K to isolate trap $E_{b1}$. In this case, lower applied bias is associated with a lower probability of being in the low current state and therefore $E_{b1}$ is charge neutral during carrier capture, indicating an acceptor-like trap. Similar RTS responses have been observed for $E_{a3}$ and $E_{b3}$ traps in PD3, indicating donor-like and acceptor-like natures, respectively. Unfortunately no clear RTS signature was obtained in the temperature range corresponding to $E_{c1}$ and $E_{c3}$, so the trap type of $E_{c1}$ and $E_{c3}$ is not resolved.
3.3.3 Discussion of deep levels in unstrained and strain-compensated MQW photodiodes obtained from LFNS and RTS

By comparing the deep levels observed in the full MQW photodiode, structures evaluated here to those found in homojunction and single-heterojunction test samples by their energy levels and capture cross sections, it is clear that the traps observed in the photodiodes overlap closely with some of those identified in the single-junction test structures. However, due to the band alignments in the type-II superlattice in the MQW detector structures, only donor-like defects within the InGaAs electron well and acceptor-like defects within the GaAsSb hole well are expected to contribute to photodetector dark current and noise, since other possible defect types (e.g. donors in GaAsSb, acceptors in InGaAs) would have occupancy statistics that are unfavorable for carrier capture and emission in the MQW structure. In addition, quantum confinement in the MQW shifts the
apparent energies of the traps; from a numerical Schrodinger equation solution (as shown in Figure 3.8) the ground state for electrons is \(\sim 0.09\) eV above the conduction band edge in InGaAs, and the heavy hole ground state lies \(\sim -0.02\) eV below the valence band edge in GaAsSb. Thus the apparent trap energies are expected to increase somewhat compared to traps found in the bulk test samples.

In particular, one can see that traps \(E_{a1}, E_{a2}\) and \(E_{a3}\) observed in all three photodiodes are very similar in energy and type to the InGaAs bulk trap \(E1\) (0.11 eV) in the single-junction test structure, suggesting that this defect resides in the bulk material. If this trap were in the MQW region, it must be associated with InGaAs layer because of the superlattice, but one would also expect the energy to be increased by \(\sim 0.09\) eV due to confinement. The fact that the energy is closer to the energy extracted from bulk InGaAs suggests that it may instead lie in the bulk InGaAs layers outside the quantum well.

Additional characterization by DLTS has been performed to confirm the spatial location of the trap, as will be discussed in the next section. It should be noted that traps with similar energy levels \(\sim 0.13-0.16\) eV have been reported previously in bulk InGaAs, however the physical origin remains unknown [36, 37]. Also, the close overlap in energy, as well as the same acceptor-like signature, between \(E_{b1}\) and \(E_{b3}\) in PD1 and PD3 reported here and \(E8\) (0.37 eV) in an InGaAs/GaAsSb heterojunction indicates they may be the same InGaAs/GaAsSb interface-related trap. But if we consider the energy shift of \(\sim 0.02\) eV due to the heavy hole ground states, it is more likely that \(E_{b1}\) and \(E_{b3}\) are the same trap as \(E4\) (0.29 eV), which is a GaAsSb bulk trap. The defect \(E_{c1}, E_{c2}\) and \(E_{c3}\) may be associated with the interface-related trap \(E8\) (0.39 eV effective energy after projection into a confined structure), but this is not fully determined since the type of the three
defects (i.e., donor- or acceptor-like) was not able to be resolved. We note that it is unlikely that these deep levels are related to GaAsSb bulk trap E5 despite the similar activation energy, as this donor-like state’s energy lies well above the InGaAs conduction band edge in the MQW structure. The discrepancy in cross-sections between the MQW interface traps and those extracted from the simpler test structures may arise from the high degree of localization of carriers in the MQW structure. As for E$_b$ in PD2, since no RTS noise was observed, the location cannot be determined unambiguously. However, there are still two possibilities that can be inferred from the energy level. If it is a donor-like level, then it can be an InGaAs related trap within the superlattice region and is the same one as E1 or E6 (~0.11 eV) after electron ground state compensation by 0.09 eV. The other possibility is that it is the same acceptor-like level as E3 (~0.20 eV) in GaAsSb bulk after heavy hole ground state compensation by 0.02 eV. While E$_b$’s capture cross section is closer in magnitude to that of E6, strain and quantum well confinement adds additional uncertainty to the determination from cross section.

3.3.4 DLTS characterization of unstrained and strain-compensated InGaAs/GaAsSb quantum well photodiodes

In addition to LFNS, DLTS was performed on the three MQW photodiodes to obtain more detailed information about the traps, such as trap type, trap density and spatial distribution. Here, computer DLTS was used instead of the conventional “rate window” method, as described in Chapter 2. Figure 3.17 shows a typical measured capacitance transient for PD3, along with a single-exponential fit to each curve. It is clear that the emission time constant decreases as the temperature increases, which is a typical thermal emission signature. The trap is also identified as an electron trap (majority-carrier
trap) from the transient shape. The trap energy level and the capture cross section were then extracted from an Arrhenius plot after emission time constant extraction at several temperatures.

![Capacitance transient for typical strain-compensated MQW photodiode (PD3) at several temperatures.](image)

Figure 3.17 Measured and fitted capacitance transient for a typical strain-compensated MQW photodiode (PD3) at several temperatures.

For this analysis, the device temperature was scanned from 100 K to 300 K and all three photodiodes were measured by DLTS over a range of bias conditions. With the reverse bias fixed at -0.1 V and an injection pulse of +0.2 V, an electron trap, $E_{a1,DLTS}$, at $E_C-0.13$ eV with capture cross section of $2.07\times10^{-18}$ cm$^2$ was found in PD1 between 125 K and 150 K. With the reverse bias fixed at -0.2 V and an injection pulse of +0.2 V, an electron trap, $E_{a2,DLTS}$, at $E_C-0.13$ eV with capture cross section of $9.50\times10^{-19}$ cm$^2$ was found in PD2 between 120 K and 160 K. With a reverse bias at -0.2 V and pulse bias at +0.1 V, an electron trap, $E_{a3,DLTS}$, was revealed in PD3 between 100 K and 125 K, with
an energy level of 0.11 eV below conduction band edge and capture cross section of \(2.21 \times 10^{-18} \text{ cm}^2\). The three traps extracted here are plotted as black dots in Figure 3.18. All the trap parameters extracted, including using both LFNS and DLTS are listed in the Table 3.2. It can be seen that the three ~0.11- 0.13 eV traps found by DLTS overlap extremely well with the ~0.12 - 0.15 eV traps revealed using LFNS in both energy level and capture cross section. For temperatures above 160 K, the reverse bias was swept from -1 V to 0 V with pulse biases ranging from -0.8 V to +0.5 V. Under these bias conditions, traps located within the quantum well region should be observed at some temperatures, since the MQW region is almost totally depleted under zero bias. However, no significant capacitance transient was observed in these cases. One possible explanation for this is that if the deep levels at 0.21 eV, ~0.34 eV and ~0.43 eV have very low trap density, the resulting capacitance modulation is below the sensitivity limit of the DLTS system. However, this is contradicted by the fact that the activation energy extracted from the dark current clearly showed an effective activation energy near midgap, with a strong influence on device performance. Such an effect should not be so easily observed if the trap density were low. Thus a more likely scenario is that these levels act as generation-recombination centers that are not easily detected by DLTS with positive bias pulses. Efficient G-R deep levels are not easily detected in DLTS because, unlike traps that interact solely with carriers in one band (either electrons or holes), for G-R centers both bands participate. As a consequence, both captured electrons and holes will emit back to the corresponding band edge during the steady state bias, and thus when the emission rates of electron and hole are comparable the net contribution of the trapped carriers to
the capacitance transient is zero. In this case, these deep levels have to be measured by alternative methods such as LFNS and RTS instead of DLTS.

In order to investigate the spatial distribution of the ~0.11-0.13 eV traps in three photodiodes, a quick method, first reported by Miller and Lang [12], was implemented instead of the more complicated double-correlated DLTS (DDLTS), which requires two correlated pulse generators to characterize the difference between two consecutive capacitance transients.

Normally, the pre-exponential factor in Equation (2.4) is used to roughly calculate the trap density. However, it has been noted that the results obtained using this method are typically 50% lower than the true value due to the “λ effect”, which arises from a
difference between the free-carrier depletion width and the deep level depletion width [12]. A more accurate approach is to fix the reverse bias and vary the pulse bias. The equation that describes this approach is given by [12]:

\[
\delta \left( \frac{\Delta C}{C} \right) = \left( \frac{\epsilon}{qW^2N_D} \right)^{N_T(x)} \frac{N_D(x)}{N_T(x)} \delta V
\]

(3.2)

where \(\delta (\Delta C/C)\) is the incremental change in relative capacitance at two filling pulse voltages, \(V\) and \(V + \Delta V\), \(W\) is the depletion width at the (fixed) reverse bias, \(N_D\) is the shallow donor concentration (assuming it is a one-sided p\(^+\)-n junction as used here). It can be seen from Equation (3.2) that the slope of a plot of \(\Delta C/C\) versus \(V\) is proportional to the relative trap density. This is convenient for quickly assessing the trap profiles. It should be noted that profiles may also be measured by fixing the pulse bias and varying the reverse bias; this alternative is conceptually similar but in practice can be used to measure traps deeper within the depletion region.

In this work, both of these approaches were used. Typical reverse bias was varied between 0 V and -0.5 V, and the pulse bias was varied from 0 V to +0.3 V. By combining the two directions of changing bias conditions, the spatial distribution of traps within the semiconductor junction can be estimated, as shown in Figure 3.19, Figure 3.20 and Figure 3.21 for PD1, PD2 and PD3, respectively. As the first step of deep level extraction, the free carrier concentration versus depletion width and reverse bias was determined from conventional C-V measurement at temperatures corresponding to those at which deep levels could be observed in DLTS (100 K – 150 K). Then by extracting the trap density at the edge of the depletion region corresponding to each bias condition and combining the information of bias versus depletion width obtained from the first step, it
can be seen that the traps are mostly located within 1.2 µm—1.3 µm away from the depletion edge, with peak trap densities of $3 \times 10^{13}$ cm$^{-3}$, $1 \times 10^{13}$ cm$^{-3}$ and $4 \times 10^{12}$ cm$^{-3}$, respectively. Taking into account that the quantum well region thickness is 1.2 µm in total, it is likely that the peak in trap concentration at around 1.2 µm for each device is located in or adjacent to the transition layers outside the quantum well region. By carefully comparing the three photodiode structures in Figure 3.7, it can be seen that all of these structures have identical anode structures consisting of n-InP/undoped InP/undoped InGaAs, while they have different transition layers in the cathode, with undoped InGaAs in PD1 and undoped InP in PD2 and PD3. Due to the similarity of the ~0.1 eV traps observed in different devices, they are most likely to be exactly the same trap in the same transition layer. Thus, it can be inferred that the apparent trap density peaks below the n-InP/undoped InP, in the 25 nm undoped InGaAs transition layer at the anode, instead of in the transition layers on the cathode side of the superlattices. From the C-V analysis, this trap location would indicate that the superlattice region has an effective background doping that is slightly p-type, which is consistent with common impurities such as Si in GaAsSb. A trap (E1) at 0.11 eV with capture cross section $2.02 \times 10^{18}$ cm$^2$ in bulk InGaAs was found previously from the analysis of InGaAs homojunctions; this photodiode trap is likely the same one. This shows that this level is not a unique feature of the superlattice structure, but rather originates from bulk material properties.
Figure 3.19 Trap profile for $E_{a_{DLTS}}$ (0.13 eV) in PD1. (a) CV characteristics, (b) carrier density profile with the corresponding the bias condition, (c) trap density as a function of bias.
Figure 3.20 Trap profile for $E_{a_{DLTS}}$ (0.13 eV) in PD2. (a) CV characteristics, (b) carrier density profile with the corresponding bias condition, (c) trap density as a function of bias.
By combining LFNS and DLTS, comprehensive characterization of traps in both unstrained and strain-compensated MQW photodiodes was performed. This study resulted in estimates of trap energy, capture cross section, and possible physical locations, which are summarized in Table 3.2 below. This work provides a baseline for comparing future device iteration against to assess improvements in material quality, as well as a
clear explanation for the limited noise performance of photodiodes based on this heterostructure family to date.

### TABLE 3.2

**SUMMARY OF MQW TRAP PARAMETERS**

<table>
<thead>
<tr>
<th></th>
<th>PD1</th>
<th></th>
<th>PD2</th>
<th></th>
<th>PD3</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>E (eV)</td>
<td>σ (cm²)</td>
<td>J (mA/cm²)</td>
<td>E (eV)</td>
<td>σ (cm²)</td>
<td>J (mA/cm²)</td>
</tr>
<tr>
<td>LFNS</td>
<td>0.14</td>
<td>4.33×10⁻¹⁷</td>
<td>1.0</td>
<td>0.15</td>
<td>6.51×10⁻¹⁷</td>
<td>0.02</td>
</tr>
<tr>
<td></td>
<td>0.34</td>
<td>2.12×10⁻¹⁴</td>
<td>1.0</td>
<td>0.21</td>
<td>2.04×10⁻¹⁶</td>
<td>0.02</td>
</tr>
<tr>
<td></td>
<td>0.43</td>
<td>1.13×10⁻¹⁴</td>
<td>2.3</td>
<td>0.45</td>
<td>5.50×10⁻¹⁵</td>
<td>0.02</td>
</tr>
<tr>
<td>DLTS</td>
<td>Eₐ⁻</td>
<td>2.07×10⁻¹⁸</td>
<td>---</td>
<td>Eₐ⁻</td>
<td>9.50×10⁻¹⁹</td>
<td>---</td>
</tr>
</tbody>
</table>

3.4 Deep level characterization of strained-well InGaAs/GaAsSb quantum well photodiode

The photodiodes characterized in the previous sections are based on a conventional way of strain compensating the active region, wherein two adjacent layers contain opposite strains to achieve zero net strain over the whole quantum well stack. However, it has been shown that if a non-zero net strain is introduced in the quantum well, the band alignment of InGaAs and GaAsSb can be tuned further to achieve even smaller effective band gap [38]. In other words, the detection wavelength of the
photodiode can be extended further to the longer wavelength direction, as illustrated conceptually in Figure 3.22 (b). From this point of view, the conventional strain-compensated structure loses a degree of freedom by tying the strain of one layer to the adjacent layer. In order to have zero net strain globally over the active region so that sufficiently thick absorption layers can be grown without crystal relaxation – while still incorporating strain in the quantum well – a strain-compensation barrier layer with opposite strain to the quantum well can be inserted between two QWs. This concept is illustrated schematically in Figure 3.22 (a) [38], and the experimentally-realized device structure (PD4) is shown in Figure 3.23 (grown by IQE, Inc. by MBE). In the actual structure, the active region contains 20 periods of tensile-strained In$_{0.2}$Ga$_{0.8}$As sandwiching a compressively-strained InGaAs/GaAsSb quantum well structure. As a first attempt to demonstrate this design approach, a relatively simpler structure has been utilized. Hence, instead of a more complicated MQW, a single quantum well of In$_{0.75}$Ga$_{0.25}$As/Ga$_{0.35}$As$_{0.65}$/In$_{0.75}$Ga$_{0.25}$As with local strain is used in each period. Each single quantum well contains a total compressive strain of 1.04%, and the tensile-strained barrier layer has 2.29% strain.
Figure 3.22 (a) Schematic illustration of the concept for photodiodes incorporating strained MQW and compensation barrier layer that achieves zero net strain. (b) The impact of different strain on absorption wavelength. [38]

Figure 3.23 MBE grown quantum well photodiode heterostructure (PD4) based on the conceptual structure of Figure 3.22. 20 periods of barrier/QW/barrier structure are incorporated in the device as active region.
The energy band diagram and wavefunction amplitudes for electrons and heavy holes for this structure are shown in Figure 3.24, as calculated from self-consistent solutions to Poisson and Schrödinger equations [35]. The effective band gap of the superlattice is 0.32 eV. Additional 6 higher energy heavy hole states (originating from the wider well region in the valence band) within the In$_{0.75}$Ga$_{0.25}$As/In$_{0.2}$Ga$_{0.8}$As quantum well are not illustrated in the figure for clarity.

![Figure 3.24 Energy band diagram and wavefunctions for the strained type II quantum wells.](image)

3.4.1 IV characteristics of the strained-well InGaAs/GaAsSb quantum well photodiode

The dark current-voltage characteristics of the InGaAs/GaAsSb photodiodes with strained quantum well (PD4) were measured as a function of temperature, as shown in Figure 3.24. Comparing to conventional MQW photodiodes studied in previous sections,
this device shows similar breakdown features. With about one third of the quantum well region thickness (0.436 µm versus 1.2 µm for the conventional structures), the breakdown voltage is also decreased by the same ratio, indicating the same breakdown field for the two different structures. The ideality factor n extracted from the small forward bias region is 2.01, which suggests the generation – recombination dominated transport.

Figure 3.25 I-V characteristics of PD4.

3.4.2 LFNS characterization of the strained-well InGaAs/GaAsSb quantum well photodiode

LFNS was applied to the strained-well InGaAs/GaAsSb quantum well photodiode (PD4) to characterize the deep levels. Devices with areas of $4.91 \times 10^{-4}$ cm$^2$ were measured over a temperature range from 100 K to 300 K, with typical (forward) bias voltage of $\sim 100$ mV. Similar to the techniques described in the previous section, by fitting to the
frequency-weighted noise spectra (f×PSD), carrier lifetimes of each deep level were extracted from the corresponding G-R noise peaks, as illustrated in Figure 3.26. Then according to the Arrhenius relationship, two traps have been identified with activation energies of 0.15 eV (E_{1,PD4}) and 0.26 eV (E_{2,PD4}), and capture cross sections of 9.15×10^{-19} cm^2 and 6.41×10^{-17} cm^2, respectively. Notice that in Figure 3.26 although the two sets of Lorentzians are observed over a similar temperature range, different bias current densities (2.65 A/cm^2 versus 8.15 A/cm^2, respectively) were applied to reveal the two traps. These traps are summarized on the Arrhenius plot shown in Figure 3.27.

![Figure 3.26 Noise spectra for traps in novel structure. The left column shows the Lorentzian peak corresponding to the trap at 0.15 eV, and the right column shows the one at 0.26 eV.](image_url)
Figure 3.27 Traps found in the strain-well photodiodes PD4 using LFNS.

Since RTS noise signatures could not be observed in this device, the origins of the two deep levels can only be determined by comparing to previously-observed deep levels, leading to some uncertainty. For $E_{1,PD4}$, it seems to have very close activation energy and capture cross section with $E_{a1}$, $E_{a2}$ and $E_{a3}$ in the conventional MQW photodiodes. If this were the case, it would be expected to be located in the transition layer outside the quantum well region. However, as will be shown in the next section, DLTS studies show that $E_{1,PD4}$ is actually a new trap located within the quantum well. For $E_{2,PD4}$, two possible origins exist, similar to $E_{b2}$ in PD2 studied previously. It could be the same donor-like level in bulk InGaAs as $E6$ (0.13 eV, $1.14\times10^{-16}$ cm$^2$), after electron ground state compensation of 0.12 eV (recall that the electron ground state increased from 0.09 eV above the conduction of band of InGaAs in the conventional MQW photodiodes; in this structure the offset increases to 0.12 eV, due to the decrease in the InGaAs layer.
thickness from 7 nm to 5 nm). Another possibility for $E_{2, PD4}$ is the E3 (acceptor-like level) in GaAsSb (0.20 eV – 0.22 eV, $1.08 \times 10^{-17} \text{ cm}^2$) after hole ground state compensation of 0.02 eV. Both of these possible origins indicate that $E_{2, PD4}$ is expected to reside within the quantum well region.

3.4.3 DLTS characterization of the strained-well InGaAs/GaAsSb quantum well photodiode

To augment the LFNS-based trap study discussed above, DLTS was also performed on the strained-well InGaAs/GaAsSb quantum well photodiodes (PD4) to obtain information such as trap type, trap density and spatial distribution.

During the experiment, the device temperature was scanned from 100 K to 300 K. A fixed reverse bias of -1 V was used, and the injection pulse was set to +0.2 V. A trap $E_{1, PD4, DLTS}$ at $E_v + 0.12$ eV with capture cross section of $8.10 \times 10^{-19} \text{ cm}^2$ was found between 120 K and 150 K. A typical measured capacitance transient evolution with temperature is shown in Figure 3.28, along with single-exponential fit to each curve. From the transient shape, it can be determined to be a hole trap. The trap energy level and the capture cross section were then extracted from an Arrhenius plot after emission time constant extraction at each temperature. The trap extracted here is plotted as black dots in Figure 3.29. All the trap parameters extracted, including using both LFNS and DLTS are listed in the Table 3.3.
Figure 3.28 Capacitance transient evolution with temperature for the 0.12 eV hole trap \( E_{1,PD4,DLTS} \) in PD4.

Figure 3.29 Hole trap found in PD4 by DLTS comparing to LFNS results.
The spatial distribution of the hole trap $E_{1,PD4,DLTS}$ was also investigated by the method used in section 3.3.4. Both fixed reverse, varying pulse bias and fixed pulse, varying reverse bias scans were used to cover a wide space charge region. During the measurement, the pulse bias was fine tuned from 0 V to 0.3 V while reverse bias was fixed at -1 V, or the reverse bias was varied from -2 V to 0 V while pulse bias was fixed at 0.1 V. The free carrier concentration versus depletion width and reverse bias was first estimated from standard C-V measurement. Then by extracting the trap density at the edge of the depletion region corresponding to each bias condition, a plot of trap density versus distance was constructed, as shown in Figure 3.30. It can be seen that $E_{1,PD4,DLTS}$ is fairly uniformly distributed within ~0.45 µm from the edge of depletion region, with trap densities of $\sim 7 \times 10^{12}$ cm$^{-3}$, and the trap density abruptly decreases beyond 0.45 µm. Since the quantum well region thickness is 0.44 µm in total, it is clear that the trap is located within the quantum well region. Also taking into account the hole trap property, $E_{1,PD4,DLTS}$ actually lies 0.10 eV above GaAsSb valence band edge (after 0.02 eV hole ground state compensation), and within the GaAsSb layer. Due to the trap type and spatial distribution discussed above, this is a new trap that was not previously observed in either the single-junction test structures or the conventional PD1 – PD3. The close activation energy and capture cross section of $E_{1,PD4,DLTS}$ and $E_{1,PD4}$ indicate they are the same trap, which means the seemingly plausible explanation of $E_{1,PD4}$ being a bulk InGaAs trap located outside of the quantum well region is in fact not correct. That this more unconventional structure, with its increased local strain and wider range of material compositions might exhibit different deep levels is perhaps not surprising.
Figure 3.30 Trap profile for 0.12 eV trap \( E_{1,PD4,DLTS} \) in PD4.
TABLE 3.3
SUMMARY OF STRAINED-WELL QUANTUM WELL PHOTODIODE (PD4) TRAP PARAMETERS

<table>
<thead>
<tr>
<th>Trap Type</th>
<th>E (eV)</th>
<th>σ (cm$^2$)</th>
<th>J (mA/cm$^2$)</th>
<th>Possible location or origin</th>
</tr>
</thead>
<tbody>
<tr>
<td>LFNS</td>
<td>0.15</td>
<td>9.15×10$^{19}$</td>
<td>0.8</td>
<td>GaAsSb bulk in QW</td>
</tr>
<tr>
<td></td>
<td>0.26</td>
<td>6.41×10$^{17}$</td>
<td>3.3</td>
<td>---</td>
</tr>
<tr>
<td>DLTS</td>
<td>E$_c$+0.12</td>
<td>2.07×10$^{18}$</td>
<td>---</td>
<td>GaAsSb bulk in QW</td>
</tr>
</tbody>
</table>

3.5 Summary of deep level characterization of InGaAs/GaAsSb photodiodes

A comprehensive deep level characterization study on different types of InGaAs/GaAsSb photodiodes has been performed. Some commonality in deep levels was observed in similar structures (e.g., a donor-like level at ~0.11 eV and acceptor-like level at 0.43 eV in conventional MQW devices), while others were unique to specific device designs (e.g., 0.21 eV level in PD2, and the two levels in PD4). The impact of strain on deep levels was also investigated by comparison of structures with different strains. It has been found that while activation energy does not depend strongly on strain, capture cross section can be significantly influenced by strain. This then directly affects the probability of carriers being captured by deep levels. Taken together, the above results indicate the strong dependence of deep levels characteristics on the details of the device structures. However, it should be noted that the comparison of deep levels extracted here is based on the assumption that the activation energy level does not change appreciably with ternary composition over the limited range explored. For GaAsSb, several traps have been found to be independent of Sb mole fraction, with electron traps tracking the conduction band edge and hole traps tracking the valence band edge [31, 39].
The trap signatures and properties identified here are expected to assist both in future material growth optimization studies, as well as to provide guidance to device designers on approaches to mitigate the deleterious effects of deep levels in MQW photodetectors.
4.1 Brief review of GaAs FETs

GaAs based devices are of particular interest for high speed circuit applications, mostly because of the high electron mobility and semi-insulating substrates. The lack of a high quality insulator/semiconductor interface makes the Schottky-contact gate the default approach for GaAs-based FETs. Although GaAs based MESFETs, HEMTs, and pHEMTs have been widely used in RF blocks such as power amplifiers, low-noise amplifiers, and switches, they all suffer from a common problem of a relatively low gate barrier height that can result in substantial gate leakage current. As a consequence, the forward gate bias is restricted to a small voltage, usually smaller than 0.7 V, in order to avoid excessive gate current. Consequently, in order to handle large gate voltage swings, the device must operate in depletion mode with a negative threshold voltage. Both positive and negative power supplies are thus needed for drain and gate biases, which increases the complexity of the overall circuit and system.

In Contrast, MOS structures can have significant advantages over Schottky-gate approaches, primarily due to the large band gap of gate dielectric, which results in low leakage current. Historically, significant effort has been expended trying to identify a suitable gate insulator on GaAs. SiO₂, SiNx, and Al₂O₃ (among others) have been studied
as gate insulators, but all of them have exhibited the problem of an extremely high
density of interface states, leading to unsatisfactory device performance. Breakthroughs
have been made since the 1990s, with the advent of high quality high-k gate dielectric
deposition on GaAs first by MBE [40, 41] and later by atomic layer deposition (ALD)
[42-46]. The good electrical performance of devices fabricated with these approaches
demonstrates that these materials are promising candidates for achieving high
performance III-V MOSFETs.

An alternative approach to the use of a deposited oxide is to use InAlP oxide as
the gate dielectric. Since InAlP oxide can be formed by wet thermal oxidation of
epitaxially-grown In$_{0.5}$Al$_{0.5}$P (which is lattice matched to GaAs), it can be easily
integrated into conventional III-V FET fabrication processes with low cost and minimal
disruption. Over the past few years, researchers at the University of Notre Dame have
reported four generations of GaAs- and InGaAs-channel MOSFETs using InAlP oxide as
the gate dielectric [1, 47-51]. To further improve the device performance, one of the
critical issues is obtaining the lowest possible interface state density at the InAlP-
oxide/channel interface. To quantitatively evaluate these interface states, MOS capacitors
on two different epitaxial test structures were fabricated, and interface state densities
were measured by both capacitance-voltage and conductance methods, as described in
Chapter 2.

As another potentially attractive gate oxide, ALD-grown Al$_2$O$_3$ has become one
of the most popular materials in recent years. The high dielectric constant of Al$_2$O$_3$ makes
it attractive for FET gate dielectric application since the oxide can be grown thicker
without reducing the gate capacitance or the gate control ability, while at the same time
gate leakage current due to tunneling is strongly suppressed. Interface state densities as low as $\sim 10^{12} \text{ cm}^{-2} \text{eV}^{-1}$ have been achieved, which makes $\text{Al}_2\text{O}_3$ a promising candidate as gate dielectric for GaAs-based RF transistors [52-54]. However, most studies to date have centered around direct deposition of $\text{Al}_2\text{O}_3$ on top of the channel layer. This nearly always results in exposure of the channel surface to atmosphere ambient, and increases the possibility of surface contamination. As part of the MOS interface quality examination performed here, a buried-channel design with lattice-matched InGaP as the barrier between $\text{Al}_2\text{O}_3$ and the channel is explored.

4.2 InAlP oxide as gate dielectric

As the first part of this chapter, the fabrication and characterization of MOS capacitors with InAlP oxide as the gate dielectric are described.

4.2.1 Fabrication of MOS capacitors using InAlP oxide as gate oxide

MOS capacitors were fabricated on test wafers Y110 and Y111 (grown by MBE through a collaboration with RFMD, Inc.), which have structures as shown in Figure 4.1. The Y110 heterostructure consists of a semi-insulating GaAs substrate, a 2000 Å GaAs buffer layer, an undoped isolation superlattice of AlGaAs/GaAs with total thickness of 2580 Å, a 9000 Å GaAs channel layer (with the top 1000 Å more lightly doped at $N_d=3\times10^{17} \text{ cm}^{-3}$, and a 8000 Å n+ sub-channel ($N_d=2\times10^{18} \text{ cm}^{-3}$)), a 70 Å highly doped InAlP layer ($N_d=1\times10^{18} \text{ cm}^{-3}$) lattice matched to GaAs, and a heavily doped 900 Å GaAs cap layer ($N_d=4.5\times10^{18} \text{ cm}^{-3}$). The Y111 heterostructure has exactly the same structure as Y110, except that it includes a 20 Å thick oxidation stop layer of InGaP inserted between the InAlP and the GaAs channel.
The fabrication of MOS capacitors on these epitaxial structures is very similar to the non-self-aligned MOSFET process demonstrated by Zhang [51], which uses regional oxidation for the gate dielectric formation. The process details are briefly described below.

After the sample is cleaned in solvent and dipped in a dilute HCl:DI solution (1:2) to remove the native oxide on the GaAs cap layer, a thin layer of silicon nitride is deposited on the surface by PECVD. The oxide pattern is then transferred into the SiN\textsubscript{x} by contact lithography and etching in BOE. The GaAs cap layer is then etched, using the SiN\textsubscript{x} gate window as an etch mask, using 10:1 citric acid (citric acid powder: H\textsubscript{2}O by weight =1:1):H\textsubscript{2}O\textsubscript{2}. The sample is then immediately oxidized in a dedicated furnace in a water vapor/N\textsubscript{2} ambient. Oxidation time is critical in this step, especially for structure Y110 since it does not include an oxidation stop layer. From VASE measurements, it takes about 16 minutes to fully oxide the 70 Å InAlP layer in these structures at a
typical oxidation temperature of 440 °C, resulting in an InAlP oxide layer thickness of approximately 115 Å. An ohmic contact metal stack of AuGe/Ni/Au, with AuGe to Ni thickness ratio of 6:1, is then deposited on the GaAs cap layer by thermal evaporation after BOE etching of SiNₓ in the ohmic region, which is also defined by contact photolithography. After metal deposition, the ohmic contacts are annealed in a rapid thermal processor (RTP), typical conditions are 405 °C for 5 s. The contact resistance obtained from TLM test structures is typically around 0.08 ohm-mm. Finally, the gate pattern is defined by photolithography, and Ti/Au gate electrodes are formed by electron-beam evaporation and lift-off. For the MOS capacitors evaluated here, the lateral distance between gate metal and ohmic metal is only a few microns, so that the series resistance is minimized. Figure 4.2 shows a schematic cross section of a completed MOS capacitor on wafer Y111. Capacitors on the Y110 wafer have the same structure except without the InGaP oxidation stop layer beneath the oxide.

Figure 4.2 Schematic cross section of a MOS capacitor on the Y111 heterostructure.
4.2.2 Current-voltage, capacitance-voltage and conductance measurements of MOS capacitors

Current-voltage characteristics were measured using an Agilent 4156 semiconductor parameter analyzer. Typical measured I-V curves for 40 µm * 40 µm capacitors fabricated using a 16 minute oxidation time are shown in Figure 4.3. These devices exhibit low leakage current, comparable to previous reports [49-50]. The leakage current densities at -2 V are \(8.5 \times 10^{-5} \text{ A/cm}^2\) and \(2.6 \times 10^{-5} \text{ A/cm}^2\) for Y110 and Y111, respectively. This small difference between the reverse leakage currents of the two structures may be due to the effective increase of the gate dielectric thickness due to the InGaP layer in Y111. Overall, however, the small leakage current density indicates the good insulating properties of InAlP oxide.

![Figure 4.3 Typical I-V characteristics measured for 40 µm * 40 µm capacitors with structures Y110 and Y111, oxidized for 16 minutes at 440 °C.](image-url)
Although VASE studies suggest that 16 minutes is sufficient to fully oxidize the InAlP layers in these structures, the impact of oxidation time on leakage current was also directly assessed experimentally. Oxidation times from 14 minutes to 21 minutes were explored, while keeping the rest of the process conditions the same. I-V curves of these capacitors are shown in Figure 4.4. It can be seen that the leakage current decreases as the oxidation time increases until approximately 16 minutes, after which the current saturates. This suggests that 16 minutes is in fact just enough to fully oxidize the InAlP layer, consistent with the VASE measurements. Precise control of the oxidation time can be quite critical, since extra oxidation may damage the insulator/semiconductor interface, and thus increase the interface trap density.

Figure 4.4 I-V characteristics for Y111 capacitors with oxidation times ranging from 14 minutes to 21 minutes.
Frequency dependent capacitance-voltage characteristics of capacitors with both heterostructures were also measured using an Agilent E4980A LCR meter. Measurement frequencies from 1 kHz to 1 MHz were used. Figures 4.5 and 4.6 show the typical measured and theoretical CV for 40 µm × 40 µm capacitors for the two structures. It can be seen that there is significant frequency dispersion for both types of capacitors in both the depletion and accumulation regions. In addition, significant voltage stretch-out is exhibited between the measured and the theoretical capacitance. Both phenomena are clear indications of high $D_{it}$ [19].

![Figure 4.5 Measured (solid line) and theoretical (dashed line) capacitance-voltage characteristics for MOS capacitors fabricated on the Y111 structure, for full oxidation (16 minutes oxidation time).](image-url)
In order to characterize the density and distribution of interface traps (Dit), the Terman method [18-19], as discussed in section 2.3.1, was implemented by comparing the measured 1 MHz CV and the theoretically-predicted CV characteristics. Series resistance was neglected in the calculation, since for both the Y111 and Y110 structures, the very thick heavily doped subchannel layer and the low contact resistance that were observed led to insignificant series resistance effects. By constructing the $\psi_s$ versus $V_G$ relationship, the Dit distribution was extracted from equations (2.12) and (2.13). The resulting Dit versus energy for the two structures are plotted in Figure 4.7 and Figure 4.8, respectively.
Figure 4.7 $D_{it}$ of Y111 structure extracted using the Terman method.

Figure 4.8 $D_{it}$ of Y110 structure extracted using the Terman method.
It can be seen that the extracted $D_{it}$ for both structures are on the order of $5 \times 10^{12} \sim 10^{13} \text{ eV}^{-1} \text{cm}^{-2}$, which is comparable to published values for $D_{it}$ of Al$_2$O$_3$/GaAs channel interface [52-54]. We also notice that the extracted $D_{it}$ increases abruptly for energies around $\sim 1.0 \text{ eV}$. This can be anticipated from the CV characteristics shown in Figure 4.5 and Figure 4.6, since the measured capacitance saturates for gate bias from 0 V to -1 V, indicating that the Fermi level has entered a high $D_{it}$ region, which causes the capacitance to change more slowly with gate bias before reaching full depletion of the channel layer.

In addition to the Terman method, the conductance method as discussed in section 2.3.2 was also applied to the analysis of the capacitors to provide a different approach to determining the $D_{it}$. The conductance was measured by sweeping the frequency from 100 Hz to 1 MHz at several gate bias conditions, using an Agilent E4980A LCR meter. In order to probe deeper into the band gap without using extremely low frequencies, the temperature was increased to 150 °C in addition to room temperature measurement. Instead of a conventional conductance versus frequency plot, a false-color conductance map was constructed as shown in Figure 4.9 (Y111) and Figure 4.10 (Y110). The energy level corresponding to each frequency was calculated as outlined previously, and a constant capture cross section of $10^{-15} \text{ cm}^{-2}$ was assumed in order to simplify the extraction. The resulting $D_{it}$ versus energy obtained is shown in Figure 4.9 (c) and Figure 4.10 (c) for structures Y111 and Y110, respectively.
Figure 4.9 Conductance map for Y111 MOS capacitor measured at 150 °C (a) and at 25 °C (b). Dit extracted from the conductance peaks is shown in (c).
Figure 4.10 Conductance map for Y110 MOS capacitor measured at 150 °C (a) and at 25 °C (b). Dit extracted from the conductance peak is shown in (c).

From Figure 4.9 (c) and Figure 4.10 (c), one can see that the estimated Dit is on the order of $10^{13}$ eV$^{-1}$cm$^{-2}$, in reasonably close agreement with the results obtained from the Terman method. One can see some “misalignment” of the Dit between the two temperature measurements in Figure 4.9 (c). Given the severe Fermi level pinning in this
structure, the $D_{it}$ should just be treated as rough estimates. It can also be seen that the functional form of the $D_{it}$ distribution with energy is rather different than that found using the Terman method.

By comparing the $D_{it}$ in the two structures, it can be seen that the InGaP oxidation stop layer does not necessarily improve the interface quality, and so (at least for the fabrication process parameters used here) devices with InGaP did not demonstrate any significant performance improvement. Furthermore, the $D_{it}$ values extracted here using both methods above are about an order of magnitude higher than previous reports of $8 \times 10^{11}$ eV$^{-1}$cm$^{-2}$ by Li [1]. However, the structure used by Li included a 630 Å thick InAlP layer, almost 10 times the thickness of the InAlP layer used here, which may have a significant impact on the interface quality.

4.3 Al$_2$O$_3$ as gate dielectric

As a second part of this chapter, ALD-grown Al$_2$O$_3$ is investigated as a potential gate dielectric using MOS capacitor structures similar to the previous section. $D_{it}$ was extracted under various process conditions to see the impact of surface treatment and annealing process.

4.3.1 Fabrication of MOS capacitors using Al$_2$O$_3$ as gate oxide

MOS capacitors were fabricated on wafer X1 with structure as shown in Figure 4.11 (also grown by RFMD using MBE technique). The heterostructure consists of a semi-insulating GaAs substrate, a 2000 Å AlGaAs buffer layer, a delta doping layer with doping concentration of $3 \times 10^{12}$ cm$^{-2}$, a 35 Å undoped barrier layer of AlGaAs, a 125 Å
undoped InGaAs pseudomorphic channel layer, a 20 Å undoped InGaP isolation layer, and a 250 Å heavily doped GaAs cap layer with doping concentration of $4 \times 10^{18} \text{cm}^{-3}$.

<table>
<thead>
<tr>
<th>Layer Description</th>
<th>Doping/Concentration</th>
</tr>
</thead>
<tbody>
<tr>
<td>250 Å n+ GaAs cap</td>
<td>4e18</td>
</tr>
<tr>
<td>20 Å uid InGaP isolation</td>
<td></td>
</tr>
<tr>
<td>125 Å uid In$<em>{0.22}$Ga$</em>{0.78}$As channel</td>
<td></td>
</tr>
<tr>
<td>35 Å uid Al$<em>{0.22}$Ga$</em>{0.78}$As back barrier</td>
<td>delta doping (Si) 3e12</td>
</tr>
<tr>
<td>2000 Å uid Al$<em>{0.22}$Ga$</em>{0.78}$As buffer</td>
<td></td>
</tr>
<tr>
<td>SI GaAs substrate</td>
<td></td>
</tr>
</tbody>
</table>

Figure 4.11 Device structure of X1 wafers.

As briefly discussed previously, gate oxide is deposited directly on top of the channel layer in most studies [40-46], which will result in the interface states located right along the channel surface, leading to very strong interaction with carrier. In this work, a thin InGaP barrier layer is inserted between the Al$_2$O$_3$ and the channel, thus making any interface states form on top of the InGaP instead of at the top of the channel. Furthermore, since InGaP is a large band gap material (1.92 eV versus 1.42 eV for GaAs and 1.11 eV for In$_{0.22}$Ga$_{0.78}$As), the fact that $D_{it}$ peaks near band edge and decreases as approaching the mid-gap makes the defect further away from the GaAs or InGaAs channel band edge. Hence the overall impact of interface states on the channel carrier may be reduced by the additional InGaP layer.

The fabrication process for MOSCAP using ALD grown Al$_2$O$_3$ is very similar to the InAlP oxide capacitor described in the previous section, so only the unique processes
will be discussed. After wet etch of the GaAs cap layer using SiNₓ as the gate mask, instead of using a furnace to wet oxidize the semiconductors, the Al₂O₃ is deposited by ALD at 300° C with precursors of Tri-Methyl Aluminum (TMA) and H₂O. Typical as-deposited oxide thickness is around 200 Å, as determined by both VASE and P-6 stylus profiler. An ohmic metal stack of AuGe/Ni/Au which is similar to that used for the InAlP oxide devices is then deposited and annealed at 410°C for 20 s to achieve low-resistance ohmic contact. The contact resistance obtained from TLM test structures is typically around 0.4 ohm-mm. Fabrication concludes with deposition of a Ti/Au gate electrode by electron-beam evaporation and lift-off. Due to the enhancement-mode nature of the structure, the surface is fully depleted after cap layer removal. Thus in order to avoid excess series resistance due to surface depletion in the ungated region, the gate metal is designed to fully overlap the oxide region. Figure 4.12 shows a schematic cross section of a completed Al₂O₃ MOS capacitor on wafer X1.

![Figure 4.12 Schematic cross section of a MOS capacitor on the X1 structure.](image-url)
4.3.2 Interface quality characterization using capacitance and conductance methods

Since the surface is exposed to lab ambient before oxide deposition, uncontrolled surface oxidation and an associated high density of interface states is expected. Thus surface treatment is normally required for ALD grown oxide. Researchers have reported a wide range of pre-treatments for ALD oxides in order to improve $D_{it}$, and it is found that pre-deposition soaking with certain solutions (e.g., HCl, HF, ammonium hydroxide ($\text{NH}_4\text{OH}$), ammonium sulfide ($\text{(NH}_4\text{)}_2\text{S}$)), as well as post-deposition annealing (PDA) often show significant improvements [42-46, 52-54]. In order to obtain a baseline for evaluating the impact of treatments for the structure studied here, four test samples were prepared under different conditions, including one control sample without any special treatment, one sample with 20 mins ($\text{NH}_4\text{)}_2\text{S}$ treatment, one sample with 500°C PDA for 30s in nitrogen ($\text{N}_2$) ambient, and one sample with both 20 mins ($\text{NH}_4\text{)}_2\text{S}$ treatment and 500°C PDA for 30s in N$_2$. The resulting capacitance-voltage characteristics of the four samples are shown in Figure 4.13. Different degrees of stretch-out between the measured 1 MHz and theoretical C-V curve and horizontal shift of the C-V curve at different measurement frequencies can be observed from the figure, which indicates significant change in interface traps and oxide traps, respectively. Note that the oxide thickness used in the theoretical C-V calculation was measured by VASE after PDA, due to the fact that the thickness of Al$_2$O$_3$ will decreases after high temperature process. It is clearly that sulfide treatment improves the surface pinning by comparing Figure 4.13 (a) and (b), and after incorporating PDA the surface states and oxide defects are further reduced by comparing Figure 4.13 (b) and (d), while PDA without sulfide treatment barely improves the interface quality by comparing Figure 4.13 (a) and (c). This is attributed to sulfide
bonds preventing surface oxidation, while high temperature post-annealing “heals” broken bonds in the Al$_2$O$_3$ film and also improves surface quality.

Figure 4.13 Measured and theoretical C-V for MOS capacitors on structure X1 with several pre- and post-treatments. (a). no special treatment. (b). 20 mins (NH$_4$)$_2$S soaking. (c). 500 °C 30 s nitrogen PDA. (d). 20 mins (NH$_4$)$_2$S soaking + 500 °C 30 s nitrogen PDA.
I-V characteristics of four test samples above were also measured and shown in Figure 4.14. It can be seen that the leakage current in both forward and reverse directions only increased slightly after treatment.

![Figure 4.14 I-V characteristics of four test samples](image)

Based on this first crude experiment showing significant impact of pre- and post-treatments on capacitor operation, was performed. For sulfide treatment, both 10 mins and 20 mins were evaluated for the same PDA condition; the difference in $D_{it}$ is indiscernible, which suggests that the $D_{it}$ does not strongly depend on sulfide dipping time, at least within this range of conditions. As for PDA, several experimental parameters need to be adjusted in order to optimize the condition. Thus a design of experiment (DOE) based on the Taguchi method was designed and performed, which involved using orthogonal arrays to organize the parameters that affect the process and the levels for each parameter. Instead of having to test all possible combinations, the
Taguchi method tests pairs of combinations. Table 4.1 below shows the DOE that includes changes in annealing temperature, time, and gas ambient. The measured C-V characteristics from 1 KHz – 1 MHz frequencies for test samples are shown in Figure 4.15 and Figure 4.16. Note that only N₂ is used for samples #10 - #15 because it was found from the C-V of #1 to #9 that forming gas and nitrogen did not exhibit significant differences. This allowed elimination of one experimental factor, and a considerable reduction in experimental runs required.

<table>
<thead>
<tr>
<th>sample</th>
<th>temperature</th>
<th>time</th>
<th>gas</th>
</tr>
</thead>
<tbody>
<tr>
<td>#1</td>
<td>500 C</td>
<td>30 s</td>
<td>N₂</td>
</tr>
<tr>
<td>#2</td>
<td>500 C</td>
<td>1 min</td>
<td>forming gas (FG)</td>
</tr>
<tr>
<td>#3</td>
<td>500 C</td>
<td>5 mins</td>
<td>FG</td>
</tr>
<tr>
<td>#4</td>
<td>550 C</td>
<td>30 s</td>
<td>N₂</td>
</tr>
<tr>
<td>#5</td>
<td>550 C</td>
<td>1 min</td>
<td>N₂</td>
</tr>
<tr>
<td>#6</td>
<td>550 C</td>
<td>5 mins</td>
<td>FG</td>
</tr>
<tr>
<td>#7</td>
<td>600 C</td>
<td>30 s</td>
<td>FG</td>
</tr>
<tr>
<td>#8</td>
<td>600 C</td>
<td>1 min</td>
<td>N₂</td>
</tr>
<tr>
<td>#9</td>
<td>600 C</td>
<td>5 mins</td>
<td>N₂</td>
</tr>
<tr>
<td>#10</td>
<td>450 C</td>
<td>30 s</td>
<td>N₂</td>
</tr>
<tr>
<td>#11</td>
<td>450 C</td>
<td>1 min</td>
<td>N₂</td>
</tr>
<tr>
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<td>450 C</td>
<td>5 mins</td>
<td>N₂</td>
</tr>
<tr>
<td>#13</td>
<td>480 C</td>
<td>30 s</td>
<td>N₂</td>
</tr>
<tr>
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</tr>
<tr>
<td>#15</td>
<td>480 C</td>
<td>5 mins</td>
<td>N₂</td>
</tr>
</tbody>
</table>
Figure 4.15 C-V characteristics of PDA test samples based on the Taguchi method (continued on next page).
Figure 4.16 C-V characteristics of PDA test samples based on the Taguchi method.
Since C-V stretch-out and horizontal shift at different frequencies represent the interface and oxide quality, respectively, some general trends of PDA conditions on interface states and oxide traps can be inferred from the above test. As for the annealing temperature, it can be seen that as the temperature is raised above 500°C, either oxide or semiconductor crystal is severely degraded since the 1 MHz C-V significantly deviates from the theoretical value and the frequency dispersion becomes very large. It also makes intuitive sense that at 500°C significant As desorption can occur [55-57]. Thus temperature between 450°C – 500°C is more appropriate for the PDA process. For the annealing time, the oxide quality is improved (less frequency dispersion) as the annealing time increases at a fixed temperature (e.g., at 450°C or 480°C).

Similar to the previous section, the Terman method is then used to characterize $D_{it}$. By constructing the $\psi_s$ versus $V_G$ relationship, the $D_{it}$ distribution was extracted, and the resulting $D_{it}$ versus energy for samples #1, #12 and #15 are plotted in Figure 4.17, since these three samples have the lowest stretch-out and frequency dispersion in their C-V characteristics. The energy in the $D_{it}$ plots below uses the InGaAs valence band edge as the reference for zero energy. It can be seen that the three samples have very similar $D_{it}$ distribution signature, that is, the $D_{it}$ has a peak value of $\sim10^{13}$ cm$^{-2}$eV$^{-1}$ at around 0.6 eV – 0.7 eV, then reaches as low as $\sim10^{12}$ cm$^{-2}$eV$^{-1}$ from 0.7 eV to 1 eV, and finally increases dramatically as it approaches conduction band edge.
The conductance method was also applied to the analysis of the capacitors in addition to the Terman method. The conductance was measured by sweeping the frequency from 100 Hz to 1 MHz at several gate bias conditions. False-color conductance maps were constructed as shown in Figure 4.18 (a), (b) and (c) for test samples #1, #12 and #15. A large dispersion was found at frequencies below 1 KHz, which might indicate a high $D_{it}$ near mid gap. The energy level corresponding to each frequency was calculated, and the resulting $D_{it}$ versus energy is shown in Figure 4.18 (d) for these three test samples.
It can be seen that the $D_{it}$ extracted from conductance method is very close to Terman method, which is on the order of $10^{12} \text{ cm}^{-2}\text{eV}^{-1}$ within an energy range of $0.8 \text{ eV} – 1 \text{ eV}$. However, the conductance method didn’t reveal the traps deeper in the bandgap, primarily due to the fact that the conductance peaks become obscured by the conductance background at lower frequencies. For simplicity, a constant capture cross section of $10^{-15} \text{ cm}^{-2}$ was assumed during the calculation in order to simplify the extraction. This will lead to some error in the extracted $D_{it}$, but the trends and order of magnitude are expected to be preserved.
Figure 4.18 Conductance map for test samples (a) #1, (b) #12, and (c) #15. Dit extracted from the conductance peaks is shown in (d).

Many researches have reported on efforts to improve the interface quality of Al$_2$O$_3$ on GaAs or InGaAs channel, and the reported Dit value is typically around $10^{12}$ cm$^{-2}$eV$^{-1}$ [52-54]. The study of buried-channel structures reported here exhibits comparable Dit value, however, with the advantage that the interface states are located between the Al$_2$O$_3$ and the InGaP. Although the interface states can still have a similar
impact on the modulation of surface potential (such as stretch-out of the C-V curves), the buried channel design results in less direct interaction between channel carriers and interface traps, thus this structure may exhibit better performance such as lower noise and higher oxide breakdown. This is at the expense of degraded channel electrostatics, however, but for microwave applications (as opposed to high-density logic) this is of much less concern.
CHAPTER 5.
SUMMARY AND FUTURE WORK

Since deep levels are important material properties that can limit device performance, a comprehensive study of deep levels in two emerging device technologies has been undertaken in this work. Both quantum well InGaAs/GaAsSb photodiodes for mid-IR detection, and GaAs-based MOS capacitors using InAlP oxide and Al$_2$O$_3$ as gate dielectric for the purpose of improving interface quality in GaAs-based MOSFETs have been evaluated. A range of characterization tools and approaches were used to assess and quantify the deep levels, including deep level transient spectroscopy (DLTS), low frequency noise spectroscopy (LFNS), random telegraph signals (RTS) characterization, and capacitance- and conductance-based methods for evaluating oxide/semiconductor interface states.

As a first part of the work reported here, deep levels in quantum well InGaAs/GaAsSb photodiodes with different structures were characterized. While a few of the deep levels were found to exist only in certain heterostructure designs, most defects were universally present across the devices studied here. Strain-related effects – primarily manifested in the cross-section – were also observed for some levels by comparing structures with different material composition. Moreover, devices with a strained quantum well structure were also characterized in contrast to conventional multiple quantum well structures. New traps were revealed, primarily due to the strain introduced;
additional work is required to fully quantify the role of strain in the formation of these new defects. The work done here is mostly focused on deep levels in different structures with changing material composition. However, fabrication processing is also a significant potential source for defect formation, and by changing some critical process conditions (for example, wet vs. dry etching or alternative surface passivations) chemical bonding in certain regions might change, which can potentially influence the type and density of defects in these devices. Thus process impact on defects could be a fruitful topic for related future work.

To characterize deep levels in the work described above, several characterization tools were used, including DLTS, LFNS and RTS. From the measurements, it has been shown that each technique has its own strengths and weaknesses in practice, beyond the fundamental differences discussed in Chapters 1 and 2. As the most general technique for characterizing traps, DLTS is difficult to use for measuring efficient generation-recombination centers, due to the comparable electron and hole capture and emission rates. As an alternative method, LFNS can measure both traps and GR centers. However, it is unable to reveal some important properties of deep levels, such as density, spatial profile, and type (e.g., donor or acceptor). RTS provides a complementary technique to LFNS, and can measure type of the deep level. However, RTS cannot always be observed easily during measurement, and sometimes requires small area devices with sub-micron geometry. While this is not a problem for many devices, it is not very practical for large-area photodetectors, such as those used here. It also requires a relatively low defect density, since single electron transition behavior that results RTS can only be observed when only a few electrons are experiencing transitions. Defects with high density will
average out the electron transition, resulting in a many-level system with indistinct transitions. Consequently, in practice sometimes all of these methods are needed to obtain a full understanding of the deep levels in devices.

As the second part of the work, interface quality of GaAs based MOS capacitors with InAlP oxide and Al$_2$O$_3$ as gate oxide was studied. For InAlP oxide, although four generations of GaAs and InGaAs channel MOSFET incorporating InAlP native oxide have been explored previously, no detailed work had been done to evaluate interface quality for thin oxides. By using the Terman capacitance method and the conductance mapping method, interface state densities of $10^{12} - 10^{13}$ cm$^{-2}$eV$^{-1}$ were extracted between the InAlP oxide and GaAs channel. Although this $D_{it}$ value is on the high end of what is commonly observed for deposited oxide films, the wet oxidation process makes it easier to be integrated into current GaAs FET process in industry. For Al$_2$O$_3$ deposited by ALD, instead of a direct deposition of oxide on the channel layer, an InGaP barrier layer was incorporated to improve the interface quality between oxide and InGaAs channel. Some surface treatments such as sulfide soaking and post-deposition annealing were studied in detail to see the effects on $D_{it}$. Interface state density was then found to be $\sim 10^{12}$cm$^{-2}$eV$^{-1}$ in the upper half of InGaAs band gap.
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