GATING OF TWO DIMENSIONAL MATERIALS USING SOLID POLYMER ELECTROLYTES AND FERROELECTRICS

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Abstract

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Two-dimensional (2D) materials, particularly graphene and transition metal dichalcogenides (TMDs), have been the subject of many recent studies because of their unique mechanical and electrical properties. All the bonds are in-plane, and the layers are separated by a van der Waals gap. While most properties can be characterized by measuring the unmodified materials, many electrical properties require the charge state of the material to be modulated. For traditional semiconductors, this is achieved by field-effect gating through a dielectric combined with substitutional doping. However, the lack of dangling surface bonds makes the deposition of a gate dielectric challenging, and methods for controlled substitutional doping have not yet been developed. Solid polymer electrolytes (SPEs), which consist of a salt dissolved in a polymer, offer a relatively simple solution. By using the SPE in the place of a gate dielectric, ions in the SPE are driven to close proximity ($\sim$1 nm) of the material surface to induce image charges in the 2D material. The ion and corresponding image charge layers are collectively known as an electrostatic (or electric) double layer (EDL). The EDL can induce charge carrier densities in the material in excess of 10^{14} cm^{-2}.

The work presented in this dissertation details ways of using EDL-induced sheet charges to open up new applications in the field of nanoelectronics. By tuning the

glass transition temperature of the SPE, the EDL retention time can be increased by six orders of magnitude at room temperature while still achieving charge carrier densities in excess of 10^{14} cm^{-2}, enabling unique hardware security. We also investigate applying large electric fields over the SPE, which causes volumetric change in 2D electronics due to ion intercalation. 2D devices typically are top-gated by the SPE. However, in this work, backgating by an SPE is demonstrated for the first time. As well, we explore partial switching of the ferroelectric material $HfZrO_2$ The objective is to use the ferroelectric in conjunction with a 2D channel to form a two-terminal resistive processing unit for use in hardware-based neural networks.

Dedication

For my family, who throughout my life has provided nothing but love and assistance.

Also for my Wife, who remained supportive through many late nights of research and writing.

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CHAPTER 1

INTRODUCTION

Sheet charges, theoretical, infinitesimally thin planes of charge, have long plagued the problem sets of physics students, because they provide a good example of how Maxwell's equations deal with free charge. However, in material science, sheet charges can be a good approximation for physical phenomena, such as charged trap states at a crystal interface, the two dimensional electron gas in a MOSFET, or charge within a two dimensional system, such as graphene. In this work, I will focus on two such sheet charge devices: first, electrostatic double layers induced by the ions in an electrolyte, and second, the remnant polarization of a ferroelectric.

1.1 Ions

Ions, molecules with a nonzero charge, are important components of devices we use every day, like batteries and sensors, and are even integral for the biological processes required to sustain life. For example Na^+, K^+, Ca^{2+} and Cl^- are all used in biological systems as charge carriers, through which signals can propagate from cell to cell, triggering events such as mitosis (cell division) and muscle contraction.[8] A lack, or excess of certain ions in the brain, or the inability to properly detect the presence of those ions can cause problems ranging from depression to brain death. Ions are also vital for synthetic devices, such as batteries, where electrochemistry occurring within the cell provides energy to power a portable device. In such cells, ions travel through an electrolyte to electrodes where they undergo chemical reactions that produce an electric current.

Ions are also integral to the materials used to fabricate integrated circuits as sources of fixed charge for p- or n-type doping. These ions can either be substitutional dopants, occupying the lattice sites of the host atoms, or interstitial dopants where the atoms occupy non-lattice sites. Doping is typically performed one of three ways. The first is ion implantation, where ions are accelerated and collided with the target substrate.[9] Second, ions can be deposited on a surface by using a spin-on glass containing a high concentration of dopant atoms that will diffuse into the wafer at high temperatures.[10] A third method is to simply add dopants to the source material from which the boule is grown.[11]

In this work, I show how electrolytes, similar to those used in batteries, can be used in conjunction with two-dimensional (2D) materials to investigate the electronic properties of the 2D materials. In addition I demonstrate device operation that is only made possible by the combination of an electrolyte and a 2D material.

1.2 Electrostatic Double Layers

An electrostatic (or electric) double layer (EDL) is comprised of parallel sheets of charge at the interface between two materials. One example of a device that uses EDLs is an EDL capacitor (EDLC) for which the dielectric is replaced with an electrolyte (*i.e.* an electrically insulating material with mobile ions). By using an electrolyte in the place of a dielectric in the EDLC, bias applied across the electrodes migrates ions to within 1 nm of the electrode surfaces. The ions near the channel and their image charges are collectively known as an EDL. The EDL effectively decreases the electrode separation distance from the physical thickness of the capacitor to the distance between the ion and its induced image charge ($\sim$1 nm). Because the capacitance is inversely related to the charge separation distance, close proximity of the ion to its image charge, as shown in the schematic of an EDLC in Figure 1.1, creates a large capacitance, on the order of several μF/cm^2.[12]

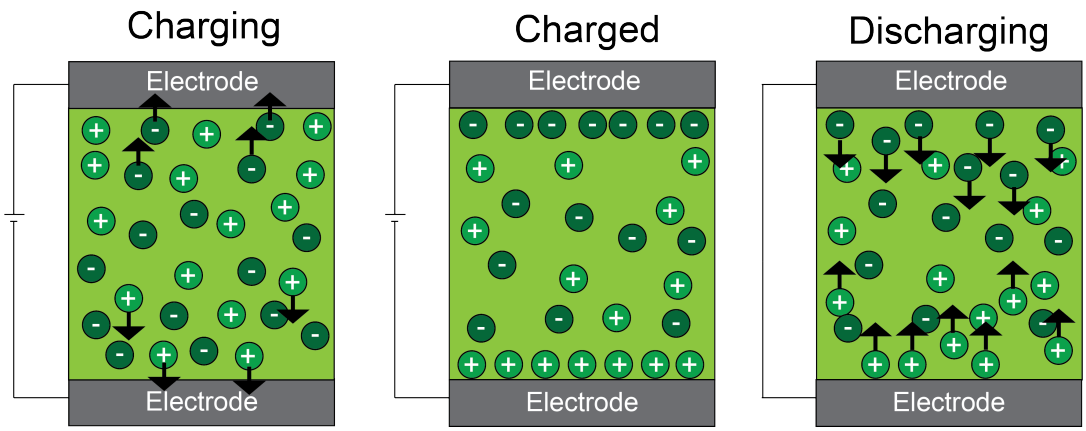

Figure 1.1. Schematic of an EDL capacitor charging (left) by establishing the EDL, charged (center), and discharging (right) by dissolving the EDL.

Electrolyte gating (*i.e.*, using an electrolyte as a gate dielectric in a FET) is a tool for inducing large sheet carrier densities ($> 10^{14}$ cm^{-2} for both holes and electrons) in channel materials such as graphene[13], 2D semiconductors[14], and topological insulators.[15] In this electrolyte-gated structure, the EDLC serves as a FET gate capacitor. The properties of the EDLC preserve the low-leakage current and increase the gate capacitance that would normally be provided by a high-k dielectric in modern MOSFETs.[13, 12] Figure 1.2 demonstrates the operation of an EDL-gated transistor, with the ions homogeneously dispersed throughout the electrolyte when zero gate bias is applied (Figure 1.2, left). When a negative bias is applied to the topgate, the ions respond by forming layers at the gate/electrolyte and electrolyte/channel interfaces (Figure 1.2, center). The negative ions close to the semiconducting channel induce holes in the channel, promoting hole conduction. When a positive gate bias is applied (Figure 1.2, right), the opposite occurs, with the positive ions near the channel inducing electrons.

Electrolyte gating is attractive for investigating the electronic properties of new materials, because it can be used as a gating solution without the need for discovering a process to deposit a high-quality dielectric. Because of the lack of dangling surface bonds in van der Waals 2D materials it can be difficult to nucleate high quality dielectrics. This dielectric growth is required to make a MOSFET using a 2D semiconductor as the channel. By using an electrolyte gate as a replacement for the oxide gate stack, FET characteristics of 2D materials can be determined without requiring a dielectric growth recipe.

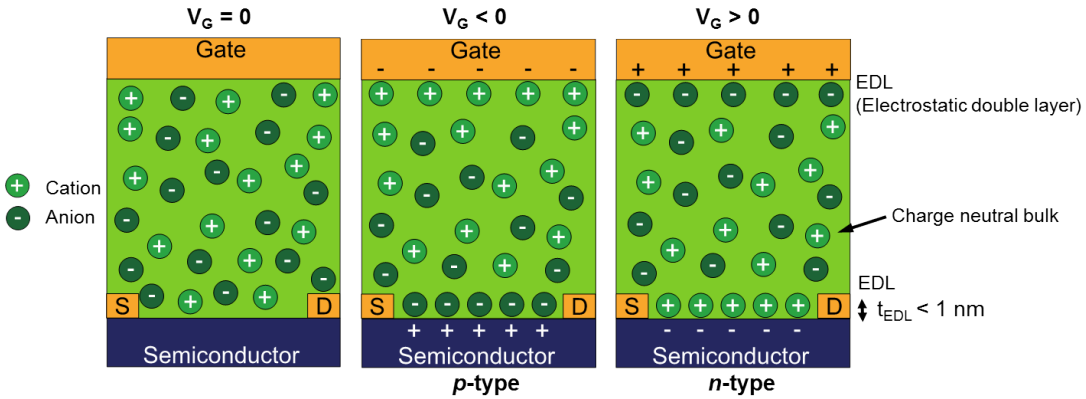

Figure 1.2. Schematic of an electrolyte gated FET operation. At $V_G = 0$ V, the cations and anions are distributed homogeneously throughout the electrolyte (left). When a positive gate bias is applied, anions are driven to the channel surface, inducing holes in the channel (center). When a negative gate bias is applied, cations are pushed towards the channel, inducing electrons in the channel (right).

EDL gating can also serve as a replacement for doping. This can be accomplished by forming an EDL at the surface of the channel and then immobilizing the ions. In this way, the ions remain fixed in their locations even without an applied bias and

the induced charge in the channel mimics the effect of a dopant. This is especially important for 2D materials because standardized substitutional doping strategies have not yet been developed. Furthermore, EDL-based doping is especially attractive for materials that are only one atomic or molecular layer thick, because EDL doping is a surface phenomenon which will decrease in intensity the with increasing distance from the interface.

1.3 Electrolytes

Electrolytes are materials containing mobile ions. One simple example is table salt in water, which is comprised of Na^+ and Cl^- dissociated in liquid water. The cations (Na^+) and anions (Cl^-) are solvated by H_2O, and because the H_2O is mobile, the ions are also mobile. However, saltwater is electrically conductive, and would create a short if applied to a device. In this work, the electrolytes of interest are those that are electrically insulating within a particular voltage range referred to as the electrochemical window. Therefore, they do not provide a leakage path in devices utilizing them as long as the applied voltage is within this range.

Ionic liquids are one type of electrolyte. These materials are known as "liquid salts" where the cations and are weakly coordinated with the anions, leading to low melting temperatures.[16] Essentially, the salt serves as its own solvent.[16] Common ionic liquids, such as N,N-diethyl-N-(2-methoxyethyl)-N-methylammonium bis (trifluoromethylsulphonyl) imide (DEME-TFSI) have been used for electrolyte gating.[17] One benefit to using ionic liquids is their large electrochemical window (the voltage range in which the electrolyte can be biased without catalyzing a chemical reaction). However one disadvantage is that ionic liquids are extremely hygroscopic. They absorb and retain water readily, which is difficult to remove due to the low vapor pressure of the material.[18] The presence of water increases the electrical conductivity of the ionic liquid, and therefore ionic-liquid gated devices that are not

prepared and measured in anhydrous environments require additional fabrications steps, such as covering all exposed contacts with an oxide layer to reduce electrolyte gate leakage.[19] Due to these stated difficulties, and the fact that the ionic liquid is not solid state, we chose to use another type of electrolyte called solid polymer electrolytes (SPE).

Polymers are ubiquitous in modern society. From polytetraflouroethylene (PTFE, commonly known as Teflon) on non-stick pans, to polyethylene terephthalate (PET) used in clear plastic bottles, everyday life is full of polymers. Their molecular structure consists of long chains of covalently bonded repeat units, called monomers. The long chains entangle with each other, giving rise to the physical properties of polymers that are familiar to us, such as mechanical flexibility. Though polymers have a variety of interesting properties and applications, this work will focus on the polymer properties as they pertain to electrolyte gating using SPEs.

As mentioned above, one advantage of SPEs over ionic liquids is that they are solid at room temperature and therefore stay in place following deposition. A SPE can be deposited into a film by dissolving polymer and salt in a solvent, and then drop-casting or spin-coating the solution onto the substrate. After the solvent evaporates, a solid film is left behind that conformally coats the surface.[20] The film thickness can be controlled by varying the solution concentration, or by changing the spin-speed. Because the SPE forms a the solid, conformal, pinhole-free film, a metal topgate can be deposited onto the surface of SPEs using a shadow mask; in Chapter 2, we demonstrate, for the first time, a photolithographically defined metal topgate. The polymer that is typically used in SPEs is polyethylene oxide (PEO) which has a low electrical conductivity, and thus, low leakage current (< 10 pA/μm^2) when implemented as an electrolyte gate.[21] As with ionic liquids, SPEs are hygroscopic; however water (which can cause higher leakage current) can be driven out by annealing the film.[22]

There are several key characteristics when considering polymers as candidates for SPEs. The first is ion solubility. To avoid forming a two phase system of the polymer in one phase and the salt in another, the ions must be soluble in the polymer. The second is ion mobility in the polymer. In certain phases, and in certain temperature ranges, portions of the individual polymer chains, called segments, are mobile, allowing for the polymers to "slide" around one another. This mobility also permits dissolved ions to move within the polymer in response to an applied field, thereby permitting EDL formation.

The extent to which the ions can move within the polymer is a function of the crystalline structure of the polymer.[23] The phase diagram of polymer electrolytes are traditionally more complex than a simple solid/liquid phase. Depending on the temperature, molecular weight, and salt content of the electrolyte, different structures can form within the same electrolyte. For example, a common SPE, PEO:$LiClO_4$, can form several different phases as shown by the phase diagram in Figure 1.3.[1]

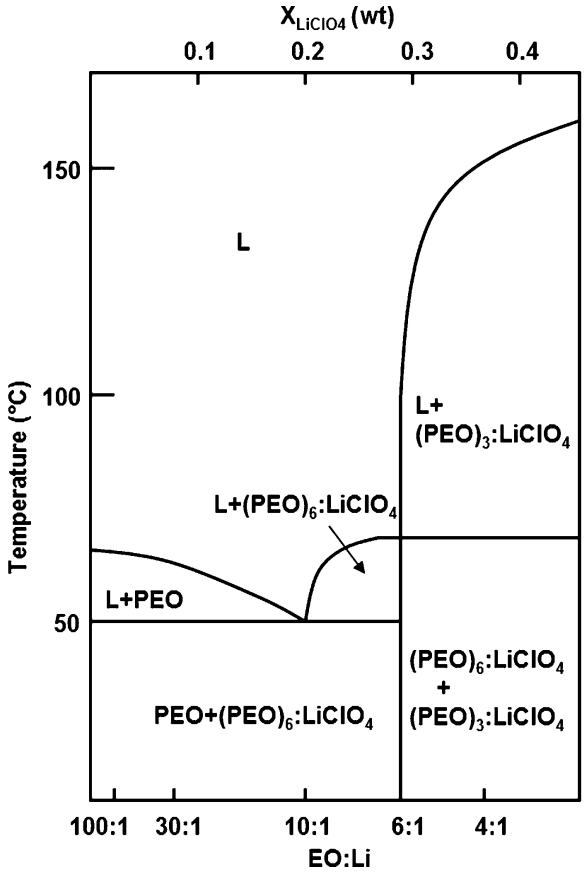

Figure 1.3. Phase diagram of PEO:$LiClO_4$ with varying ether oxygen:$LiClO_4$ concentrations. Reproduced from Robitaille *et al.*.[1]

One crystalline phase is pure crystalline PEO (labeled PEO in Figure 1.3), where the PEO forms a densely packed crystal that has low segmental mobility and is devoid of ions.[24] The ions are pushed out of the crystalline regions into nearby amorphous regions. High fractions of pure crystalline PEO tend to form at lower temperatures and at lower salt concentrations (the bottom left of Figure 1.3). Due to the lack of ions in the crystalline phase, and the lack of ion mobility in the nearby amorphous phase, pure crystalline PEO is not desired when ion transport is required of the electrolyte.

Another phase is made up of three PEO monomers coordinated to one Li^+ ion, referred to as $(PEO)_3$:$LiClO_4$ in Figure 1.3. In this phase, the PEO forms a channel-like structure that is so concentrated with Li^+ that there is no free space for the Li^+ to move into (*i.e.*, no vacant sites for the ions to hop to), prohibiting ion mobility through this phase.[25] This phase tends to form at high salt concentrations (the right side of the phase diagram).

On the other hand, the third crystalline structure, $(PEO)_6$:$LiClO_4$, has 6 PEO monomers coordinated to each Li^+ ion. Although $(PEO)_6$:$LiClO_4$ has similar channel-like structures to $(PEO)_3$:$LiClO_4$, the three additional monomer units provide vacancies for the ions to move to, meaning that the ions are mobile in this phase.[26] $(PEO)_6$:$LiClO_4$ tends to form at lower temperatures (the bottom of the phase diagram) and at all salt concentrations, indicating that this phase will more readily melt than the $(PEO)_3$:$LiClO_4$ and pure PEO phases.

The final phase on the diagram shown in Figure 1.3 is the liquid phase (L). This phase is fully amorphous, meaning there is no long-range crystalline structure; instead the chains are randomly entangled with one another. Because there is no crystalline structure holding the segments into place, the segmental motion of the polymer is high within the amorphous phase, which in turn means that the mobility of the dissolved ions is also high. This amorphous phase is found at higher temperatures in the phase diagram, because the crystalline phase melts into the liquid phase at these temperatures. As the phase diagram shows, the amorphous liquid phase can coexist with the other crystalline phases discussed in this work. For polymer electrolytes that have crystalline structures that do not allow ionic mobility, having a higher fraction of amorphous phase can lead to higher ion mobility in a SPE film. This can be accomplished by increasing the temperature of the electrolyte above the melting temperature of the crystalline phase.

For the SPEs in this work, there are two important temperatures. The first tem-

perature is the melting temperature, T_m, which can be identified on the phase diagram as a boundary defining the interface between the liquid and crystalline phases. As can be seen from Figure 1.3, T_m depends strongly on the salt concentration in the SPE, varying from 50 ^{o}C for 10:1 EO:Li ratio to over 150 ^{o}C for ratios above 4:1. While distinct phases may melt at different temperatures (*e.g*, at 4:1 EO:Li ratio in Figure 1.3, the $(PEO)_6$:$LiClO_4$ melts to the liquid phase at 60 ^{o}C, while the $(PEO)_3$:$LiClO_4$ doesn't melt until 150 ^{o}C), the T_m is defined as when the entire SPE is in the liquid phase. A polymer film is typically annealed at T > T_m because all previously formed crystalline structures are eliminated at these temperature, effectively "erasing" the thermal history of the material.

Another important temperature for polymer electrolytes is the glass transition temperature (T_g). Below T_g, the polymer's segmental mobility decreases to nearly zero.[27] This means that the ions in a polymer electrolyte below T_g are, in effect, immobilized, because ionic motion requires the individual polymer segments to be mobile. Above the T_g, the nonzero segmental mobility of the polymer allows for mobile ions in the electrolyte. This property allows ionic mobility within an SPE to be essentially "switched" on and off by changing the temperature of the electrolyte. Because the T_g does not involve a phase change (*i.e.*, it is only related to mobility of the amorphous polymer), this transition cannot be included on the phase diagram. However, the T_g can be directly measured using a calorimeter (for further information on calorimetry, see Appendix A).[26]

In Chapters 3 and 4 of this work, we choose PEO:$LiClO_4$ as the SPE for electrolyte gating. This SPE has been investigated as an electrolyte for polymer-based batteries, as well as used for electrolyte gated FETs.[13, 28] This electrolyte is attractive for our purposes because it is solid state, has mobile ions at room temperature, and the ion mobility can be well controlled by heating or cooling the electrolyte. Because the T_g of PEO:$LiClO_4$ is below room temperature (approximately -20 ^{o}C[29]), ions

are sufficiently mobile at room temperature to establish an EDL. Therefore, if the bias is not applied continuously, the EDL will dissipate, and the gating effect will be lost. Herein, we will refer to electrolyte gating as the process of using a gate to dynamically control the movement of the ions, whereas electrolyte doping will be will be used to refer to the condition where ions are stabilized on a surface in the absence of a gate bias. Several studies have accomplished electrolyte doping by establishing an EDL at T $> T_g$, cooling the device to T $< T_g$ thereby arresting the segmental mobility and therefore the ion mobility. This approach"locks" the ions into place, even when the gate bias is removed, as we show in Chapter 2.[21, 13]

1.4 Ferroelectrics

Thus far, only electrolytes have been discussed for using sheet charges to gate or dope materials. Another method of forming a sheet charge is through the polarization from a ferroelectric (FE). Ferroelectricity is a bulk property of some crystalline materials wherein the crystal has a spontaneous electrical polarization which can be switched by application of an electric field opposing the polarization.[30] The spontaneous polarization is typically provided by the unit cell of a crystal having a dipole moment due to asymmetry, with the asymmetry being reversed under an applied field. One well-studied example of this is $PbZrTiO_3$ (PZT). In PZT, the Ti within the crystal is bistable, either being above or below the center of the unit cell, as shown in Figure 1.4.[31] This bistability manifests as the dipole moment of the unit cell pointing either up or down, with an applied field switching the position of the Ti or Zr atom. This minimum field required to switch the dipole moment is called the coercive field ($\mathcal{E}_c$). When switching a FE crystal, the crystal switches polarization in groups called domains. The size of these domains are controlled by factors such as growth temperature, stoichiometry, and the FE film thickness (thicker films typically having larger domains).[32]

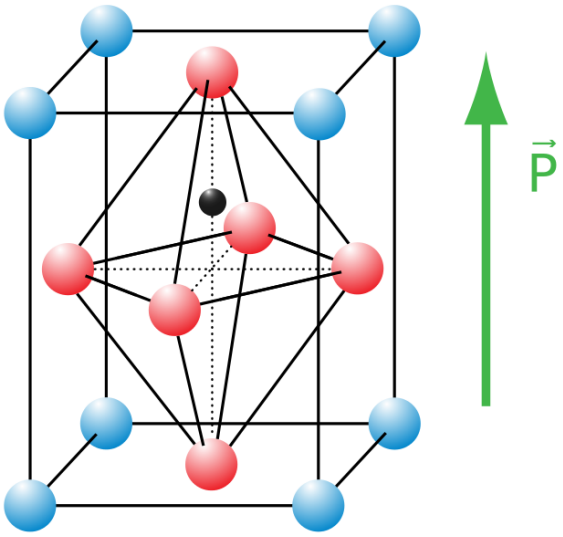

Figure 1.4. Ball and stick representation of PZT with the Pb (blue) and O (red) serving as the immobile lattice, while the Ti/Zr (black) atom is bistable either above or below the center of the unit cell, depending on the remnant polarization. Image by Wikimedia user Pinin, distributed as a work in the public domain, 5/18/2017.[2]

A FE capacitor consists of a FE clad by two metal electrodes. As the capacitor is charged such that the field within the dielectric is opposing the remnant polarization (*i.e.* the polarization induced by the dipole in the unit cell) of the FE, the FE will switch when the field exceeds the coercive field. One way that this is measured is with a current vs voltage (I-V) plot generated by sweeping the voltage beyond the coercive voltage (*i.e.*, the voltage at which the FE switches, V_c) in both the positive and negative direction, to the capacitor and measuring the current (Figure 1.5). The capacitive contribution to the current is seen as a constant current with the magnitude related to the capacitance and the sweep rate of the triangle wave, while the FE switching portion is two peaks in current, one at each switching event, positive $(+P)$ to negative $(-P)$ polarization and negative $(-P)$ to positive $(+P)$

polarization. The current peaks result from the polarization of the FE switching direction, which in effect changes the interface charge on each FE/metal contact interface to the opposite charge.

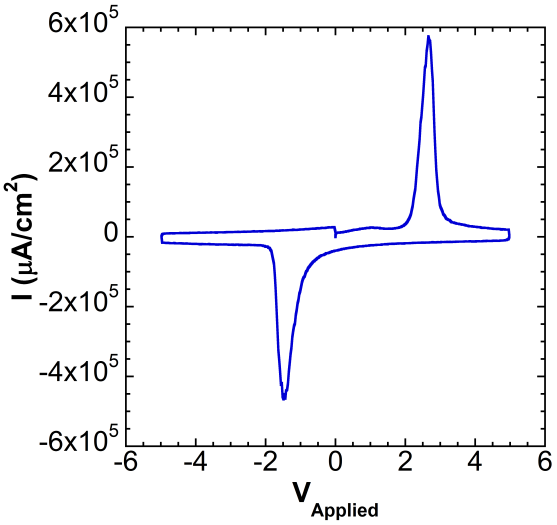

Figure 1.5. I-V of a PZT FE capacitor resulting from a 5 V triangle wave with a 3000 V/s sweep rate, showing the switching current visible at approximately ±2 V. Note, at the first measurement point there has been no prior change in voltage, so that all current contributions at this point are zero, making the first data point 0 A at 0 V. Measurements by C. Alessandri and E. Kinder.

By subtracting the capacitive portion from the I-V data, the switching current is obtained, which when integrated yields the FE polarization. The hysteresis shown in the polarization vs applied field (P-E) plot (Figure 1.6) demonstrates that the FE does not switch until the applied bias is near $\mathcal{E}_c$ (approximately ±2 V on Figure 1.6).

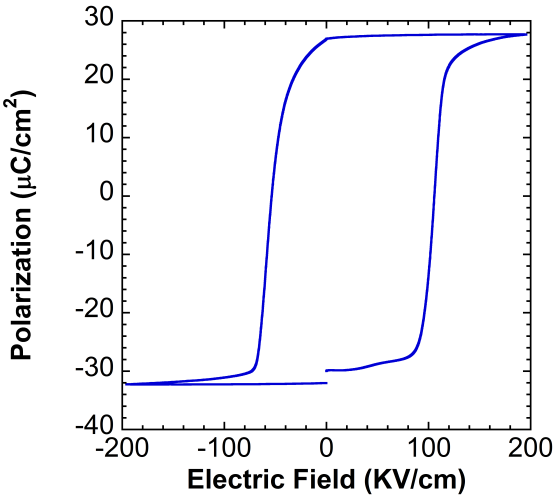

Figure 1.6. P-E calculated from integrating the switching current of the PZT capacitor, showing the hysteresis of the polarization. Measurements by C. Alessandri and E. Kinder.

It is this hysteresis that allows for FE capacitors to be used in memory, specifically FE random access memory (FeRAM).[33] Typical FeRAM is integrated in a one transistor, one capacitor setup, where the capacitor is a FE capacitor, where the state of the polarization stores 1 bit of data.[34] In order to read the memory element, a voltage sufficient to switch the polarization FE capacitor is applied, and the current measured. If the remnant polarization is in the opposite direction as the applied field, the switching current is detected, however if the remnant polarization and applied field are in the same direction, no switching occurs, and therefore no switching current is detected. Because the voltage applied during the read step is enough to switch the FE, reading the memory element is a destructive read, which requires re-writing data to the memory element.

A FeFET is a MOSFET with a gate dielectric that has FE properties.[35] This turns the gate capacitor into a FE capacitor, with the state of the FE serving to shift

the threshold of the FET. By operating the FE as a 2-state system, the threshold voltage of the FET has two values, depending on the remnant polarization of the FE. However, it has been shown that FEs can be partially switched, where the remnant polarization takes a value between $+P$ and $-P$.[36, 37] This allows for the threshold shift of a FeFET to take on more than 2 values, allowing for applications such as multibit storage in a single transistor or using a FeFET as a circuit-level implementation of machine learning, which is the focus of Chapter 5 of this work.[38]

In order to partially switch a FE, fast voltage pulses ($\sim$1 μs) are used.[39, 37] By applying voltage pulses across the FE that are short enough that some of the domains switch while others remain unswitched, the remnant polarization can be modulated to take on values between $+P$ and $-P$. The varying hysteresis loop results from shorter pulse widths switching fewer states than longer pulse widths, meaning that the polarization is a function of pulse width, as can be seen in Figure 1.7 where the size of the hysteresis loop indicates the polarization of the FE. The resolution of the partial polarization is determined by the domain size, which then determines the minimum charge switched per domain flip. For partial switching applications, FEs with smaller domains are preferred, which can be achieved by reducing the FE thickness.[40] This means that for partially switching FeFETs, where the channel in effect senses the polarization state of the FE, the thinner the FE gate dielectric, the higher the resolution of polarization.

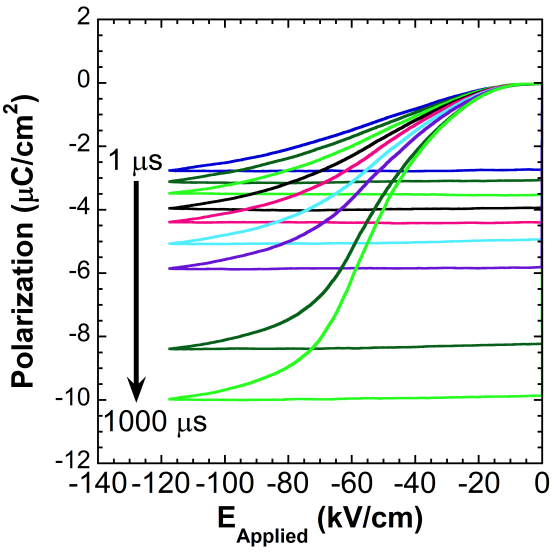

Figure 1.7. Polarization vs E curve of a PZT capacitor switched using 3 V pulses varying in width from 1 to 1000 μs. Measurements by C. Alessandri and E. Kinder

1.5 Two-Dimensional Materials

Since the isolation of graphene in the mid 2000's, two-dimensional (2D) electronics has been an active area of research. 2D electronics typically have a channel composed of few or single layer van der Waals crystals.[41] These crystals, such as graphene and transition metal dichalcogenides (TMDs), are layered materials held together by Van de Waals forces. Electronics fabricated with these 2D materials have a number of interesting characteristics, such as an ultra-thin channel which confines transport to one molecular layer, record high mobilities, and the ability to form heterojunctions through crystal stacking.[42, 43]

The first 2D material to be investigated by physicists and material scientists is graphene, the monolayer form of graphite. Graphene is an allotrope of carbon, consisting of a single planar hexagonal lattice of sp^2 bonded carbon (Figure 1.8). Mono-

layer graphene is a semi-metal (a zero-bandgap material), however bilayer graphene has shown a band gap that is dependent on the electric field normal to the graphene surface.[44] Monolayer and few layer graphene nanoribons have also been shown to have a band gap that depends nanoribbon size and crystal orientation.[45]

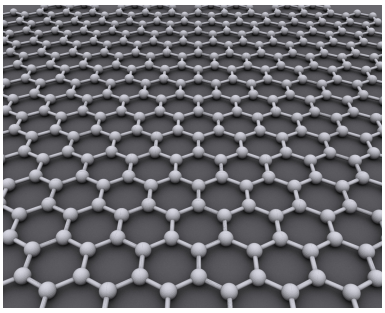

Figure 1.8. Ball and stick representation of graphene showing carbon atoms (spheres) connected by sp^2 bonds (rods). Image distributed under CC-BY-SA License, 5/18/2017.[3]

Graphene is isolated by one of three methods. The first is the so-called "Scotch tape method", which involves taking a graphite crystal and using tape to repeatedly cleave the graphite crystal until just a few layers remain.[46] The tape is then pressed onto the substrate (typically a SiO_2 wafer) and peeled off, cleaving the crystals one final time, leaving behind few and monolayer graphene sheets adhered to the substrate. The graphene isolated in this fashion is typically the most defect-free with the fewest grain boundaries. Flake sizes resulting from this method are on the order of 400 μm^2.[47]

The second technique is chemical vapor deposition (CVD), whereby graphene is synthesized directly on a metal substrate, such as copper or nickel.[48, 49] Unlike me-

chanical exfoliation, this approach can provide 150 mm wafer-scale growth, opening up the possibility of using graphene in VLSI processes. After the graphene is grown, the metal layer can be etched away, releasing the graphene layer to be deposited onto a substrate.[50] This type of graphene tends to have a large number of defects due to the metal ions introduced during the transfer process,[51] as well as defects originating during crystal growth.[52] CVD graphene is known for small grain sizes (on the order of 0.0625 μm^2).

The third method is to grow graphene directly from SiC, creating multilayer (on the order of 5-10 layers, depending on growth conditions) graphene on the SiC surface.[53] This growth strategy produces n-type graphene due to the interaction of the graphene with the SiC substrate with few defects.[54] However the graphene fabricated using this method can become significantly thicker at SiC step edges - in excess of 20 layers.[53]

Transition metal dichalcogenides (TMD), the crystalline structure of which is shown in Figure 1.9, are layered 2D crystals similar to graphene. Unlike graphene, they are made up of two different elements in the MX_2 configuration, with M representing a transition metal and X representing a chalcogenide atom, such as S, Se or Te. This leads to the molecular layers being three atomic layers thick, instead of the single layer of graphene. The most heavily-researched TMDs are the semiconductors that do not readily oxidize in air, namely MoS_2, $MoSe_2$, $MoTe_2$, WS_2 and WSe_2. These TMDs have an indirect band gap in the bulk state, but as the layer thickness decreases, the band gap increases and the monolayer forms have a direct band gap.[55]

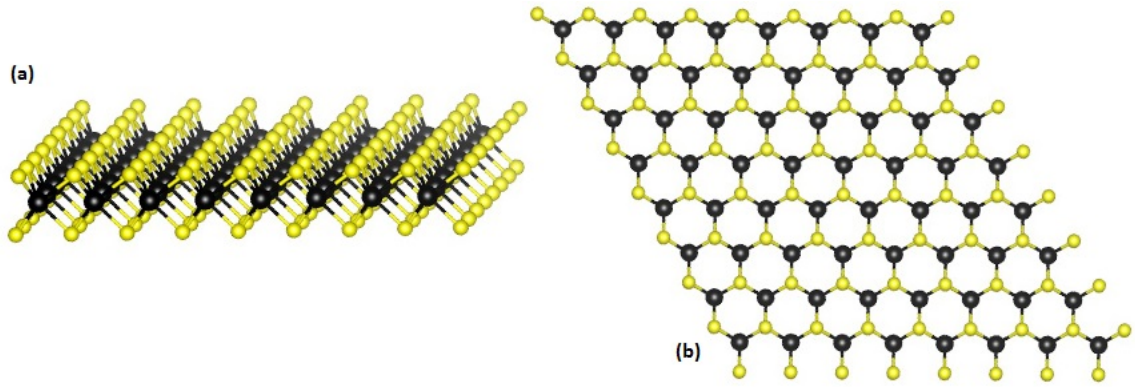

Figure 1.9. Isometric (a) and top-down (b) schematics of a TMD showing transition metals (black spheres) bonded to the chalcogenides (yellow spheres). Image distributed under CC-BY-SA 5/16/2017.[4]

Similar to graphene, mechanical exfoliation and CVD are the two most popular methods of producing TMDs for electronics. Mechanical exfoliation using the "Scotch tape method" typically yields few- or monolayer thick flakes. CVD grown material (most commonly on sapphire) is typically monolayer or bilayer, but has poor substrate coverage, often consisting of isolated triangles of TMD crystals.[56]

The 2D materials used in this dissertation are prepared by all three methods described above. In Chapter 2, devices are fabricated on epitaxially grown graphene, while in Chapter 3, exfoliated MoS_2 forms the channel material for the devices tested. For chapter 4, CVD grown graphene on Cu foil is used to create the FET channels, while epitaxially grown graphene is used as one type of backgate contact.

1.5.1 Doping of 2D Materials

While conventional doping strategies, such as substitutional doping are being investigated by other groups,[57, 58] doping using an electrolyte provides a method to investigate the electronic properties of 2D materials without developing a traditional

doping method. The thin planar nature of 2D materials that makes traditional doping strategies more difficult make them ideal for electrolyte gating. The possibility of a single monolayer body thickness allows for electrolyte gating of the entire thickness of the channel. This, along with the lack of chemical reactivity between commonly used electrolytes and 2D materials allows for large charge carrier densities (in excess of 10^{14} cm^{-2}[13]), which provides an easy way to dope 2D materials to explore their fundamental properties.

1.6 Overview of Dissertation

In this work, we investigate materials that produce sheet charges (SPEs and FEs) with an eye towards application to gating and doping 2D materials. In chapter 2, we explore the ability to tune the EDL retention time by changing the T_g of the electrolyte. Specifically, we replaced PEO with polyvinyl alcohol (PVA) in an electrolyte gated FET, increasing the T_g of the electrolyte by approximately 110 ^{o}C. This results in a device that can retain an EDL 10^6x longer at room temperature than the same device gated with a PEO-based electrolyte, while having a sheet carrier density in excess of 10^{14} cm^{-2} for holes and 10^{13} cm^{-2} for electrons. This room temperature, reconfigurable electrolyte doping strategy has applications in hardware based security, both information security, as well as obfuscation of proprietary components to prevent reverse engineering.

In Chapter 3, we explore the effect of high fields on electrolyte-gated MoS_2 FETs to characterize the signatures associated with ion intercalation and electrochemistry. We show that we are performing electrochemical reactions involving the MoS_2 channel not only by the change in transfer characteristics, but by the physical expansion of the height of the channel. For the thinner devices, this change in channel thickness led to device failure (to an open circuit). We observed that device longevity (*i.e.* the number of voltage cycles) increased with increasing channel thickness.

In Chapter 4 we demonstrate a method which allows for the transfer of a fully fabricated 2D crystal FET directly onto a PEO:$LiClO_4$ layer, allowing for an electrolyte backgate, the first demonstration of such a transfer. The motivation for this electrolyte backgate is the development of a low-power memory based on 2D crystals. Such development is motivated by the Center for Low Energy Systems Technology's (LEAST) goal of fabricating low energy transistors(< 60 mV/dec), for which a low-energy memory is required if computation is to be done using all low-energy technologies. Because of the materials properties of the organic electrolytes involved, the proposed device architecture represents a huge fabrication challenge which is addressed, in part, in this chapter.

Finally, in Chapter 5, we demonstrate partial switching of the remnant polarization of the FE, $HfZrO_2$ (HZO). By using a pulsed bias method that has previously been used on other FE systems, to switch the remnant polarization of HZO, we are able to modulate the sheet carrier density at the FE surface. The ability to change the polarization of HZO to values other than just $-P$ and $+P$ (the fully switched remnant polarizations) allows HZO to be operated as a multistate system rather than just a 2-state system, which is vital for analog memory and resistive processing. As well, a new model is proposed to predict the switching behavior of the FE based on a distribution of switching voltages. This work is the first steps toward a new 2-terminal resistive processing unit outlined in the chapter.

CHAPTER 2

STATIC DOPING OF 2D CRYSTALS *VIA* ROOM TEMPERATURE ION LOCKING OF ELECTROLYTES[1]

2.1 Motivation

It has been shown that by cooling a SPE to below its glass transition temperature (T_g), ionic motion in the electrolyte can be arrested, "locking" the ions in place, effectively doping the 2D channel with the EDL.[59, 60] This strategy of exploiting the temperature-dependent mobility of the polymer to dope the channel of a FET device has proven useful for exploring new regimes of transport in 2D materials; however, the electrolyte gates reported to date are primarily based on PEO with a T_g well below room temperature. The reason for choosing PEO up to this point is that research on polymer electrolytes has been almost exclusively driven by the battery community for which fast ion transport and therefore the lowest possible T_g is desired. The low T_g requires the device to be cooled below room temperature to lock the ions into place.[5, 13] For ion doping to be used in a practical device operating near room temperature, the ions would have to be drifted into place at a temperature greater than room temperature, then cooled to room temperature to fix the position of the ions. Specifically, by creating the EDL using a polymer electrolyte with $T_g > 23\ ^oC$,

[1]Related Publication: Erich Kinder; Ashley Fuller; Yu-Chuan Lin; Joshua Robinson; Susan Fullerton-Shirey "Increasing the room-temperature electric double layer retention time in two-dimensional crystal FETs", ACS Applied Materials and Interfaces, 2017, Vol. 9, Issue 29, pp 25006-25013.

Contributions: Kinder - electrolyte preparation, device fabrications, electrical measurements, FTIR, DSC; Fuller - DSC; Lin and Robinson - epitaxial graphene synthesis; Fullerton-Shirey - directing author

a static doping profile can be obtained at room temperature in the absence of a gate bias. In this way, devices can be programmed n- or p-type, or p-n junctions can be created at $T > T_g$, and the resulting doping profiles can be maintained at room temperature without the need for constant biasing. It is also conceivable that these programmed devices could be engineered to be deprogrammed by specific triggers, such as exposure to air, water or light, giving rise to new applications in hardware-based security. Such security could safeguard information by automatically erasing data stored in the EDL when tampered with, or when prompted to by the user. As well, with EDL-doped FETs working as programmable gates, the purpose of a circuit could be obfuscated, leading to hardware-level encryption of data as well as obfuscation of the circuit defending against reverse engineering of proprietary circuits.

In this study, we replace the commonly used polymer, polyethylene oxide (PEO), with polyvinyl alcohol (PVA). While the T_g of PEO electrolytes can vary depending on the type and amount of salt, the T_g typically ranges from -36 to -8.5 ^{o}C (for ether oxygen to Li ratios of 100:1 and 4:1, respectively).[26] In contrast, the T_g of pure PVA is approximately 85 ^{o}C.[61] While PEO and PVA are chemically similar, moving the oxygen from the main chain backbone in PEO to the side chain in PVA increases T_g by over 100 ^{o}C. In this work, we demonstrate that EDLs created using PVA:$LiClO_4$ at 100 ^{o}C can be locked into place at room temperature while maintaining high sheet carrier densities ($n_s \approx 10^{14}$ cm^{-2}) for 160 minutes. This is a six order of magnitude improvement in EDL retention time over PEO:$LiClO_4$ at room temperature.[5] In addition to the increase in room temperature EDL retention time, we also demonstrate, for the first time, the deposition of a photolithographically defined metal top gate deposited directly onto the electrolyte surface.

2.2 Experimental Details

2.2.1 Electrolyte Preparation and Characterization

Electrolytes were prepared by dissolving polyvinyl alcohol (PVA, Mw = 100,000 g/mol, Polymer Standards Service) and lithium perchlorate ($LiClO_4$, Sigma Aldrich, 99.9%) in 80 ^{o}C deionized water to form 1.0 wt% solutions with vinyl alcohol to Li ratios of 8:1, 10:1, 20:1 and 100:1.

Samples for differential scanning calorimetry (DSC) measurements were prepared under ambient conditions by depositing a portion of the PVA:$LiClO_4$:water solution in a teflon beaker and heating it to 105 ^{o}C to evaporate the solvent (see Appendix A for more information on DSC). 8 - 10 mg of the resulting film was placed in a 40 μL aluminum DSC pan (Perkin Elmer), heated to 200 ^{o}C to soften the film, and pressed to create a hermetic seal. DSC measurements were taken using a Mettler-Toledo DSC1, calibrated with an indium standard. Samples were measured in the temperature range of 25-225 ^{o}C at a heating rate of 10 ^{o}C/min and cooling rate of 5 ^{o}C/min. Heat/cool/heat scans were acquired, where the first heating scan removed the thermal history of the samples.

Samples for FTIR analysis were prepared by dropcasting approximately 1 mL of the electrolyte solution onto a glass slide (for more information on FTIR, see Appendix A). The samples were then left in ambient until all the solvent had evaporated, leaving an electrolyte film on the glass slide. Two of the samples were then heated to 100 ^{o}C for 40 and 180 minutes, respectively. FTIR spectra were then acquired using the ATR module of a Jasco FT/IR-6300.

2.2.2 Device Fabrication

Devices were fabricated using a bilayer resist and the lithography processing details are outlined in Appendix B. Devices were fabricated on both CVD-grown

graphene deposited on a Si/SiO_2 substrate (Supermarket Graphene, 10 nm SiO_2), and epitaxially grown graphene on SiC.[53] CVD graphene on Si/SiO_2 was used for devices in which both top and back gates were required, while epitaxial graphene on SiC was used where possible due to the high quality and wide area of the material. Despite its low on/off ratio, graphene was used in this study to test the electrolyte because of the availability of wide-area and high-quality graphene.

A Bruker Dimension Icon Atomic Force Microscope (AFM) in ScanAsyst mode was used to characterize surface residue after photolithography. ScanAsyst Air tips were used, which have a Si cantilever and a SiN lever (for more information see Appendix A).

The electrolyte with a vinyl alcohol to lithium ratio of 20:1 was chosen as the electrolyte gate for the devices in this study. $(PVA)_{20}$:$LiClO_4$ was deposited on the devices by dropcasting approximately 0.5 mL of 1 wt% solution on a 1 x 1 cm sample, and the solvent evaporated under ambient conditions. The sample was heated on an 80 ^{o}C hot plate for 3 minutes to drive off remaining solvent, leaving a film approximately 1 μm thick, as measured by AFM. Metal top gates were deposited directly onto the electrolyte using the same process to deposit source/drain contacts (described in Appendix B). A 150 nm Au top contact was evaporated onto the electrolyte and lift-off was performed using acetone and isopropanol.

2.2.3 Device Measurements

Electrical measurements were acquired in a dark, nitrogen filled Cascade Summit 11861 probe station, using an Agilent B1500a Semiconductor Parameter Analyzer. The temperature of the device was controlled by a Temptronic TP03000 temperature controller to within +/- 0.1 ^{o}C. To record temperature-dependent transfer characteristics, the samples were held for 10 minutes at each target temperature to allow the device to reach thermal equilibrium before the measurement.

To establish an electrostatic double layer (EDL) at the interface between the electrolyte and the channel (*i.e.*, to program the device), the sample was first heated to the programming temperature (T_{Pr}) of 100 ^{o}C. Because T_{Pr} is higher than the glass transition temperature of the electrolyte (T_g), the ions are mobile and the EDL can be established. While holding the temperature at T_{Pr}, the programming bias (V_{Pr}) was applied to the top gate for 10 minutes (V_{DS} = 100 mV), driving ions to the surface of the channel and establishing the EDL. The device was then cooled (with V_{Pr} still applied) to 23 ^{o}C at a cooling rate of 0.7 ^{o}C/s. Because the T_g of the electrolyte is higher than than room temperature, the polymer mobility and therefore ion mobility is reduced and the device is considered to be programmed. With the EDL "locked" into place at room temperature, the gate bias can be removed while maintaining a static doping density.

Retention time, defined as the time at which a programmed EDL begins to dissipate, was measured using devices fabricated on a graphene/SiC substrate. First, the device was heated to 100 ^{o}C and top gate transfer characteristics were taken to locate the Dirac point and record the bias-dependent current values. Next, the device was programmed to V_{Pr} = +2 V while monitoring the drain current (V_{DS} = 100 mV). At time = 0 s, the top gate was grounded, and the I_D measurements continued for 36 hours. In one case, V_{DS} = 100 mV was continuously applied, and in another case, V_{DS} = 100 mV was pulsed for 10 ms every 10 s. The decay of I_D quantifies the dissipation of the EDL over time.

Sheet carrier density measurements were made on a top-gated van der Pauw device with V_{Pr} = -2, +2 V. Devices were fabricated on a 1 x 1 cm piece of epitaxially grown graphene on SiC. Contacts (5 nm Ti/145 nm Au) were deposited on the corners *via* a shadow mask. The electrolyte was deposited using the same method as described above, and a metal top gate (5 nm Ti/145 nm Au) was deposited directly on the electrolyte using a shadow mask. A Nanometrics HL5500PC Hall Effect

measurement system was used to quantify the sheet carrier density *via* the van der Pauw method.[62]

After the programming procedure was completed and the sample was cooled to room temperature, five consecutive measurements were taken within 10 minutes (this was done two separate times for the +2 V case, and once for the -2 V case). Error was calculated as one standard deviation from the mean of these measurements. The main contribution to the error arises from variations in the contacts between the probes and the device contact pads.

2.3 Results and Discussion

To program the device *n*- or *p*-type, the programming temperature, T_{Pr}, must be larger than the glass transition temperature (T_g) of the PVA electrolyte. This ensures that the ions have sufficient mobility to respond to the applied field and establish an EDL. The T_g is measured directly using DSC to set the lower bound for the T_{Pr}. DSC data from the second heating segment of a heat/cool/heat cycle are shown in Figure 2.1 for pure PVA along with four electrolytes with varying $LiClO_4$ concentrations, with the transitions corresponding to T_g highlighted by arrows. The T_g of pure PVA is 80 ^{o}C, which agrees with a previous report.[63] Although the $LiClO_4$ concentration varies over a large range (*i.e.*, vinyl alcohol to lithium ratios from 100:1 to 8:1), all of the corresponding T_g values remain within 4 ^{o}C of pure PVA, indicating that the mobility of PVA is not significantly affected by $LiClO_4$. This contrasts PEO-based electrolytes for which the T_g increases from -55 ^{o}C for pure PEO to -8.5 ^{o}C with an ether oxygen to lithium ratio of 4:1.[26]

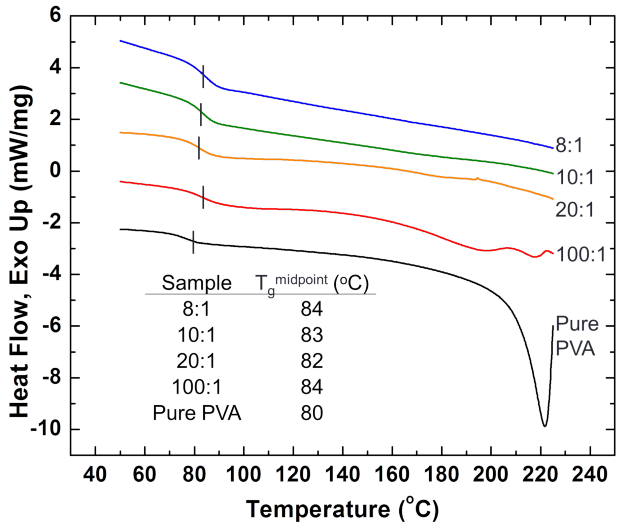

Figure 2.1. Second heating segments of DSC heat/cool/heat scans for pure PVA and PVA with varying vinyl alcohol to lithium ratios. The midpoints of the glass transitions are indicated with vertical lines on the plot, and the corresponding values are listed in the table. The heating rate is 10 ^{o}C/min. Data are offset on the y-axis for clarity.

The endothermic feature present in the majority of samples shown in Figure 2.1 at T $>$ 230 ^{o}C corresponds to the decomposition temperature (T_d) of the PVA.[64] Therefore, T_g and T_d set the lower and upper bounds for T_{Pr} to between 80 and 225 ^{o}C, respectively. T_{Pr} must be sufficiently higher than T_g to establish the EDL, but not too high to thermally degrade the electrolyte. Therefore, 100 ^{o}C is chosen as the initial T_{Pr}, meaning that the operating temperature, 23 ^{o}C, will be more than 50 ^{o}C below T_g. Similar studies using PEO-based electrolytes for "locking" the EDL show that a lock-in temperature that is 20 ^{o}C below T_g is sufficient to create a static EDL in the absence of a gate bias.[60, 59]

The melting point of pure PVA appears as a well-defined endothermic peak in Figure 2.1 at T = 225 ^{o}C, with a crystal fraction of 0.28. However, the samples

containing $LiClO_4$ either show no melting feature, or a weak melting feature in the case of a low salt concentration of 100:1. This result indicates that $LiClO_4$ slows the recrystallization kinetics of PVA to the extent that it does not recrystallize on the timescale of the DSC measurement - similar to what has been shown before for PEO:$LiClO_4$.[65] The recrystallization kinetics are measured and discussed in Appendix B. Based on these data, the 20:1 concentration is chosen for this study.

When polymer electrolytes are used to explore transport in 2D materials, the deposition of the electrolyte is typically the last processing step and the device is gated by touching the electrolyte surface near the device with the gate probe. This approach can lead to significant differences between measurements on the same device because the probe tip is not anchored onto a contact pad, meaning that the probe shifting over time can change the contact area and physically move the electrolyte in such a way that induces noise in a measurement. Another method is to use a side gate; however, the primary drawback is a longer EDL formation time compared to a top gate because the side gate is often located several microns or tens of microns away from the channel, while a top gate can be located at a distance less than one micron above the channel, providing less resistance and faster ion response. Most polymer-based electrolytes cannot be lithographically processed because they are soluble in the solvents and developers traditionally used in photolithography (*e.g.,* acetone, water, isopropyl, and TMAH-based developers), and as such, a patterned top gate cannot be deposited. PVA:$LiClO_4$, however, is insoluble in these solvents at room temperature. This insolubility permits photolithography and lift-off to be completed directly on the surface of the PVA:$LiClO_4$, thereby enabling a patterned metal top gate to be deposited directly on the electrolyte. Although not demonstrated in this work, an oxygen plasma etch could be utilized to pattern the electrolyte (*i.e.*, the electrolyte not protected by the metal top gate could be removed). Figure 2.2a is a 3D schematic of the FET device fabricated in this study, which includes the patterned

metal top gate (cross-section shown in Figure 2.2b). Figure 2.2c is an optical image of a fabricated device on CVD graphene, where the top gate is located on the surface of the electrolyte and the source and drain contact pads are visible underneath the optically transparent electrolyte.

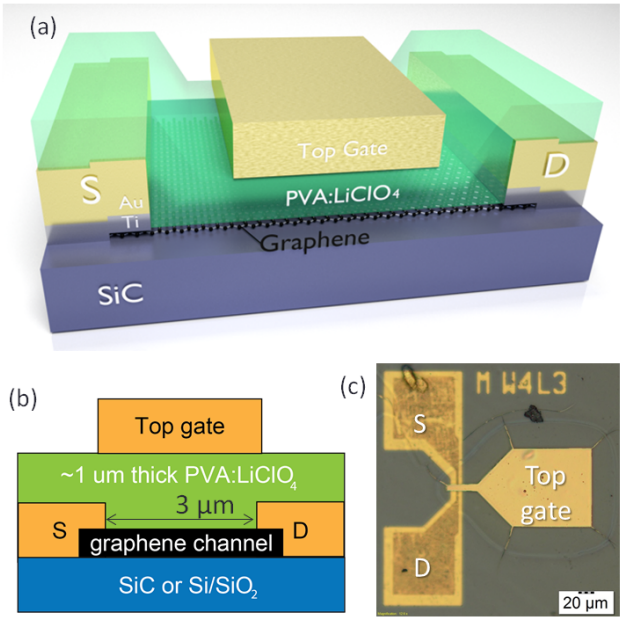

Figure 2.2. (a) 3D Schematic and (b) cross-section of the electrolyte-graphene FET fabricated for this work and (c) an optical image of a fabricated device using CVD graphene on Si/SiO_2 with a patterned metal top gate deposited on the electrolyte, with the source/drain contacts visible beneath the transparent electrolyte.

The goal of the first I-V measurements was to confirm that the ions in the electrolyte are immobile at room temperature, and mobile at T_{Pr}. Temperature-dependent transfer characteristics, shown in Figure 2.3, were taken on a device fabricated on transferred CVD graphene on Si/SiO_2 that has not been previously

programmed. For measurements at T = 25^o C (55 ^{o}C below T_g), the ions in the electrolyte are immobile, meaning that the electrolyte is simply acting as a thick ($\sim$1 μm) dielectric. As the device temperature increased and approaches T_g, the polymer mobility begins to increase thereby increasing ion mobility. An EDL forms at the electrolyte/channel interface in response to the applied bias, thereby improving gate control detected as an increase in the drain current with increasing temperature. This is seen in Figure 2.3 as an increase in current modulation of a CVD graphene FET gated with $(PVA)_{20}$:$LiClO_4$. At V_{TG} = 5 V, the current increases by 0.01, 0.07 and 0.11 μA for 50, 75 and 100 ^{o}C, respectively. Because graphene has no bandgap and is semi-metallic, the off current is high ($\approx$ 0.25 μA) and the on/off ratio is less than 2 μA at T = 100 ^{o}C.

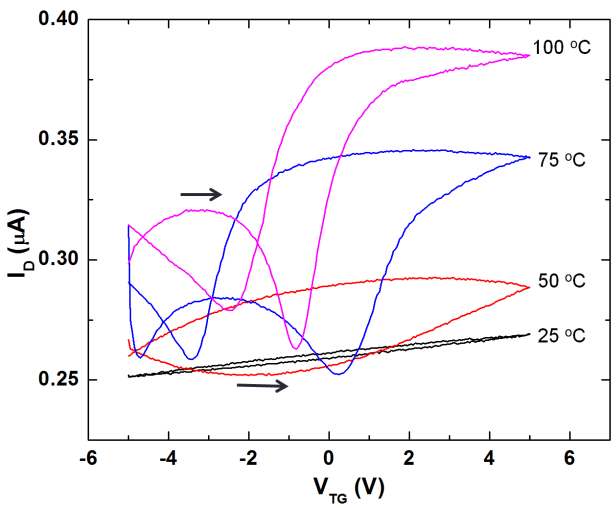

Figure 2.3. Transfer characteristics of a CVD graphene FET gated using a SPE consisting of $(PVA)_{20}$:$LiClO_4$ showing an increase in gate control and hysteresis with increasing temperature. V_{DS} = 0.1 V, sweep rate = 0.5 V/s, 10 minutes between sweeps. Gate leakage is below 10 pA for all points in this measurement.

Along with increased gate control, hysteresis increases with temperature as the ions become more mobile (Figure 2.3). The hysteresis originates from the low polymer mobility at $T < T_g$ and therefore a sluggish response of the ions to the changing gate bias. As the gate bias is swept at 0.5 V/s, the slow ion motion leads to a lag between the applied field and the ion response resulting in two Dirac points: one for the forward sweep direction and a second for the reverse sweep. As the temperature further increases above T_g the hysteresis loop begins to close, and the separation between the two Dirac points decreases. If the ionic mobility were increased, or the top gate sweep rate were reduced to the point where the ions could respond to the field in the sampling time of the instrument, then the hysteresis would be reduced or eliminated.[59]

To measure the sheet carrier density induced by the electrolyte and the mobility of the channel, Hall measurements are made using a gated van der Pauw device. To measure the electron and hole carrier density, the device is programmed using $V_{Pr} = \pm$ 2 V. The sheet carrier densities, tabulated in Table 2.1 (with error equal to one standard deviation and data provided in Appendix B, Table B.1), exceed 10^{13} cm^{-2} for electrons and 10^{14} cm^{-2} for holes, which is comparable to carrier densities reported for similar electrolytes.[13, 66] The electron and hole mobilities are also consistent with previous reports for graphene FETs gated with PEO at the same $LiClO_4$ concentration as this study.[5] As expected, the mobility values are low because mobility decreases with increasing n_s due to carrier scattering.[67, 53]

After confirming that the sheet carrier densities are large for both electrons and holes, we directly measured the time that the EDL can be retained in a programmed state - defined as the EDL retention time. A $(PVA)_{20}$:$LiClO_4$-gated FET, fabricated on epitaxially grown graphene on SiC, is programmed to $V_{Pr} = +2$ V at T = 100 ^{o}C for 10 minutes. This long programming time was not optimized for this system -

TABLE 2.1

SHEET CARRIER DENSITY AND MOBILITY ACQUIRED *VIA* HALL MEASUREMENT OF VAN DER PAUW STRUCTURE ON EPITAXIAL GRAPHENE ON SIC

V_{Pr} (V)	Sheet carrier density (cm^{-2})	Mobility ($cm^2V^{-1}s^{-1}$)
+2	-6.3 ± 0.03 x 10^{13}	443 ± 12
−2	1.6 ± 0.3 x 10^{14}	41 ± 4.2

it was simply chosen as a starting point to provide time for the EDL to equilibrate to the maximum drain current, corresponding to the fully established EDL. Under a gate positive bias, an EDL is formed between the Li^+ ions near the channel and the electrons induced in the channel, resulting in n-type doping of the channel. The device is then cooled to room temperature under bias to lock the EDL in place. Following the programming and cooling steps, the top gate is grounded and I_D is monitored as a function of time, shown in Figure 2.4, superimposed on the transfer characteristics of the device taken previously at T = 100 ^{o}C. The drain current remains constant for the first 1000 seconds, indicating that the full EDL has been retained during this time in the absence of an applied bias.

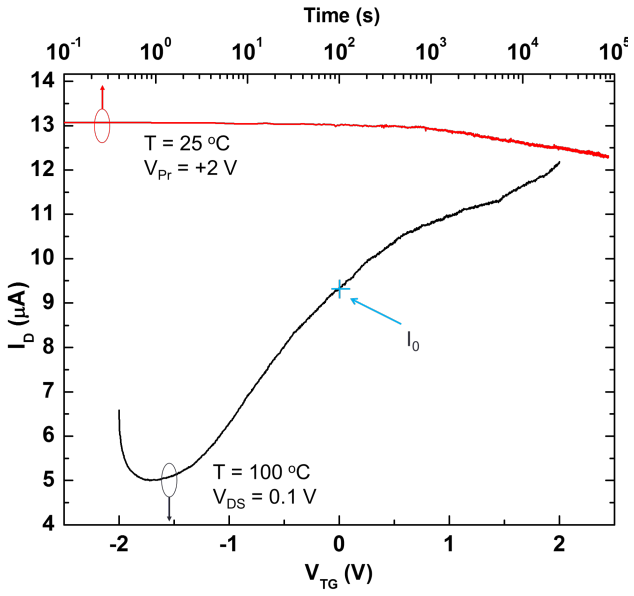

Figure 2.4. Top gate transfer characteristics of a epitaxial graphene FET on SiC with $(PVA)_{20}$:$LiClO_4$ at T = 100 ^{o}C (black trace, bottom axis, 0.5 V/s sweep rate); I_0 is the current at V_{TG} = 0 V which is used in equation (1), identified on the plot with a blue cross. Room temperature I_D vs time data (red trace, top axis) for the same device following programming (V_{Pr} = +2 V) is also shown, with t = 0 s defined as the time at which the top gate is grounded. V_{DS} = 0.1 V for both cases. Gate leakage is less than 20 pA for all points in this measurement.

To quantify the fraction of the EDL that is maintained over time, the $I_D(t)$ data are normalized by the current of the fully dissipated EDL using Equation 2.1. The EDL will be fully dissipated at V_{TG} = 0 V and 100 ^{o}C, and therefore the drain current at this voltage, I_0, is first subtracted from the time-dependent $I_D(t)$ data. Next, each data point is divided by the difference in the current between the fully established EDL and the fully dissipated EDL (*i.e.*, $I_D(t = 0) - I_0$). Thus, a value of $I_D^{Norm}(t)$

equal to 1 corresponds to the maximum EDL and 0 corresponds to no EDL.

$$I_D^{Norm}(t) = \frac{I_D(t) - I_0}{I_D(t=0) - I_0} \tag{2.1}$$

The normalized data for $(PVA)_{20}$:$LiClO_4$ are plotted in Figure 2.5 along with normalized data for $(PEO)_{20}$:$LiClO_4$ measured and analyzed in the same way on epitaxially grown graphene FETs.[5] Notice that two types of measurements were made on the PVA devices: the first with a constant $V_{DS} = 100$ mV applied, and the second with 10 ms pulses of $V_{DS} = 100$ mV applied every 10 seconds. The rationale for the pulsed measurements is to verify that Joule heating is not responsible for the dissipation of the EDL. If Joule heating were causing the dissipation, then the continuous measurement, which has 1000x larger power dissipated than the pulsed case, would have a shorter EDL retention time. The results are the same for the continuous and the pulsed measurements and they show that ∼75% of the EDL is retained for more than four hours.

The normalized I_D verses t data can be fit to a stretched exponential equation, Kohlrausch-Williams-Watts (KWW), which is used to describe relaxation in polymers,[68]

$$I_D^{Norm} = E + (1 - E)exp[-(\frac{t}{\tau})^{\beta}] \tag{2.2}$$

where E is the fraction of the decay that occurs outside the time window of the measurement, τ represents the EDL dissipation time, and β is a stretching parameter which describes the distribution of dissipation times. The stretched exponential fit to Equation 2.2 for both $(PVA)_{20}$:$LiClO_4$ (pulsed data only) and $(PEO)_{20}$:$LiClO_4$[5] are also included in Figure 2.5 (dashed lines). In contrast to $(PEO)_{20}$:$LiClO_4$, I_D for $(PVA)_{20}$:$LiClO_4$ does not decay to zero in the time window of the measurement because the EDL has not fully dissipated during this time, and therefore E will assume a non-zero value (∼0.75). In contrast, the EDL of $(PEO)_{20}$:$LiClO_4$ dissipates

on the timescale of milliseconds, and the full decay is captured in the window of the measurement. The stretching exponent, β, is similar for both systems (0.4 to 0.5), indicating a similar distribution of relaxation times. Note that if the data could be described by a single exponential then $\beta = 1$, indicating that the EDL dissipates uniformly with a single time constant, τ. A comparison of the transient current data in Figure 2.5 for $(PEO)_{20}$:$LiClO_4$ and $(PVA)_{20}$:$LiClO_4$ shows that the retention time of the EDL can be increased by 10^6x by increasing the T_g of the polymer by 100 ^{o}C.

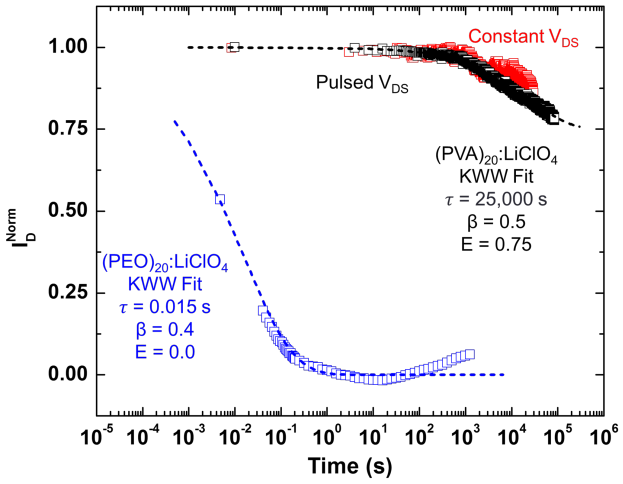

Figure 2.5. Normalized I_D verses time at room temperature after programming an epitaxial graphene FET on SiC with V_{Pr} = +2 V. All terminals are grounded at time equals zero; therefore, the decay in the data indicates the dissipation of the EDL. Measurements for which V_{DS} is held constant for $(PVA)_{20}$:$LiClO_4$ are shown in red, and pulsed are shown in black. Constant V_{DS} measurements for $(PEO)_{20}$:$LiClO_4$ are shown in blue from Li *et al.*.[5] The PEO and pulsed PVA data are fit to the Kohlrausch-Williams-Watts (KWW), Equation 2.2), indicated by the dashed lines. The KWW fitting parameters are provided on the plot. V_{DS} = 0.1 V for all measurements.

The retention time demonstrated in this study does not represent a fundamental limit. It is reasonable to conclude that the retention time can be tuned by tailoring the architecture of a polymer electrolyte to tune the T_g. It is also noteworthy to consider that the EDL dissipation times reported here are accelerated because the top gate is grounded during the measurement - effectively discharging the device like a shorted capacitor. If the top gate were floated instead of grounded, the image charges in the gate and channel would continue to attract the oppositely charged ions, and this Coulomb force will extend the lifetime of the EDL. It is possible that this type of floated gate strategy could be integrated into devices that require long EDL dissipation times. It is important to note that the EDL programming/deprogramming approach demonstrated here is not limited to graphene, but can be extended to any 2D material for which charge in the channel can be modulated using an EDL. This includes transition metal dichalcogenides, such as MoS_2 or WSe_2, for which the on/off ratio would be increased by the presence of a band gap.

Although the data presented above show that the PVA-based electrolyte can significantly increase the EDL retention time, the electrolyte is not thermally stable. This result is illustrated in Figure 2.6 where backgate transfer characteristics on a CVD graphene FET are reported as a function of temperature. The Dirac point shifts to increasingly negative V_{BG} and the current at the Dirac point increases with increasing temperature. The shift in the Dirac point indicates n-type doping, which could result from PVA cross-linking over time. First, because the device is kept in a dry environment during testing and storage, the water content of the film is likely being reduced - especially at higher temperatures. Decreasing water content can promote cross-linking in PVA.[69] Second, a reaction involving the PVA could be occurring at higher temperatures. Because $LiClO_4$ is used as a catalyst in reactions involving alcohols,[70–72] it is possible that similar reactions are occurring in the PVA:$LiClO_4$ film, possibly leading to chemical or physical cross-linking of the PVA.

This cross-linking can give rise to phase separation between the polymer and the salt, and pure $LiClO_4$ will heavily dope the graphene n-type.[73] The presence of phase separation is supported by FTIR measurements of PVA:$LiClO_4$ films which have been heated to 100 ^oC, shown in Figure 2.7a. In agreement with previous reports[74], these spectra show the signature peaks for PVA, but when the salt is added, they also include a peak at 1630 cm^{-1} - a signature of pure $LiClO_4$.[75] The size of this peak increases with increasing annealing time at T = 100^oC.

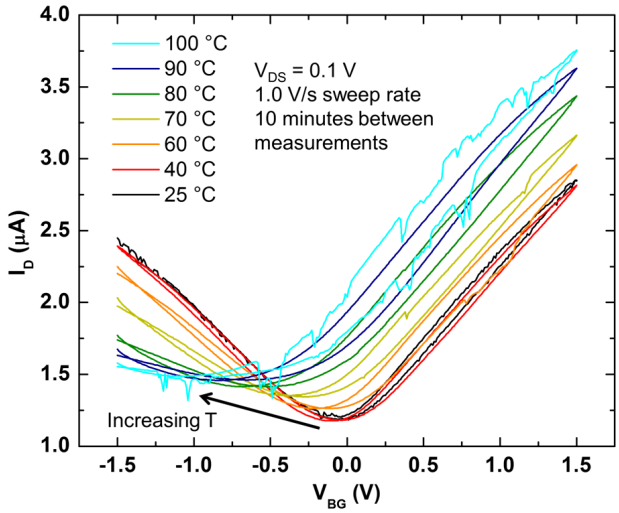

Figure 2.6. Back gate transfer characteristics of a CVD graphene FET on SiO_2 with $(PVA)_{20}$:$LiClO_4$ at increasing temperatures. The left and upward shift of the Dirac point indicates that n-type doping is occurring. Back gate leakage is less than 1 nA for all points in this measurement.

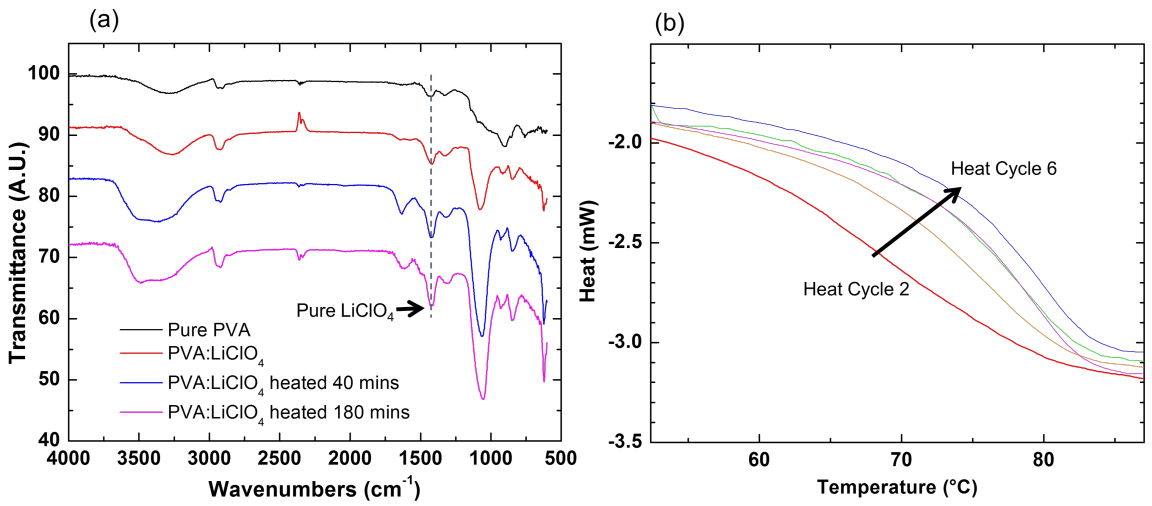

Figure 2.7. (A) FTIR spectra of PVA:$LiClO_4$ (and a pure PVA control), heated to 100 ^oC for varying times showing the growth of the 1630 cm^{-1} peak, indicating an increase in pure $LiClO_4$ as the sample is heated for longer time periods. (B) Heat scans 2-6 of repeated DSC measurements showing an increase in T_g as a function of heat exposure.

To provide more information on whether or not the PVA is being thermally cross-linked, six consecutive DSC heating scans were taken from 25 to 100 ^oC with a 10 minute hold at 100 ^oC to replicate the conditions in Figure 2.6. These measurements track the T_g as a function of temperature, and the results are shown in Figure 2.7b. The first run eliminated thermal history and is therefore not shown in the figure. Scans two through six show that the T_g increases with repeated heat exposure, suggesting that the PVA is thermally cross-linking. In combination, the DSC and FTIR data suggest that the electrolyte cross-linking is driving phase separation between the PVA and the $LiClO_4$, and that the pure $LiClO_4$ is causing irreversible n-type doping of the graphene devices. Based on the data collected, there is no indication that the cross-linking occurs at room temperature, but is instead thermally activated.

Because this reactivity, as well as the anhydrous cross-linking are both likely

specific to this electrolyte, by carefully selecting a polymer/salt combination that will not have these drawbacks, this issue can likely be overcome. Regardless, this work demonstrates that large sheet carrier densities can be established and maintained for hours at room temperature by choosing an electrolyte with T_g higher than room temperature.

2.4 Conclusion

The EDL retention time of a 2D crystal FET can be increased by increasing the T_g of the electrolyte gate. Specifically, for an EDL with $n_s = 6.3 \pm 0.03$ x 10^{13}, the room-temperature retention time can be increased 10^6x by replacing $(PEO)_{20}$:$LiClO_4$ with $(PVA)_{20}$:$LiClO_4$. The ability to induce ultra-high charge carrier densities in a 2D device and lock-in the doping for a predetermined time interval could provide new device functionality that may be useful for novel devices using SPEs. In addition to modulating the retention time, the deposition of a photolithographically patterned gate directly on the electrolyte surface is demonstrated for the first time. While polymer electrolytes have proven extremely useful for exploring transport in 2D materials, they are frequently gated using a probe tip to touch the surface of the electrolyte near the device - an impractical approach for device application, or using a side gate, which slows the EDL formation. However, the demonstration of a lithographically defined top gate represents an initial step towards practicality. With adequate control of the polymer chemistry to provide sufficient thermal stability to avoid irreversible n-type doping, the approach of using "locked" EDLs to store information with the ability to deprogram on command or at a specified time represents a new functionality for 2D, EDL-doped transistors.

CHAPTER 3

GATING MoS_2 FIELD EFFECT TRANSISTORS USING POLY(ETHYLENE OXIDE) AND LITHIUM PERCHLORATE SOLID POLYMER ELECTROLYTE[1]

3.1 Motivation

As shown in previous chapters, electrostatic doping of 2D materials using an electrostatic double layer (EDL) is achieved by applying a bias smaller than the electrochemical window of the electrolyte, which is typically around 4 V for polymer electrolytes and ionic liquids.[76–78] With this approach, charge is not exchanged between the electrolyte and the 2D material, rather it is induced at the interface of the two materials. However, if the applied bias exceeds the electrochemical window, then reduction and oxidation reactions will occur to the cations and anions in contact with the 2D material. For example, Li^+ will be reduced to Li^0, where the electron required for the reduction is supplied by the source. The Li_0 (*i.e.*, lithium metal) can be reversibly oxidized to Li^+ by reversing the polarity of the gate bias. This is the fundamental electrochemistry that occurs in rechargeable lithium-ion batteries.[79]

When the voltage exceeds the electrochemical window, the ions are not simply driven to the outermost layer of the 2D material. Ions also intercalate between the layers and undergo reduction/oxidation (*i.e.*, redox) reactions within these layers. The high-density intercalation of ions into electrodes comprised of layered materials

[1]Related Publication: Erich Kinder; Rusen Yan; Huili (Grace) Xing; Susan Fullerton-Shirey "High-field characteristics of electrolyte-gated MoS_2 field effect transistors", Target Journal: Physical Review B, In preparation.

Contributions: Kinder - electrolyte preparation, electrical measurements; Yan - device fabrication; Xing - data interpretation; Fullerton - directing author

permits charge to be stored in a battery. Ion intercalation into MoS_2 is well studied and has been demonstrated for both exfoliated[80] and sputtered[81] MoS_2. In addition to energy storage, intercalation of ions in 2D materials is attractive for 2D electronics because it can be used to convert MoS_2 from the semiconducting 2H phase to the metallic 1T phase, as shown both experimentally[82] and theoretically[83]. Li transfers charge to the MoS_2, stabilizing the 1T phase[83], which has proven useful for decreasing contact resistance in MoS_2-based devices.[84, 85]

One drawback that affects both the electrostatic and electrochemical doping of 2D materials by a solid polymer electrolyte is ion speed. Increasing ion mobility through polymer electrolytes has been a goal of the battery community for several decades.[86] Our group has shown that the EDL response time in PEO:$LiClO_4$ at room temperature is on the order of ms; however, a full-strength EDL (*i.e.* $n_s = 10x^{14}$ cm^{-2}) takes seconds to establish.[5] Operating speeds of ms to seconds are not useful for electronic devices that need to operate with MHz to GHz frequencies. Thus, our group is seeking to electrostatically dope 2D materials while overcoming the slow response of ions to the applied electric field. One approach is to apply voltages larger than the electrochemical window (*i.e.*, large driving force) for short time periods (*i.e.*, ns to ms pulses). Our hypothesis is that if the pulse time is sufficiently short, and the field-strength is sufficiently large, the larger driving force will speed-up the ion response without providing sufficient time for electrochemistry or dielectric breakdown of the polymer to occur. Breakdown typically occurs at 200 V/cm for polymers such as polyethylene and PTFE;[87] however the speed over which breakdown occurs is less understood.

To know whether or not the pulsed approach is successfully avoiding electrochemical reactions or dielectric breakdown, we must first identify the signature of these events by purposely driving devices to voltages that exceed the electrochemical window for periods of time longer than the EDL formation time ($>$ 10 ms).

Once the signature of breakdown and device failure are identified, they can be used as a control measurement by which to compare the pulsed results. Therefore, this chapter describes transfer characteristics for MoS_2 FETs for which the gate voltage is purposely swept within, and one order of magnitude beyond, the electrochemical window (zero to 40 V). The transfer characteristics show reproducible hysteretic behavior with well-defined electrochemical peaks associated with the reduction and oxidation of ions within the MoS_2. The introduction of large numbers of ions between the layers causes a volumetric expansion of the channel which ultimately leads to mechanical fracture and device failure. The number of cycles to failure increases with increasing channel thickness.

3.2 Experimental Details

MoS_2 was exfoliated from a bulk crystal (SPI Supplies) using the Scotch tape method and placed on an RCA-cleaned $p++$ Si wafer with 285 nm of SiO_2. Flake thicknesses were measured using a Bruker Dimension Icon Atomic Force Microscope (AFM), in ScanAsyst mode, using a Si probe on a SiN lever (for more information see Appendix A). Electron beam lithography was used to pattern Ti/Au (5 nm/60 nm) source and drain contacts on the MoS_2 flakes. Three devices with MoS_2 thicknesses varying from 6 to 46 nm (16 - 120 layers) were fabricated. Prior to electrolyte deposition, control measurements were made on all devices by monitoring the drain current, I_D, while sweeping the backgate voltage, V_{BG} (Figure 3.1a, black trace). These transfer characteristics show that all devices displayed n-channel behavior prior to electrolyte deposition, consistent with previous reports of exfoliated MoS_2 FETs.[88, 17]

A 1.0 wt% polymer electrolyte solution was prepared in anhydrous acetonitrile (Sigma Aldrich, 99.8%) by dissolving poly(ethylene oxide) (PEO), (Polymer Standards Service, Mw = 94,600) and $LiClO_4$ (Sigma Aldrich, 99.9%) in a 20:1 molar

ratio. The electrolyte was drop-cast onto the surface of the MoS_2 FETs, annealed at 80 ^oC for 3 minutes on a hotplate, and placed on the bench top to cool to room temperature. This procedure yielded a 1.0 μm thick film, as measured by AFM. A probe tip (tungsten, 5 μm radius, Cascade Microtech, Inc.) was used as a topgate by positioning it over the channel in contact with the electrolyte surface. The probe covered approximately 25% of the channel area.

Electrical measurements were made on an Agilent B1500A Semiconductor Parameter Analyzer, in a dark, nitrogen-filled Cascade Summit 11000 probe station at room temperature. The source contact was grounded and the source-drain bias, V_{DS}, was held at 0.5 V while the topgate bias, V_{TG}, was swept from 0 to 40 V; 40 to -40 V; and -40 V to 0 V at a sweep rate of 0.5 V/s. Because intercalated ions can change their oxidation state during the measurement, large hysteresis can occur within and between measurements. Therefore, all measurements were made in the same order for each device, so that the electrical characteristics of devices with different thicknesses could be compared.

3.3 Results and Discussion

Devices with three channel thicknesses (16, 60, 120 layers) were measured by repeatedly cycling V_{TG} between +/- 40 V while maintaining V_{DS} at 0.5 V. The number of cycles before failing to open circuit increased with increasing thickness, as shown in Table 3.1. The $I_D - V_{TG}$ characteristics during failure are provided in Appendix B Figure 1. The irreversible dielectric breakdown of polymers (without a dissolved salt) typically results from thermal breakdown. The leakage current originates from electrons excited from deep donor traps[89], and the magnitude of the leakage current increases with increasing polymer temperature. As the leakage current increases, this further increases the temperature of the polymer.[90] For low fields and low temperatures, equilibrium can be reached as the heat dissipates; however, for biases

above the critical voltage of the film, the positive feedback loop leads to thermal runaway of the device, resulting in an electrical short through the polymer. Thus, because the MoS_2 devices measured here fail to open circuit, it suggests that the failure mechanism is not the dielectric breakdown of the polymer, because breakdown would instead result in an electrical short between the gate and drain/source. The leakage current is below 10 nA for the entire voltage window for all devices, (shown in Appendix C, Figure C.2).

The 120 layer device is the only device that did not fail during cycling. The back-gate transfer characteristics of the device without the electrolyte gate deposited on the surface (Figure 3.1a, dashed line) show n-FET operation, as expected for exfoliated MoS_2 FETs with Ti contacts.[91] The first and fifth cycles using the electrolyte gate are illustrated in Figure 3.1a with red and blue lines, respectively. The electrolyte gate converts the device transfer characteristics from nearly hysteresis-free n-channel FET behavior to strongly hysteretic behavior with electrochemical peaks. During the first cycle with the electrolyte gate, the current increases by more than an order of magnitude under positive bias. This large increase in current shows that Li^+ acts as a dopant. If the Li^+ intercalates into the MoS_2 it will be reduced at these voltages and could provide the charge transfer necessary to stabilize the MoS_2 in the highly conductive 1T phase.[85] The intercalation and reduction are depicted in schematics (II) and (I) of Figure 3.1a, respectively. Further discussion of this electrochemical cycling explanation, as well as band diagrams modeling the device behavior during electrochemical cycling can be found in Appendix C.

The current maximum decreases in magnitude from the first cycle to the fifth cycle until the cycle-to-cycle deviation is minimized for cycles 6-19 (Figure 3.1b). One possibility is that the subsequent decrease in conductivity from the first cycle to the subsequent cycle in Figure 3.1a corresponds to a phase change from 1T MoS_2 (metallic) to Li_2S (semiconducting).[92] While Raman spectra were taken following

TABLE 3.1

DEPENDENCE OF DEVICE LONGEVITY ON THICKNESS

Number of Layers	Number of Cycles Before Failure
16	6
60	18
120	N/A*

* Device did not fail under testing

voltage cycling, they showed no indication of the 1T MoS_2 phase (Appendix C, Figure C.3). This suggests that if MoS_2 does transition to the highly conductive 1T phase, it does not do so permanently. Raman spectra would need to be acquired *in situ* as a function of electrical cycling to verify the existence of the 1T phase during voltage cycling.

Cycles 6-19 in Figure 3.1b provide evidence of electrochemical redox cycling with well-defined electrochemical peaks occurring at ±20 V. Peaks such as these are frequently seen in cyclic voltammetry measurements (*i.e.*, I-V measurements typically used to measure electrochemical reactions).[93] For the peak on the right, the increase in current that begins near 15 V is the onset of the reaction, where only higher energy electrons (*i.e.* thermally excited) can react with the ion. As the voltage is swept higher, more electrons are available for reaction, increasing the current. The peak forms when a diffusion layer is formed around the electrode (in this case, the channel), and the rate of new reactants reaching the electrode limits the current. The opposite of this reaction begins at -15 V, and is seen as a sharp decrease in current because holes are the charges used in this electrochemical reaction. In this work, we

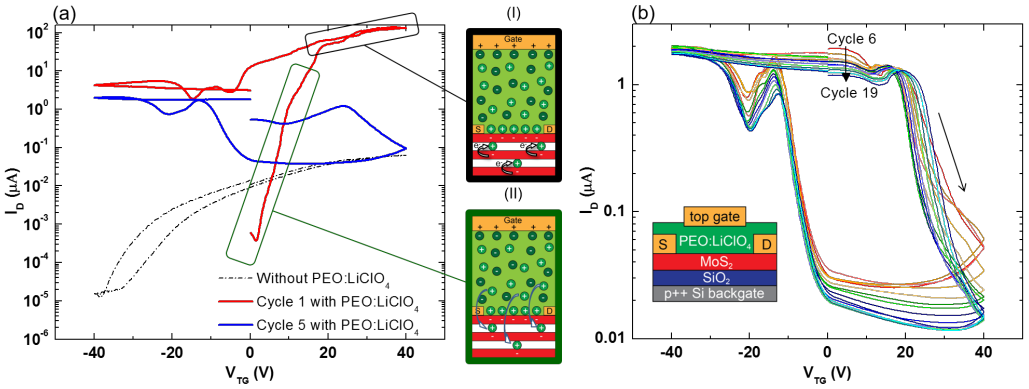

Figure 3.1. (a) $I_D - V_{BG}$ sweep wiout $PEO:LiClO_4$ (the device is backgated) and the first and fifth I_D-V_{TG} sweeps with $PEO:LiClO_4$ (the device is topgated) of a 120-layer device showing an increase in current that exceeds five orders of magnitude due to Li^+ intercalation (I) and electrochemistry (II). These data show the overall conversion of the device from largely hysteresis-free n-channel behavior without $PEO:LiClO_4$ to hysteretic behavior with electrochemical peaks with $PEO:LiClO_4$. (b) The following 14 topgate sweeps on the same device showing two electrochemical features and pronounced hysteresis.

propose that the electrochemical peaks are from Li^+ reducing to Li^0 at the peak in the positive bias regime and oxidizing from Li^0 to Li^+ at the peak in the negative bias regime. However, to confirm this, a pure lithium metal reference electrode would need to be designed into this system because the reduction potential of pure lithium is known.

The intercalation of Li^+ into the MoS_2 causes the channel of the 120 layer device to swell by 35% at minimum to over 400% in some areas, causing deformation and cracking, as illustrated by the optical images and AFM measurements shown in Figure 3.2 before and after the $I_D - V_{TG}$ measurements. Notice that this change in height cannot be attributed to electrolyte residue because the surface of undamaged MoS_2 and the surrounding SiO_2 both have surface roughness (R_q = 4.2 nm) that is nearly equivalent to the surface roughness before the electrolyte was deposited (R_q = 3.6 nm). Such swelling due to intercalation is consistent with other reports of Li-intercalated MoS_2 devices.[94] The expansion of the channel under cycling imparts stress because the contacts physically anchor the channel to the substrate at both ends. The stress is relieved by cracking - presumably along crystallographic defects in the flake.

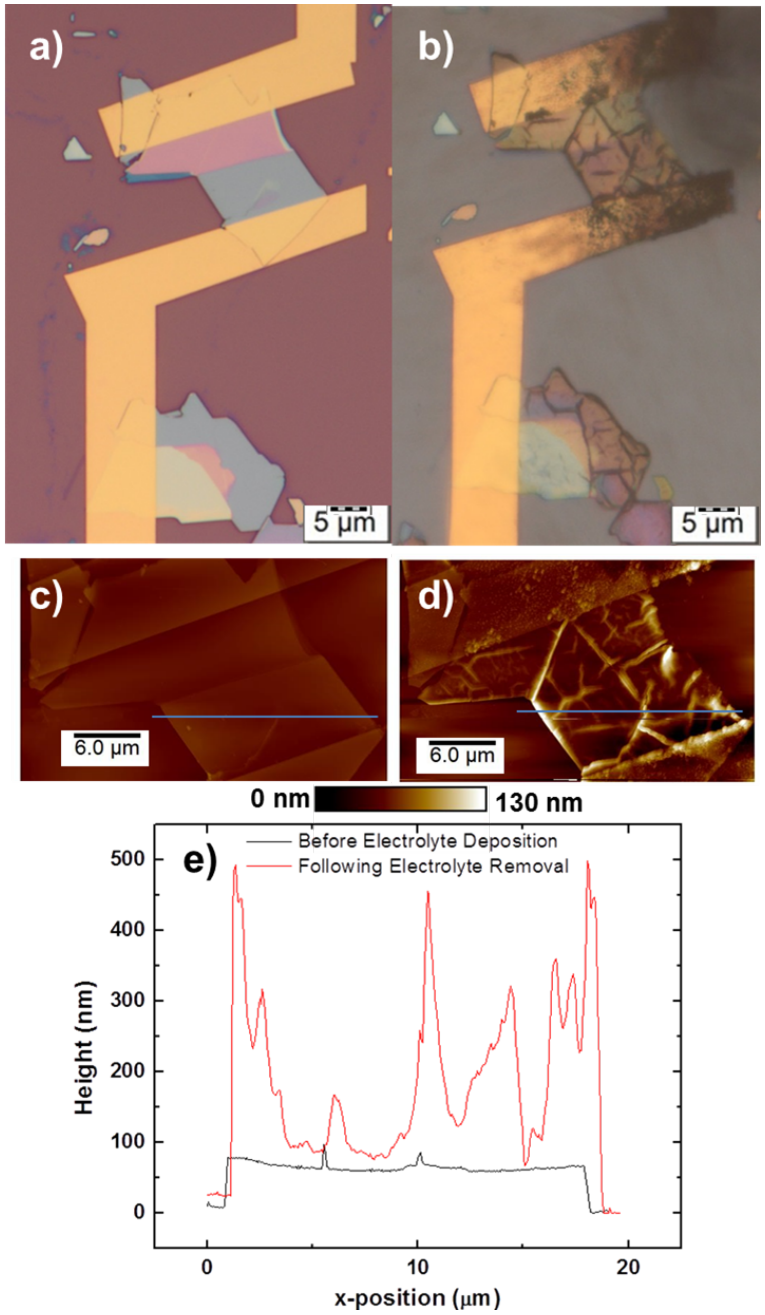

Figure 3.2. Optical images of 120 layer MoS_2 FET (a) before electrolyte deposition and V_{TG} cycling and (b) after, showing the cracked channel along with discolored contacts due to electrochemical reactions. AFM scan of the same device, (c) before electrolyte deposition and V_{TG} cycling and (d) after V_{TG} cycling and electrolyte removal. Blue lines in the AFM images indicate the location of the line scans (e).

As mentioned above, the fracture of the devices thinner than 120 layers causes them to fail to open circuit, with the time to failure increasing with device thickness. One possible explanation is that thicker channels have more conductive pathways from source to drain than thinner channels, and are therefore more tolerant of small fractures. In contrast, fractures can more easily propagate through the entire body of thinner devices, thereby removing all pathways for electrical conduction. The fracture of the thinnest devices was further evidenced by the observation that the 16 and 60 layer MoS_2 channels were washed away while removing the polymer electrolyte with an acetonitrile solvent clean. In contrast, the thickest device of 120 layers, while heavily fractured and swelled, was not washed away, and the channel remained electrically conductive.

Previous work by Xiong *et al.* where Li^+ was intercalated into 35-layer MoS_2 showed an approximately 50% increase in thickness of the intercalated MoS_2, as well as cracking in thicker devices (but not in thinner devices).[94] However, Xiong *et al.* intercalated and de-intercalated at much smaller biases of 1.1 and 3.2 V with respect to a pure lithium reference electrode (*i.e.*, an electrode that monitors the Li/Li^+ reaction). As mentioned above, the devices studied in this work do not include a reference electrode, meaning we cannot confirm that the electrochemical peaks we observe are cycling of Li without additional measurements.

The optical image in Figure 3.2b also shows that regions of the Ti/Au contacts closest to the MoS_2 channel show some discoloration. It is possible that this represents electrochemical deposition of Li^+ on the gold surface in the region where the field is the strongest (*i.e.*, near the channel). While electrodeposition would be accompanied by a change in height on the contacts that could be detected by AFM, it would not be a conclusive analysis because the deposits could also be residual polymer electrolyte. Therefore, this assertion of electrodeposition of lithium on the contacts would need to be verified using a chemically sensitive spectroscopy technique such as

X-ray photoelectron spectroscopy (XPS) after the polymer electrolyte is removed.

As shown in Figure 3.1, cycling the device through +/- 40 V introduces hysteresis that exceeds two decades in I_D. It is therefore instructive to determine if this shift from low to high conductivity can be retained after setting the state and removing the applied bias. To test the state retention, the device is set to the low conductivity state by applying a +30 V topgate bias for 100 seconds (Figure 3.3). The topgate is then grounded and I_D is monitored to determine how long the state is retained. For the high conductivity state, the same procedure is used with V_{TG} = -30 V. The data in Figure 3.3 show that the current remains high for the high conductivity state; however, the current increases over time when set to the low conductivity state. The inability to retain the low conductivity state is consistent with the fact that Li has the most negative reduction potential of any element, and therefore, the oxidation of Li^0 to Li^+ is highly favored in the absence of an applied bias.[87] As intercalated Li^0 donates electrons, the current increases over the timescale of five minutes, as it converts from the low conductivity to high. The peak in the I_D vs time data is likely due to mass-transport limiting the current as discussed above for the I-V measurements.

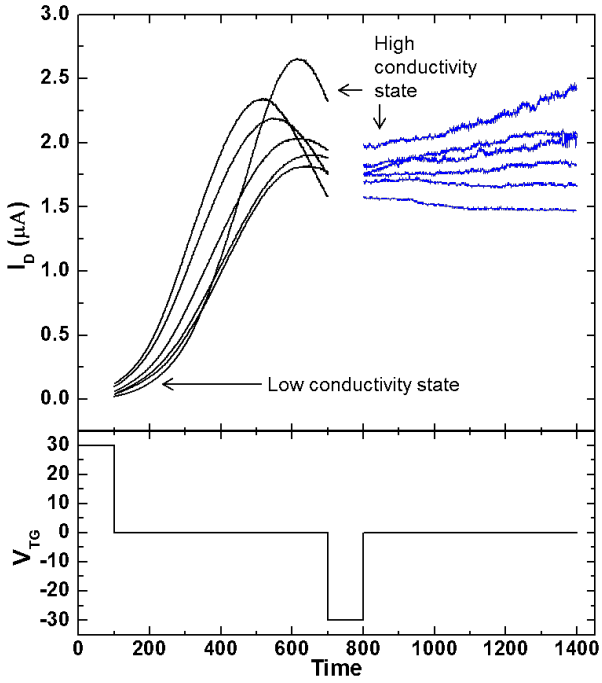

Figure 3.3. State retention test. After applying a V_{TG} = +30 V for 100 s, the bias is removed and the current is monitored for 600 seconds. Next, V_{TG} = -30 V is applied for 100 s, the bias is removed, and the current is monitored for 600 seconds. The cycle is repeated 6 times, corresponding to the six black (low conductivity state) and blue (high conductivity state) traces. While the high conductivity state is retained after negative biasing, the low conductivity state is retained only for a few seconds. V_{DS} = 0.5 V for all measurements.

3.4 Conclusion

Electrolyte-gated MoS_2 FETs of varying channel thickness (16 to 120 layers) were fabricated and the electronic properties were monitored as the gate bias was swept one order of magnitude beyond the electrochemical window. By operating the FETs outside the electrochemical window of the electrolyte, the device was changed from n-channel FET behavior to a hysteretic behavior with more than two decades of

change in current, presumably through the intercalation and subsequent reduction and oxidation of Li. In addition to electrochemical peaks, intercalation of Li is supported by an increase in the thickness of the channel by at least 1.35x its original thickness. The thinnest devices (*i.e.*, those less than 120 layers) failed during cycling to open circuit. When considering the characteristics of electrical failure along with the AFM images, the failure mechanism is likely mechanical fracture of the channel and not dielectric breakdown of the polymer. Such dielectric breakdown would manifest as a large leakage current from gate to drain/source rather than an open circuit, and would be preceded by stress-induced leakage current that increases with increasing time or voltage. Device longevity (*i.e.*, the number of $I_D - V_{TG}$ cycles before failure) increases with increasing channel thickness. The thickest devices can better tolerate fractures caused by Li^+ intercalation, possibly because the number of conductive pathways from source to drain increases with layer thickness.

This study informs pulse measurements of PEO:$LiClO_4$-gated FETs at high field strengths by showing the electrochemical and physical signatures that might be present if the pulse speed is too slow. For example, hysteresis in electrical conductivity would indicate that the electrical stress may be sufficiently high to induce elctrochemistry that may or may not be reversible. Another example is volumetric expansion of the channel, which can be directly measured with AFM before and after the pulse measurements.

CHAPTER 4

GRAPHENE FETS BACKGATED WITH A SOLID POLYMER ELECTROLYTE[1]

4.1 Motivation

Our group has recently developed a so-called "monolayer electrolyte" consisting of cobalt crown ether phthalocyanine (CoCrPc) and lithium salt.[95, 96, 73]. The CoCrPc molecule, shown in Figure 4.1, is a phthalocyanine surrounded by four crown ethers. The Li^+ ions are bistable within the crown ethers of the CoCrPc, with energetically favorable positions for the ion located just above or below the plane of the ring-shaped crown ether.[96] Our group showed that the electrolyte can be deposited by simple solution-casting and annealing into a flat, ordered monolayer of a 2D crystal.[95] DFT calculations show that the Li^+ can then be repositioned by an applied bias to the location either close to or farther away from the channel.[96] Thus, the ions in the crown will act like an ionic dopant, inducing image charge in the underlying channel. Xu *et al.* have demonstrated the monolayer deposition of CoCrPc:$LiClO_4$ on the channel of a graphene FET.[73] By using the backgate to modulate the position of the Li^+ ions, a non-volatile, two-state system (*i.e.*, Li^+ close to the channel and Li^+ further away from the channel) is formed, demonstrating a simple memory device.

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[1]Related Publication: Erich Kinder; Buchanan Bourdon, Alan Seabaugh; Susan Fullerton-Shirey "Transfer of Graphene FETs onto a Solid Polymer Electrolyte", In preparation, Projected June 2017 submission.

Contributions: Kinder - electrolyte preparation, device fabrication, electrical measurements; Buchanan Bourdon - COMSOL modeling; Seabaugh - motivated original idea and provided input; Fullerton-Shirey - directing author

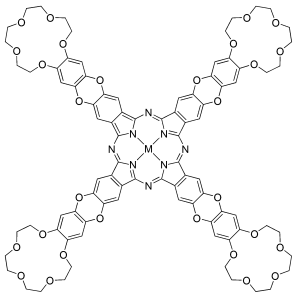

Figure 4.1. The chemical structure of crown ether phtyalocyanine where M is the metal center (Co for this work).

The eventual goal of the CoCrPc:$LiClO_4$ work is to form a single-transistor, stacked monolayer memory element, illustrated in Figure 4.2. By depositing a monolayer electrolyte onto a 2D crystal backgate, then transferring a 2D FET on top of the electrolyte, the doping level of the 2D FET can be changed, thereby controlling the memory state of the device.

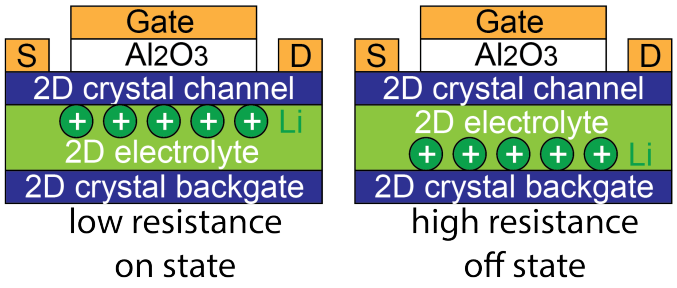

Figure 4.2. Schematic of a 2D crystal memory element consisting of a 2D crystal FET on a 2D electrolyte.

One fabrication challenge for the device shown in Figure 4.2 is that the monolayer electrolyte is soluble in water and other polar solvents typically used in photolithography.[95] Our group showed that annealing at 150 ^{o}C for 5 minutes in air significantly degrades the quality of the film, increasing the surface roughness and leading to CoCrPc aggregates on the graphene surface.[95] This means that after the monolayer electrolyte is deposited on a substrate, it cannot be exposed to polar solvents. Thus, one required fabrication step for the device in Figure 4.2 is transferring a completed 2D FET directly onto the monolayer electrolyte - a technique that has not been demonstrated previously.

As described in this chapter, we demonstrate an approach to transfer fabricated graphene FET devices directly onto a solvent-sensitive substrate, fabricating the device illustrated in Figure 4.3b. Although the yield reported in this work is low, and this technique would need to be refined for the monolayer electrolyte, to our knowledge it is the first demonstration of the transfer of a working 2D FET onto a solid polymer electrolyte (SPE) and the first demonstration of a SPE backgate.

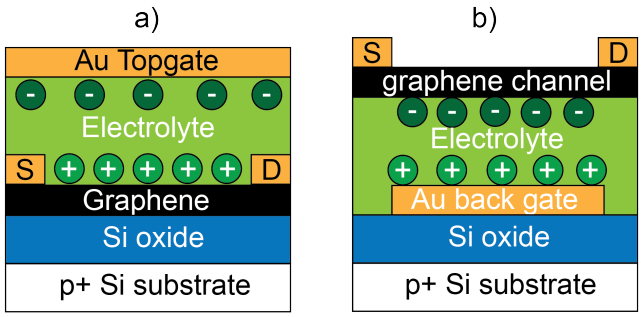

Figure 4.3. (a) Schematic of a traditional electrolyte topgated graphene FET. (b) Schematic of the backgated graphene FET with a patterned Au backgate fabricated in this work.

In addition to the experimental demonstration, COMSOL Multiphysics is used to provide physical insight into the ion-transport happening within the electrolyte in response to the applied field. Specifically, the modeling shows that the hysteresis in the transfer characteristics of the electrolyte-gated FETs can be attributed to the ion response to varying sweep rates.

The most common way to use an electrolyte to gate a FET is to deposit the electrolyte directly onto the exposed channel of the FET and then use either a top (Figure 4.3a) or side gate to control the EDL.[20, 13, 21] This only allows for gating the channel from the direction of the top gate (*i.e.* the top surface of the channel). The backgate can also be used to control the EDL in such a structure; however one of the drawbacks of this device operation is the significant voltage drop across the channel material, which reduces the coupling of the backgate to the electrolyte. By placing a fabricated FET onto the surface of the electrolyte, a device with an electrolyte backgate can be formed. Not only is this backgating strategy required for the stacked 2D memory device outlined above, but other devices can benefit from such backgating. For example, by doping the channel of an electrolyte-backgated FET using the ion-locking strategy discussed in Chapter 2, the channel of a FET can be made *n*- or *p*-type while a conventional MOS topgate stack can be used to modulate the channel. One additional advantage of this device architecture is that such a structure not only gates the channel, but also the 2D material under the metal contact, allowing the contact to be gated (unlike an electrolyte topgate, which can only gate the portion of the contact touching the electrolyte). This can open up larger design space for fabrication, allowing for further contact engineering beyond just metal choice. By electrolyte gating the contact, the Schottky barrier that exists in most contacts to 2D materials can be thinned, decreasing contact resistance.[97]

4.2 Graphene Transfer Introduction

As discussed in Chapter 1, transfer of wide-area CVD-grown graphene is typically accomplished using a PMMA handling layer - this transfer is shown schematically in Figure 4.4. First the graphene (on the sacrificial growth substrate, typically Cu, Figure 4.4a) is coated in PMMA, shown in Figure 4.4b. This handling layer keeps the graphene intact and allows for moving the graphene layer to a DI water bath following the etching of the metal growth substrate (Fibure 4.4c). The target substrate is then placed in the DI water bath and is used to remove the PMMA/graphene structure (Figure 4.4d). The target substrate/graphene/PMMA structure is then allowed to dry, ensuring adhesion between the target substrate and the graphene layer (Figure 4.4e). Last, the PMMA handling layer is removed using an acetone bath (Figure 4.4e).

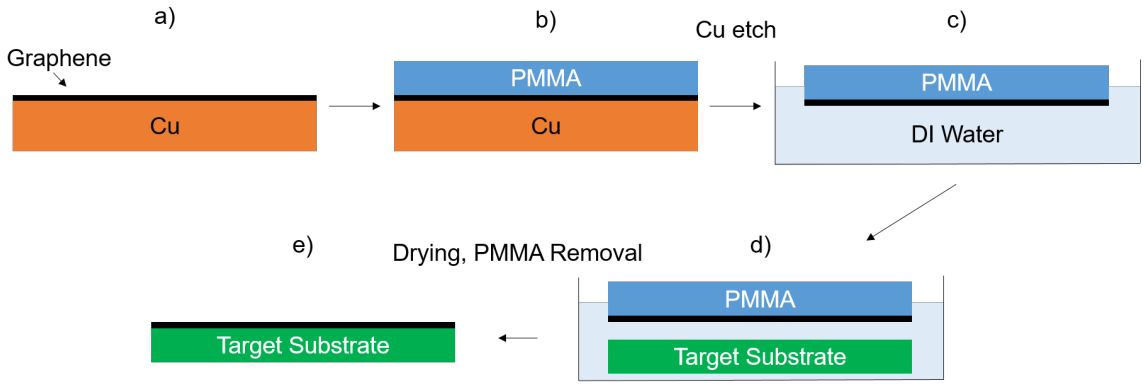

Figure 4.4. Process flow showing the transfer of wide-area CVD-grown graphene using a PMMA handling layer. (a) Graphene grown on Cu substrate *via* CVD. (b) PMMA handling layer is applied and the Cu etched (b to c). (d) The PMMA/graphene is rinsed in DI water and placed on the target substrate. (e) After drying, the PMMA is removed leaving the graphene on the target substrate.

The approach in this work is to first fabricate graphene FET devices on CVD graphene using optical lithography. Then, etch the underlying copper substrate for transfer onto the target substrate as shown in Figure 4.4. It would not be much of advantage for the target substrate to be SiO_2, because graphene device fabrication on SiO_2 is well developed. However, if the target substrate cannot withstand the processes used in fabricating a graphene FET - such as a polymer electrolyte - then a completed device transfer is required. Similar to the monolayer electrolyte, CoCrPc, PEO:$LiClO_4$ is another example of an electrolyte that is soluble in the solvents used in photolithography, including water, acetone and isopropanol. By transferring completed graphene FET devices onto a PEO:$LiClO_4$ substrate, we are able to avoid performing lithography directly on the electrolyte, while still fabricating an electrolyte backgated graphene FET.

To transfer graphene devices onto a PEO:$LiClO_4$ film, a handling layer that can be removed without damaging the target substrate is key. PMMA is not a good choice for a handling layer in this case, because both PMMA and the electrolyte, PEO:$LiClO_4$ are soluble in the same solvents. An ideal handling layer would be a polymer, or combination of polymers, that meets the general requirements for a handling layer (*e.g.,* mechanical rigidity, insoluble in metal enchants and water), but also has orthogonal solvents to the electrolyte. For example, an orthogonal solvent for a PEO-based electrolyte would be one that cannot dissolve PEO but can dissolve the handling layer. One polymer that fits most of these requirements is Polyisobutylene (PIB). PIB is insoluble in all the solvents and metal enchants used in typical photolithography on graphene, and has an orthogonal solvent to PEO, hexane. However, a deposited film of PIB is not structurally rigid. To provide rigidity, a stamp of polydimethylsiloxane (PDMS) is applied to the PIB surface to increase structural integrity.

4.3 Experimental Methods

4.3.1 Graphene FET Fabrication

Graphene FETs were fabricated on graphene provided by the Korean Institute for Science and Technology (KAIST). This graphene was grown *via* a CVD process on a Cu film that has been previously evaporated onto an SiO_2 wafer. The Cu on SiO_2 wafer provides a rigid substrate for the device to be fabricated on, prior to the graphene release etch. For the deposition of alignment marks, PMGI SF9 was spin-coated onto the graphene surface, followed by a 5 minute hard bake at 180 ^oC. To form the bilayer resist structure, SPR 700-1.2 was then spin-coated directly onto the PMGI SF9 surface and baked at 100 ^oC for 3 minutes. The sample was then exposed to 70 mJ/cm^2 of i-line radiation using a Karl Zeiss Mask Aligner. To develop the resist, the sample was immersed in a room temperature bath of AZ 917 MIF developer (Microchem) for 45 seconds. An adhesion layer of 5 nm of Ti, deposited at 1.0 Å/s by the Temscale FC-1800 electron beam evaporator, was used for the Au contacts (245 nm thick, 2 Å/s deposition rate). Lift-off was then performed using a 60 ^oC acetone (Semiconductor grade, Sigma-Aldrich) bath followed by an isopropanol (Semiconductor grade, Sigma-Aldrich) bath.

To deposit the source/drain contacts, the same bilayer resist structure described above is used. Prior to metal evaporation, the sample was placed in the chamber until the base pressure decreased to 2 x 10^{-6} torr. Ti was then evaporated with the shutter closed at a rate of 0.5 Å/s to further lower the base pressure, typically to 8 x 10^{-7} torr. The same 5 nm/245 nm Ti/Au layer described above is then deposited, then lifted off using a 60 ^oC acetone bath followed by a room temperature isopropanol rinse.

4.3.2 Substrate Preparation

To backgate a device with an electrolyte, there must be a conductor on the surface of the substrate on which the electrolyte will be deposited. Two types of substrates were used. The first substrate was Ti/Au electrodes on SiO_2. 50 μm wide Ti/Au electrodes were deposited with a separation distance of 50 μm, onto an Si/SiO_2 substrate, using standard photolithography and lift-off. The process flow for this fabrication is illustrated in Figure 4.5.

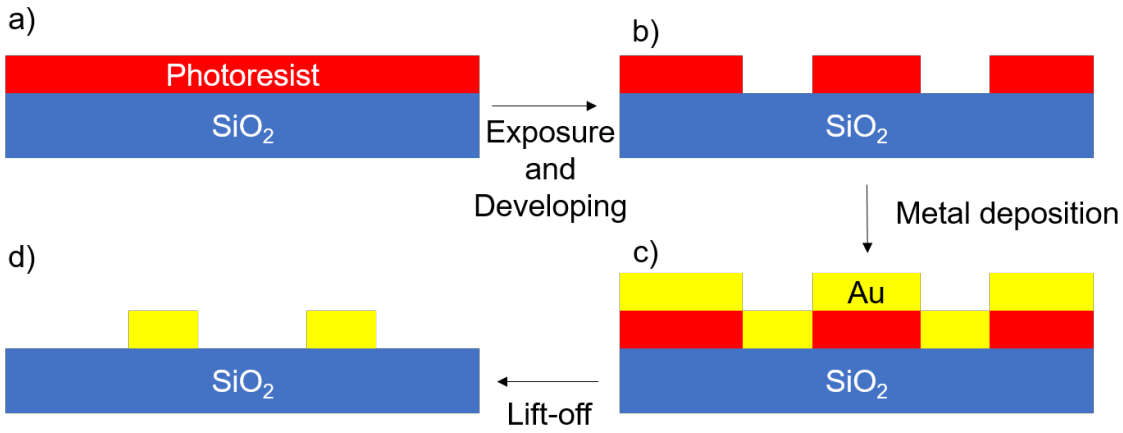

Figure 4.5. Process flow for the fabrication of a Au backgate structure. (a) A wafer with 300 nm SiO_2 is coated in photoresist, (b) which is then patterned. (c) Metal is evaporated over the whole structure, then (d) lifted-off to provide Au electrodes on SiO_2.

The second substrate was epitaxially grown graphene on SiC. In this case, the same backgate mask was used with the opposite tone resist to give 50 μm wide pillars of resist spaced 50 μm apart. The substrate was then placed in an RIE with an RF power of 150 W and DC bias of 330 V for 60 s in an oxygen environment to

etch the graphene unprotected by resit, forming into parallel electrodes. Figure 4.5 illustrates the steps taken to fabricate this backgate contact structure.

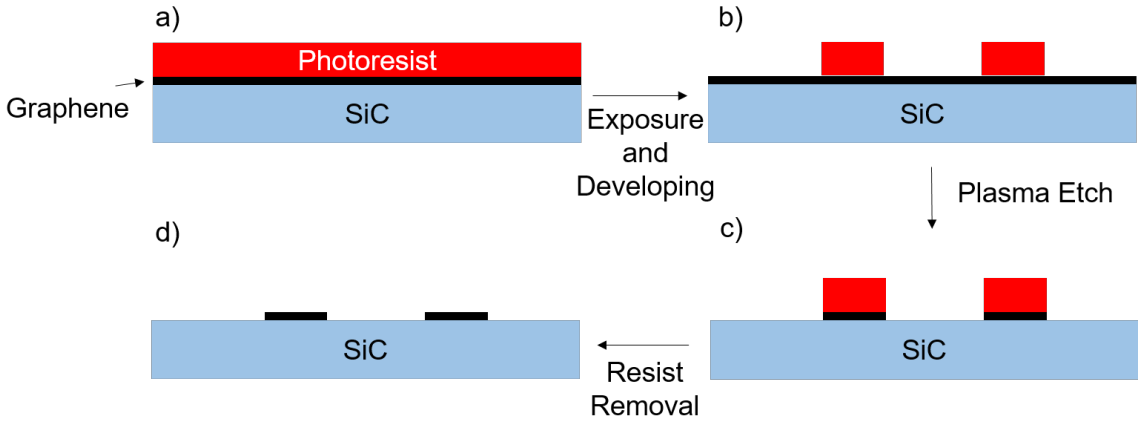

Figure 4.6. Process flow for the fabrication of a graphene backgate structure. (a) A graphene sample grown on SiC is coated in photoresist, which (b) is then patterned. (c) Oxygen plasma is then used to etch any exposed graphene. (d) The resist is then removed using acetone to leave evenly spaced graphene electrodes on the SiC surface.

4.3.3 Polymer Electrolyte Preparation

The SPE was prepared in an argon-filled glovebox (O_2 and H_2O levels < 0.1 ppm) by combining polyethylene oxide (PEO, Polymer Standards Service, 100,000 g/mol molecular weight) with lithium perchlorate ($LiClO_4$, Sigma-Aldrich, 99.9%) in a 20:1 ether oxygen:Li ratio. Acetonitrile (99.99%, Sigma-Aldrich) was then added to make a 1 wt% solution of PEO:$LiClO_4$. Approximately 1 mL of this solution was then dropcast onto one of the 1x1 cm^2 prepared substrates. The sample was then left in the glovebox until all solvent had evaporated. The substrate was then placed on a 80 ^oC hot plate for 3 minutes to drive off any remaining solvent and to anneal the

polymer film.

4.3.4 Semi-Dry Transfer Method

PIB and PDMS (as described above) was chosen as the the handling layer for this transfer method, because it is soluble in hexane, which is an orthogonal solvent for PEO. First, graphene FETs were fabricated on the graphene-covered substrate (graphene/Cu/oxide/Si) as shown in Figure 4.7b. The PIB (Sigma Aldrich) handling layer was then applied to the 1 x 1 cm^2 substrate by dropcasting approximately 1.0 mL of a 1 wt% solution of PIB in hexane (99.9%, Sigma-Aldrich), and the solvent was allowed to evaporate naturally. Thermal release tape (Nitto, 80^{o}C type REVAPLHA) was then applied to a corner of the graphene FET/PIB stack on the PIB surface, serving as a tab for the PIB layer so that it can be peeled off. A polydimethylsiloxane (PDMS, Dow Chemical) stamp was then applied on top of the PIB and thermal release tape, as shown in Figure 4.7c. This stamp provides mechanical stability (preventing the graphene/PIB from rolling up on itself) while being easy to peel off, allowing for easy removal once transfer is completed.

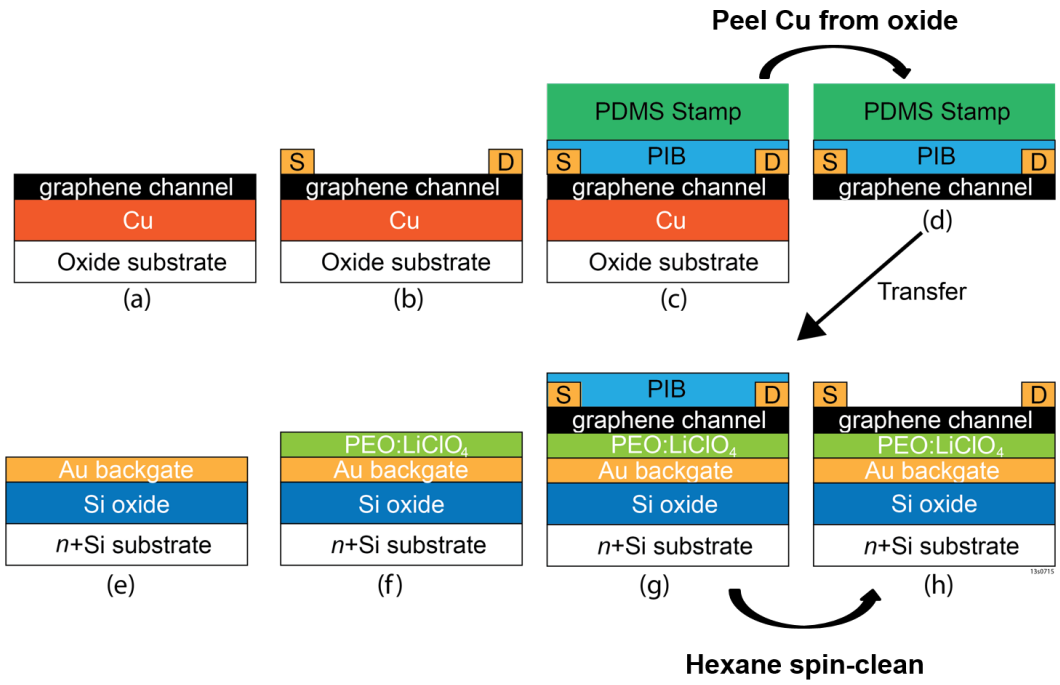

Figure 4.7. Process flow for fabricating an electrolyte-backgated graphene FET utilizing the semi-dry transfer method.

The SiO_2/Cu/graphene PDMS/PIB/FET stack was then soaked in water for 10 minutes to allow water to infiltrate the SiO_2/Cu interface. The Cu/Graphene PDMS/PIB/FET stack was then delaminated from the SiO_2 by grasping the thermal release tape and peeling the PDMS/PIB/FET stack off the SiO_2/Si substrate under water. The Cu/Graphene PDMS/PIB/FET was floated on the surface of the water and then transferred to the Cu etchant *via* a dummy wafer: the surface tension of the water prevents the graphene from adhering to the dummy wafer. This etchant bath, made up of a 10% solution of ammonium persulfate (APS, Microchem) in water completely etched the Cu film, leaving the back side of the graphene FETs exposed, as shown in Figure 4.7d. To remove the etch chemicals from the graphene

FET/PIB/PDMS stack, it was placed in a DI water bath for 1 minute, then transferred to a second, fresh DI water bath.

To transfer the FET/PIB/PDMS stack (illustrated in Figure 4.7d) to the PEO:$LiClO_4$-coated substrate (illustrated in Figure 4.7f), the PDMS/PIB/FET stack was brought into the argon-filled glovebox and into a hexane bath. The PDMS/PIB/FET stack floats on the hexane, allowing the PEO:$LiClO_4$-coated substrate to be submerged in the hexane, which was then used to pull the PDMS/PIB/FET stack out of the hexane. The entire PDMS/PIB/FET/PEO:$LiClO_4$/substrate stack, was then left to dry naturally in the argon environment. Following this drying step, with the graphene FET now adhered to the electrolyte-coated substrate, the PDMS stamp was gently peeled off to expose the PIB handling layer (this PDMS stamp can be re-used), as illustrated in Figure 4.7g. The device was then held at the surface of the hexane bath, PIB side down, to thin the PIB layer. Once the PIB was thinned enough that probes were able to contact through the PIB layer, the device was ready for testing. A schematic of the complete device, as well as an optical micrograph of a device are shown in Figure 4.8b. The polymer electrolyte is optically transparent, and therefore the patterned metal backgate is visible in the optical image.

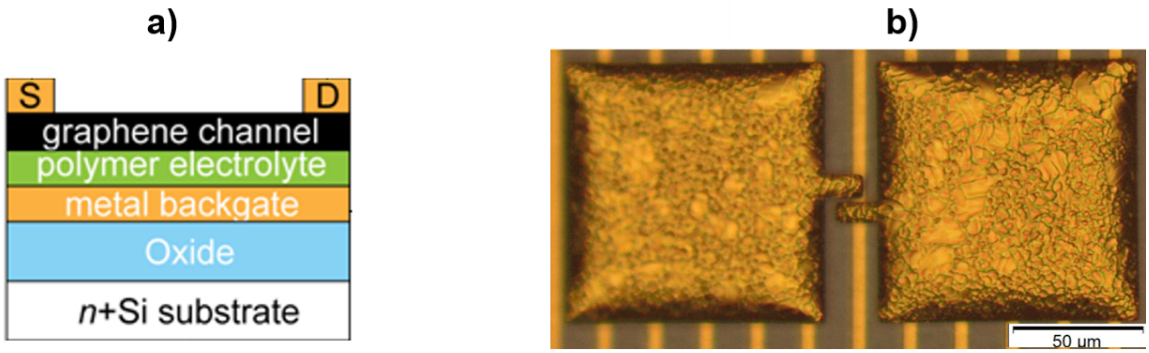

Figure 4.8. (a) A cross-sectional schematic of a fabricated electrolyte backgated graphene FET, and (b) a micrograph of the same. The graphene, as well as the electrolyte, are optically transparent, allowing the metal backgate and oxide substrate to be visible in (b).

4.3.5 Electrical Measurements

Electrical measurements were made in a dark, nitrogen filled Cascade Summit 11861 probe station, using an Agilent B1500a Semiconductor Parameter Analyzer. To make transistor characteristic measurements on the electrolyte backgated graphene FETs, first the probes must make electrical contact with the source, drain, and backgate contacts. Contact was made to the backgate electrolyte simply by using a probe to scrape the electrolyte from a portion of the backgate electrode not covered by graphene FETs. Contact to the source and drain was accomplished by using a small (typically a 0.5 μm radius) probe tip to gently scrape any remaining PIB from the contact surface. The probe was then used to gently contact each pad. Because there was no rigid substrate below the source and drain, only soft polymer, the contacts were prone to tearing, requiring that only very small adjustments be made when making contact to the source/drain pads. A bias was then applied between the source and drain to confirm that contact has been made, and that a conductive

graphene channel exists between the source and drain contacts.

4.4 Results and Discussion

4.4.1 Device Results

Transfer characteristics for the metal backgate device are shown in Figure 4.9, demonstrating that the gate is indeed modulating the channel. Not only do these transfer characteristics confirm that current is flowing from drain to source, but the characteristic "V-shape" indicates that transport is indeed occurring through the graphene, a semimetal, and not through a metal short in another portion of the device (for band diagrams demonstrating this ambipolar behavior, please see Appendix D). The unique shape of the transfer characteristics, as well as the low on/off ratio (typically between 3-10) for graphene devices results from the band structure of the graphene being a Dirac cone, where the bands intersect at the K point, rather than having a band gap. This results in ambipolar behavior, and a lack of a true "off" state that would be observed in a semiconductor FET. This result represents the first successful transfer of a fully fabricated graphene FET onto a SPE layer.

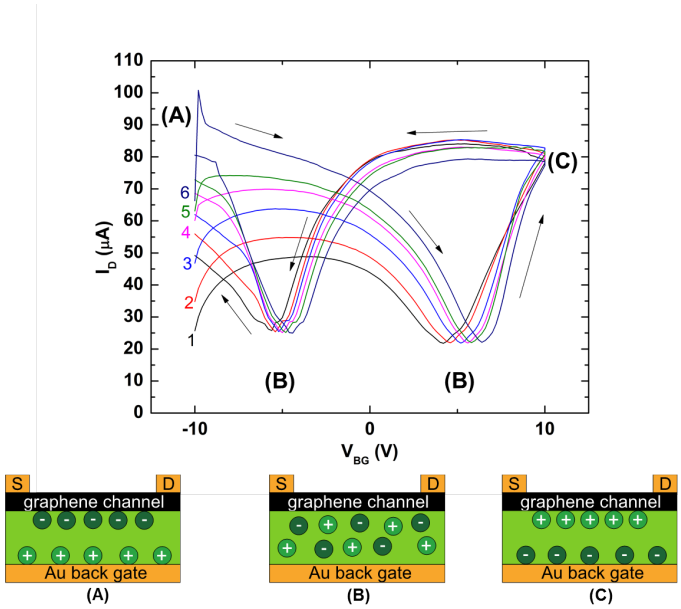

Figure 4.9. Top: Transfer characteristics of a graphene FET with electrolyte gating from underneath the channel. In this case, a Ti/Au backgate electrode was used. Sweep rate of 1.0 V/s, $V_{DS} = 0.1$ V. Measurements taken consecutively with no pause between measurements. Bottom: schematics of the ion locations at various gate biases indicating (a) hole conduction, (b) the Dirac point, (c) and electron conduction.

There are two distinct differences between the the transfer characteristics demonstrated here and the typical transfer characteristics of a non-electrolyte gated graphene FET.[98] The first is the two points of minimum conductivity (Dirac points), one for the forward sweep and one for the backward sweep, and second, measurement-to-measurement variation. The appearance of two Dirac points is due to the relatively slow ions that diffuse orders of magnitude slower than electrons/holes in graphene.[23] The 1.0 V/s sweep rate combined with the slow moving ions creates hysteresis, as the ions cannot keep up with the constantly changing field.[59] If the backgate sweep rate were slowed such that the ions could respond to the changing field within the

timescale of the measurement, the hysteresis would not be present.[59] The schematics in Figure 4.9 show the ion locations during device operation. When the gate bias is below the Dirac point, the ClO_4^- ions are close to the graphene channel, inducing holes in the channel, shown in Figure 4.9 as state A. As the backgate is swept, the ions become homogeneously distributed throughout the electrolyte, leading to a minimum in conductance, shown in Figure 4.9 as state B. It is the slow ion response that shifts this point away from near 0 V, the expected value for graphene. At biases above the Dirac point, Li^+ ions are drifted towards the graphene channel, inducing electrons, as illustrated in Figure 4.9, state C.

In addition to the double Dirac point in Figure 4.8, there exists a second deviation in I-V characteristics from a conventional graphene FET: increasing current in the hole conduction region (*i.e.* $V_{BG} < 5$ V for the forward sweep and $V_{BG} <$ -5 V for the reverse sweep) with each successive sweep. This increase in current in the hole conduction region results from the method by which each successive data run is collected. The backgate potential is first set to -10 V, then swept to +10 V, then back to -10 V. Because there is no "reset" (*i.e.*, time where the terminals of the FET are grounded to completely discharge the EDL) between consecutive runs, the EDL that provides holes to the channel will still be established, raising the "starting" current level with each successive measurement. Such variation could be removed if there were a "reset" period between each consecutive sweep, or by starting the measurement at zero.

The on/off ratio of the measured device is low ($\sim$4), even for graphene FETs, for which the on/off ratio rarely exceeds 10, due to the semimetallic nature of graphene.[13, 99, 100] The current at the Dirac point is heavily influenced by the intrinsic charge carrier density[101], which increases with defects or adsorbates on the graphene, so finding a process that allows for graphene with fewer defects or does not involve processes that create adsorbates (such as the metal etch step) would

increase the on/off ratio by decreasing the magnitude of the off current.

To better understand the operation of this electrolyte backgate structure, and its relationship to changing sweep rates, ion transport is modeled using a simplified device structure in COMSOL Multiphysics. This structure is a parallel plate capacitor structure (Figure 4.10) with PEO:$LiClO_4$ serving as the dielectric, and the graphene implemented as a equipotential boundary conditions. The charge distribution due to ions within the electrolyte is described in Equation 4.1:

$$\rho = F(c_+ - c_-) \tag{4.1}$$

Where the charge distribution (ρ) is described in terms of the Faraday constant (F), and the concentration of Li^+ and ClO_4^- (c_+ and c_- respectively). ρ is related to the potential within the electrolyte (ϕ) through the electrolyte permittivity (ϵ) using Poisson's equation (Equation 4.2).

$$\nabla \cdot (-\epsilon \nabla \phi) = \rho \tag{4.2}$$

The Nernst-Planck Equations (collectively Equations 4.3 and 4.4) are used to model the ion transport.

$$\frac{\partial c_k}{\partial t} + \nabla \cdot \boldsymbol{j}_k = s_k \tag{4.3}$$

$$\boldsymbol{j}_k = \boldsymbol{u} c_k + (-1)^{k-1} \mu_k \boldsymbol{E} c_k - D_k \nabla c_k \tag{4.4}$$

These equations relate the time derivative of the ion concentration (c_k), and the ion flux ($\mathbf{j_k}$) to s_k, the source term, which accounts for addition/subtraction of ions. The value of s_k is set to zero for all simulations, which is equivalent to the assumption that all of the salt is dissociated into its corresponding cations and anions. The ion flux is a contribution of three terms: 1) fluid convection, 2) transport in response to the applied field, and 3) transport due to a concentration gradient. The first term

containing the fluid velocity ($\mathbf{u}$) is set to zero because the electrolyte itself does not flow. The ion mobilities, μ_k, appearing in the second term are 2.4 x 10^{-11} cm^2/Vs for Li^+ and 7.2 x 10^{-11} cm^2/Vs for ClO_4. These mobility values are calculated from ionic conductivity, σ, for PEO:$LiClO_4$ in a parallel plate capacitor geometry using Equation 4.5[26, 102]

$$\sigma = F^2(z_+^2\mu_+c_+ + z_-^2\mu_-c_-) \tag{4.5}$$

where F is Faraday's constant, μ_+ is the mobility of Li^+, μ_- is the mobility ClO_4^-, and $z_+ = +1$ for Li^+ and $z_- =$ -1 are the charged states of the ions.

From molecular simulations of $(PEO)_{15}$:$LiClO_4$, it is known that the mobility of the anion in PEO is approximately three times larger than the cation.[103] Therefore, the mobility of ClO_4^- is set to a value three times larger than Li^+. The applied electric field, $\mathbf{E}$, varies throughout the simulation as the gate voltage is swept. The diffusion coefficients, $\mathbf{D_k}$, are calculated as 6 x 10^{-13} cm^2/s for Li^+ and 2 x 10^{-12} cm^2/s for ClO_4^- using the Nernst-Einstein equation (Equation 4.6):

$$D_i = \frac{\mu_i k_b T}{q} \tag{4.6}$$

where k_b is Boltzmann's constant, and q, is the elementary charge. The initial concentration of ions in the electrolyte is set to 1115 mol/m^3 (equal to a 20:1 ether oxygen:Li ratio for PEO:$LiClO_4$).

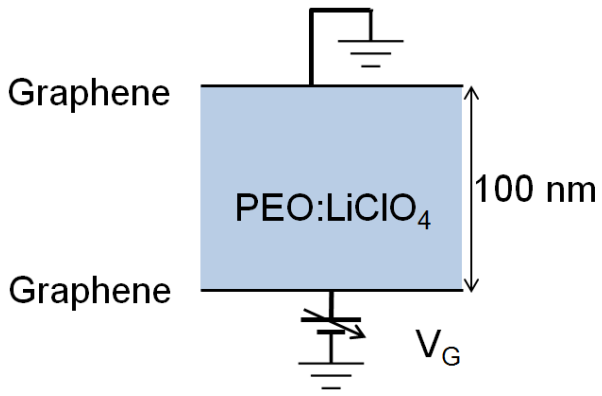

Figure 4.10. Parallel plate capacitor model structure used to simulate the electrolyte backgate structure in COMSOL. Graphene is implemented as a boundary condition, while the 100 nm thick PEO:$LiClO_4$ is defined as a dielectric with mobile ions.

In this simulation, the applied bias is swept from -0.15 to 0.15 V, then back to -0.15 V, meaning that the initial field across the 100 nm thick capacitor is 15 kV/cm. This is a smaller field than the initial 100 kV/cm (10 V over 1 μm) applied across the electrolyte in Figure 4.8, so in this simulation, ions will tend to react slower than the device it is modeling. The sweep rates simulated are 1.0 V/s (the rate used in Figure 4.8) and 0.01 V/s. The two order of magnitude difference in sweep rate allows us to discern the sweep rate's effect on hysteresis in the transfer characteristics.

By coupling these equations and applying them to a time-dependent simulation where the bias is swept, the ion concentration can be monitored as a function of time, location within the film, and applied bias. By monitoring these characteristics as the ions move from a homogeneous distribution of ions at t = 0 in response to the constantly changing an applied field, we can further understand the dynamics of the ions in the backgated graphene FET.

The charge density of the ions at the surface of the graphene boundary in the

COMSOL simulations is plotted in Figure 4.11 as a function of applied bias. This charge density vs applied field data shows the surface charge density induced by the ions at the interface between electrolyte and the top electrode vs. applied bias for both the forward and backward sweep. This is analogous to the transfer characteristics shown in Figure 4.8, because the surface charge density at the electrolyte/channel interface is measured experimentally by measuring the drain current in a graphene FET.

Simulations of a "fast" sweep rate of 1.0 V/s (the same sweep rate used in Figure 4.8) recreate the hysteresis that is evident in the transfer characteristics of the graphene FETs in this work, indicating that the hysteresis is indeed caused by the sweep rate out pacing the comparatively slow ionic motion in the electrolyte. Consistent with reports by Xu *et al.*, the hysteresis can be nearly eliminated by decreasing the sweep rate.[21] In the case of the model, slowing the sweep rate 2 orders of magnitude to 0.01 V/s causes the hysteresis loop to close completely, indicating that if the same transfer characteristics were taken on the FET devices, at a slower sweep rate, that the hysteresis would be decreased.

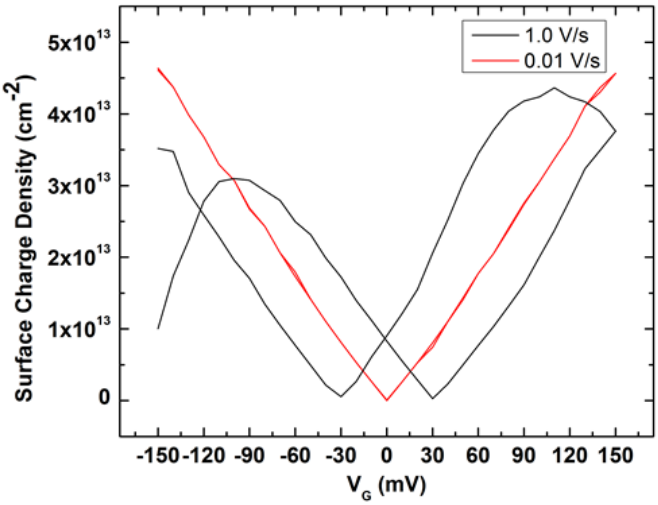

Figure 4.11. COMSOL simulation of a parallel plate capacitor with PEO:$LiClO_4$ as a dielectric, demonstrating hysteresis at higher sweep rates and a lack of hysteresis at a lower sweep rate.

In addition to a patterned metal back contact, FETs with a patterned graphene electrode as the backgate are also tested. Due to the optical transparency of the graphene backgate contact, it is not possible to locate the backgate contact in relation to the channel, which prevents us from selecting devices with proper backgate contact alignment, shown schematically in Figure 4.12. For devices with large (> 10 μm) backgate misalignment, higher backgate voltages are required, because the potential drop in the bulk of the electrolyte in such devices is no longer negligible in comparison to the voltage drop across the EDLs.

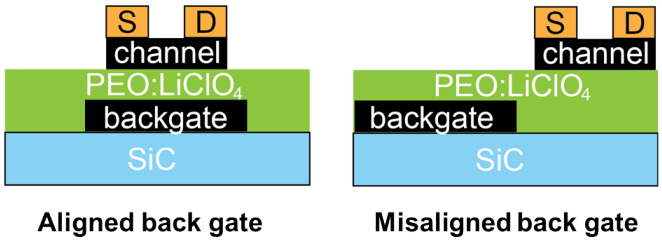

Figure 4.12. Schematic illustrating how backgate misalignment can increase the distance from the backgate electrode to the channel of an electrolyte backgated FET.

The transfer characteristics for the graphene backgate electrode device (shown in Figure 4.13) are similar to the Ti/Au backgate electrode device (though on a larger voltage scale due to the previously mentioned backgate misalignment), with the same hysteresis due to the slow ion response to the changing applied bias, and a on/off ratio again near four. However, the run-to-run variation takes a different form for this device. In general, the maximum current in the electron and hole branches seem to change inversely to one another, perhaps due to the voltage drop across the bulk of the electrolyte causing the initial applied field to be much lower than if the gate were properly aligned, meaning that the EDL will take longer to form and therefore require more time to move the ions towards/away from the graphene surface. For the first run, the large negative applied bias will tend to make the hole branch current higher, but for the later runs, there is more time *continuously* spent at positive bias. This happens because the sweep goes from -V to +V and back to -V, and so the middle

50% of the run is spent in positive bias while only the beginning and end 25% are in the negative bias. Because there is more time spent continuously at positive bias, and because the ions respond slowly, there will be a greater effect on electron conduction in graphene over hole conduction, thus enhancing conduction in the electron branch and suppressing it in the hole branch.

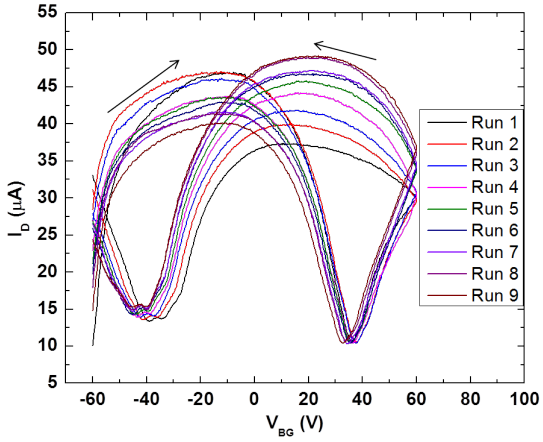

Figure 4.13. Transfer characteristics of a graphene FET with electrolyte gating from underneath the channel. In this case, a graphene backgate electrode was used. Sweep rate of 1.0 V/s, $V_{DS} = 0.1$ V.

For both the Ti/Au and graphene backgate electrode devices, the yield of these processes was quite low: less than 5% of tested devices were found to have channels that were electrically conductive from source to drain. It is possible that the device is failing due to some mechanical process, either from the source/drain contacts delaminating from the graphene channel, the APS used in the Cu etch bath attacking the grain boundaries of the graphene, or the mechanical stresses involved with the

transfer process fracturing the graphene.

It should be noted that all the devices with current flow from the source to the drain did not have an isolation etch performed, therefore a well-defined and isolated channel of graphene does not exist between the source and drain contacts. This means that the current path could be through any number of pathways that do not include the channel area. We have tried to define the channels *via* the same oxygen plasma etch used to define the graphene backgate electrode; however all subsequent transfers with the defined channel failed to yield a device that remains electrically conductive between source and drain. This result suggests that the density of fractures and defects is so high that at least one or more defects exist within all the channels following the isolation etch, thereby making all the devices non-conductive. Microscope imaging of the finished devices shows that following transfer, many metal features on the graphene surface have significantly shifted position and angle (as shown by the lack of alignment of the letters in Figure 4.14). This is likely a result of stress during the transfer process, perhaps during the etch step, a drying step, or when the device is placed on the electrolyte.

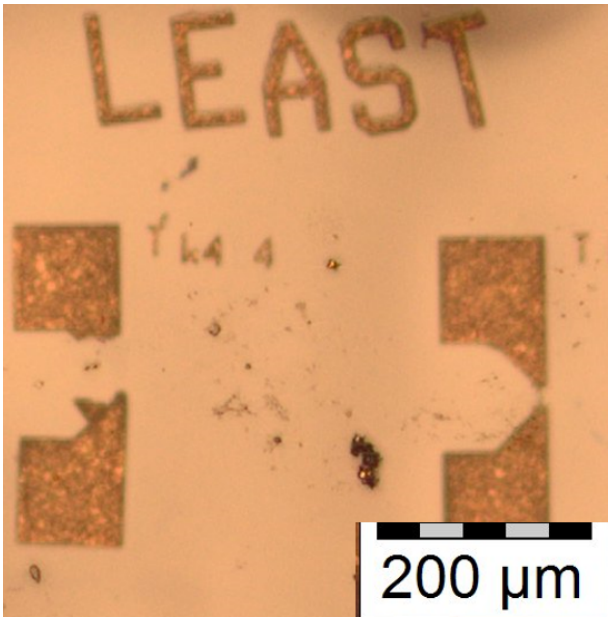

Figure 4.14. Image of fabricated electrolyte backgated graphene FETs showing the misalignment, and in some cases fracture of the contacts after the transfer. Note that the letters that spell "LEAST" have been rotated during the transfer, indicating that significant deformation happens during transfer.

To improve the yield of the etch-defined channel devices, an additional 20 nm thick handling layer of SiO_2 is deposited *via* e-beam evaporation. Figure 4.15 shows the result of the SiO_2-assisted semi-dry transfer method. The large fractures clearly show that the stresses imparted on the device during transfer are far greater than the strength of the SiO_2 thin-film. As a result, no functioning devices were found. However, it is possible that much smaller devices, with a width and length that are smaller than a single grain of CVD grown graphene (up to 0.5 mm in size for graphene grown with the goal of large grains[104]) could be more resistant to the fracturing.

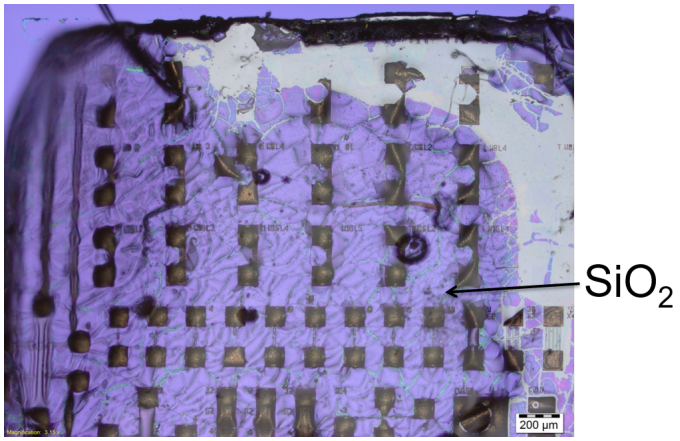

Figure 4.15. Image of electrolyte backgated graphene FET transferred using the SiO_2-assisted transfer method.

A method for transferring devices with well-defined, isolated channels, especially devices with a gate dielectric and gate contact in addition to the source/drain contacts (which would be required for a NAND memory configuration), would open more measurement possibilities. For example, with a top and backgate, field effect carrier density and mobility could be measured. TLM patterns could be used to measure contact resistance as a function of backgate bias, which would let us investigate source/drain contacts gated with an electrolyte to improve contact resistance to 2D materials.

4.5 Conclusions

A transfer method for transferring fabricated graphene devices onto a soft polymer electrolyte substrate is shown, demonstrating for the first time an electrolyte backgated graphene FET structure. Devices using Au as a backgate contact shown an on/off ratio of >4, indicating that the conductivity of the graphene channel is be-

ing modulated using an EDL. Transfer characteristics of both the Au and graphene backgate contact devices were dominated by hysteresis, a consequence of the sweep rate being too fast for the ions to respond to the changes in applied field. This is confirmed by COMSOL Multiphysics simulations that indicate that if the sweep rate were slowed, the hysteresis loop would collapse, as shown by Xu *et al.*.[21]

While this is the first demonstration of a transferred 2D FET, the device yield was low (∼5%), and when the channels were isolated *via* oxygen plasma etch, the yield decreased to zero. Attempts to improve yield using an SiO_2 layer as an additional handling layer were unsuccessful due to the excessive cracking of the SiO_2 layer. To improve the yield of such a transfer process, further exploration of different handling layers or techniques is required. A more rigid handling layer could allow for less flexing in the channel (to prevent graphene cracking), or a gentler delamination process could possibly improve yield. Because the devices measured in this study do not have etch-defined channels, current can flow through any number of paths, including the channel as well as parallel leakage paths through nearby field graphene. To investigate individual isolated devices, a process must be developed to transfer devices with etch-defined channels.

This work represents a first step towards building the device stack needed for an ion-based memory. If the yield can be improved for devices with etch-defined channels, and a topgate stack added, new devices could be explored, such as stacked 2D memory, devices with doped contacts, and dual electrolyte gated FETs.

CHAPTER 5

TWO-TERMINAL FERROELECTRIC RESISTIVE PROCESSING UNIT[1]

5.1 Motivation

5.1.1 Deep Learning

Deep learning, a class of machine learning algorithms, as discussed in an article by the New York Times[105], has been used by Google to drastically improve the functionality of Google Translate, decreasing the translation time of a 10 word sentence from 10 seconds to 0.2 seconds, and improving the BLEU (bilingual evaluation understudy, a metric for translation accuracy) scores by over 1.0 on average, a large increase in accuracy.[105] A deep neural network attempts to mimic the way the human brain makes decisions by using a cascaded configuration of multiple independent inputs to come to a conclusion. For any set of inputs, the output of a deep neural network is a function of the connection strength (weights) between each element of a layer to each of the elements in the following layer. A deep neural network is trained by repeatedly inputting known data, such as many images that are known to either contain a cat or not. The output of the deep neural network is then compared to the true answer, that is does the deep neural network determine there is a cat in the image versus is there actually a cat in the image. On an incorrect answer (*e.g.* it identifies a picture of a dog as having a cat), the weights in the neural network are adjusted in a systematic fashion. Adjusting the weights on incorrect answers, the

[1]This work was collaborative with graduate students Crostobal Alessandri and Pratyush Pandey. Devices made by P. Pandy and measurements made by C. Alessandri are acknowledged in the text or figures.

neural network can, in effect, learn (in this example, to identify if a picture has a cat in it). Deep learning improves the accuracy of a host of applications, in particular language translation and image recognition, but comes with a cost. The neural network must be trained, which costs both energy and computing time.

5.1.2 Proposed Resistive Processing Unit

In order to both improve the speed and reduce power consumption during training of a neural network, IBM researchers Gokmen and Vlasov have proposed a set of requirements for a resistive processing unit (RPU) using a network of 2-terminal variable resistors which can be electrically programmed using a bipolar pulse train.[6] Typically the time to train a neural network increases as the square of the number of inputs. Using the proposed RPU, a deep neural network can be trained in a time proportional to the training of a single node in the array, a significant improvement, especially for systems that require a large number of inputs.

The RPU Gokmen and Vlasov propose should have an area of 0.04 μm^2, with 1000 resistance levels, with an average device resistance of 24 MΩ with 100 kΩ of separation between levels, with a minimum resistance of 14 MΩ and maximum of 112 MΩ.[6]. The RPU is programmed by application of voltage pulses with a pulse duration of 1 ns at $\pm$1 V, meaning that changing the state of the device must be a fast process. In addition to this low switching voltage, the resistance state can change by at maximum 10 kΩ when a pulse of $\pm$0.5 V is applied.

In this section a RPU is proposed based on the partial switching of a ferroelectric (FE). A first embodiment of the device consists of a semiconducting channel with a FE deposited on the surface. Source contact is made to one end of the channel, while the drain not only contacts the channel, but also wraps around the FE to act as a field control gate to the FE. Several possible designs are shown in Figure 5.1. The planar configuration (Figure 5.1a) has the drain wrapping around only the sides, meaning

that most of the modulation will happen at the edges of the channel. The horizontal configuration, shown in Figure 5.1b, consists of a 2D channel with the drain wrapping around the top surface of the channel. The vertical configuration shown in Figure 5.1c has a pillar of semiconductor serving as the channel, with the drain wrapping around all sides of the channel. In this FE RPU (FeRPU) architecture instead of the FE polarization being controlled by a separate gate terminal, the overlapping drain contact creates an electric field across the FE, which promotes domain switching. Sensing of the state of the FE is achieved by measuring the conductance of the channel. The asymmetrical layout of the FeRPU promotes the FE domains nearer to the source to switch first, as the field across those domains will be higher than across the domains toward the drain contact. This layout is intended to promote partial switching, as even in a FE where every domain has the same coercive (switching) voltage, the domains near the source will switch first.

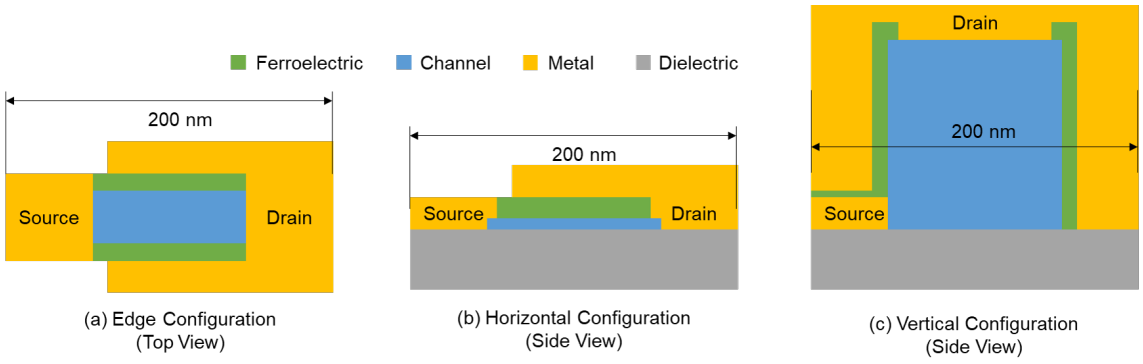

Figure 5.1. Schematic showing three proposed FeRPU device layouts, the planar configuration (left) where the drain wraps around the channel, in the plane of the channel, horizontal configuration (center) showing the drain wrapping around above the channel, and the vertical configuration (right) where the drain wraps around the vertical channel.

5.1.3 FE RPU Programming

Programming a RPU in a crossbar array (Figure 5.2) is accomplished by applying half of the amplitude of a programming pulse (*i.e.*, a 1 ns, 1 V pulse) to the drain (bit line), while the other half of the amplitude of the pulse is inputted through the source (word line). This form of device operation can allow for implementation in a crossbar setup, where a device will not be programmed unless a pulse is applied to a given bit and word line. Such operation is key for reducing the time required to train a given neural net implementing this device architecture. To read the device, a small bias (less than $\frac{1}{2}$ of the 1 V programming pulse) is applied between the drain and source, with the current through the device serving as the output to be read.

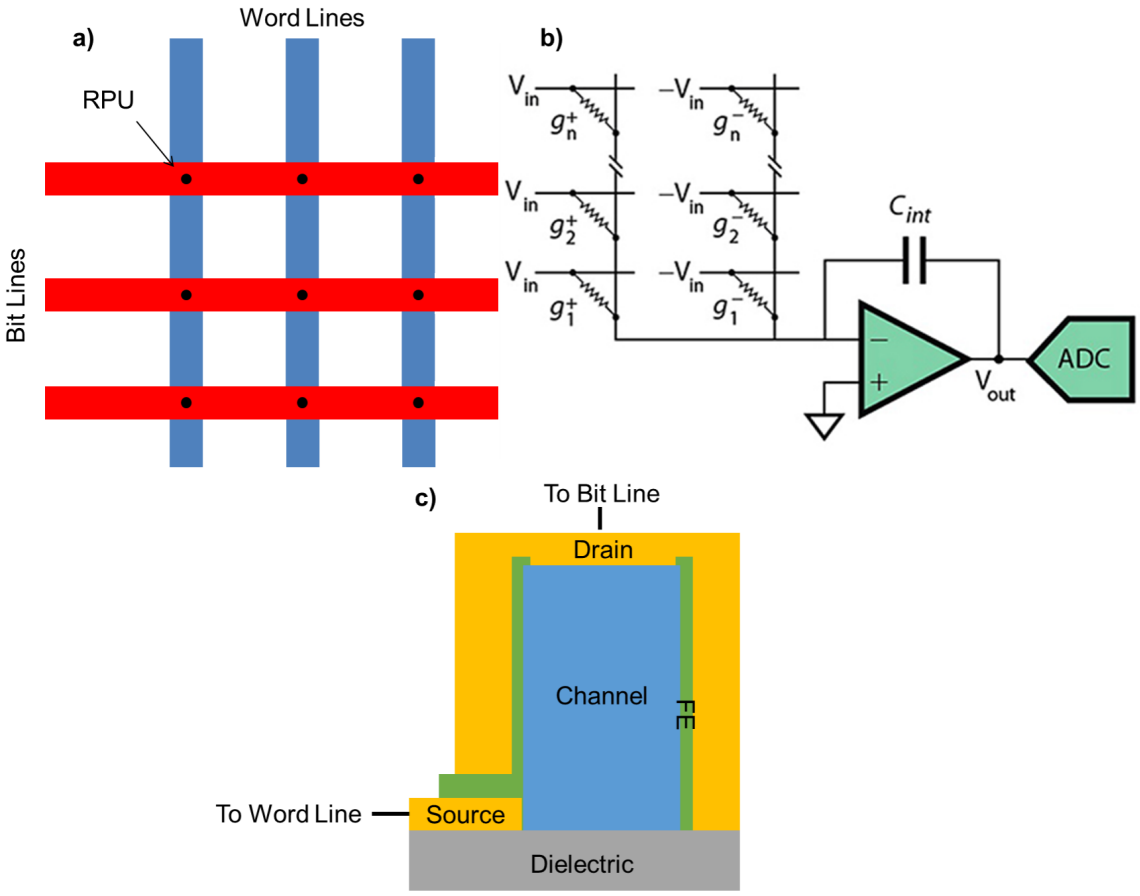

Figure 5.2. (a) Schematic of a crossbar geometry with RPUs implemented at the intersections of bit and word lines. (b) Circuit by Gokmen and Vlasov[6] showing one row (or column) operated in both the forward and reverse directions, with an amplifier to integrate the differential current and the required analog to digital converter. (c) Schematic showing how a proposed vertical FeRPU can be integrated into the crossbar structure, with the g_n being the conductance of the FeRPU channel.

5.1.4 Models of Partial Polarization in Ferroelectrics

In order to provide the greatest number of RPU states, the number of switchable domains in the FE must be maximized. It has been shown that FE film thickness is a major determining factor for domain size[32], the thinner the film, the smaller

the domain. Smaller domain size should correlate with more states available with the RPU. This means that one key for the realization of a RPU is determining the partial polarization behavior of a FE that can scale down as thin as possible. In this work, we[2] first use a $PbZrTiO_3$ (PZT) capacitor to establish that our test setup can be used to partially switch a well studied FE.[106, 37] We[3] then examined the partial switching of a HfZrO (HZO) capacitor. HZO is a FE that has been shown to scale down to < 10 nm thickness while still retaining its FE properties.[107]

A model for FE switching is given by Kolmogorov-Avrami-Ishibashi (KAI)[108] for a single FE domain in the film (*i.e.* the entire FE will switch at the same voltage, beginning from a single location), where the partial FE switching results from a wall of FE unit cells switching within the film, which halts when the bias is removed.[109–111] The KAI model is sufficient for a FE that have relatively few domains[109], but that breaks down for thin FEs.[40] A better model for thin FEs is the nucleation limited switching (NLS) model, which assumes that instead of a single domain, the film is made up of many domains, with a distribution of switching times.[112] In this work, we propose a modification to the NLS model (hereafter referred to as the modified NLS model) This model, chiefly developed by C. Alessandri, has been employed which accounts for the amplitude dependence of the applied voltage.

In the modified NLS model, we assume a Lorentzian distribution of activation voltages $F(V_c)$ (Equation 5.1) with a maximum of $\frac{1}{\pi\gamma}$ at the mean value V_m, and scale parameter defining the half width at half maximum, $\sqrt{2}\gamma$.

$$F(V_c) = \frac{\gamma/\pi}{(V_c - V_m)^2 + \gamma^2} \tag{5.1}$$

[2]This study was performed in collaboration with doctoral student C. Alessandri.

[3]This study was performed in collaboration with doctoral students C. Alessandri and P. Pandy.

The bias dependence of switching time is taken to be

$$t_o = \tau_1 e^{(V_c/V_{ap})^{\alpha}} + \tau_o \tag{5.2}$$

where the switching time, t_0, depends on the applied pulse amplitude (V_{ap}), minimum switching time (τ_1), exponent fitting parameter (α), and offset (τ_0).

The full polarization vs time model

$$P(t) = P_{max} \int_o^{\infty} \left(1 - e^{-\left(\frac{t-T_o}{t_o}\right)^{\beta}}\right) F(V_c) \mathrm{d}V_c \tag{5.3}$$

combines Equations 5.1 and 5.2 with the maximum change in polarization (P_{max}), an additional temporal fitting parameter (T_0), pulse width (t) as well as the dimensionality (β). The dimensionality is a measure of how the domain switching propagates, where $\beta = 1$ describes the domain switching in a plane, $\beta = 2$ is switching radiating outward from a column, and $\beta = 3$ describes propagation from a point. Values of $\beta < 1$ indicate that there is a barrier to switching in domain propagation, likely from domain walls. The fitting parameter T_0 is required because the applied pulses are not being rectangular, due to the 20 ns minimum rise/fall time of the Keithley 4200A-SCS Pulse Measurement Unit (PMU), Figure 5.3.

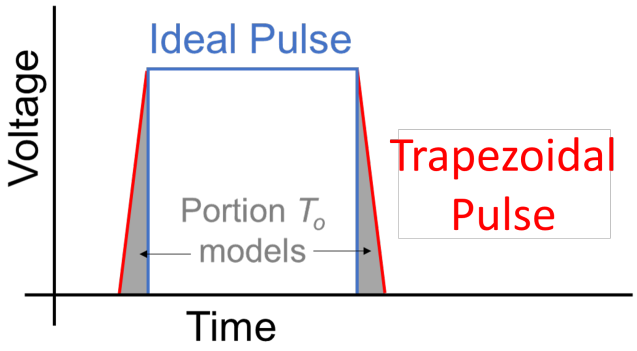

Figure 5.3. Pulse shape of an ideal rectangular voltage pulse (blue) vs trapezoidal output of the Keithley 4200-SCS PMU showing the trapezoidal shape due to slew rate limitations. T_0 fitting parameter is a fitting parameter that accounts for the polarization change that occurs due to the non-ideal portions of the pulse, highlighted in gray.

5.2 Partial Polarization Experiments

In order to understand the measurement considerations of the proposed FeRPU, first we must understand how the Keithley 4200-SCS can be used to switch FEs, using PZT capacitor as a test system. Next, we must determine how to partially switch HZO. As a FE, HZO is more suitable to FeRPU implementation than PZT, as it is FE at thicknesses < 10 nm.[107] Finally, fitting the partial switching (*i.e.* switching to polarizations between the $-P$ and $+P$, the fully switched states) of HZO is vital to understand and be able to predict the partial switching of HZO.

5.2.1 FE Capacitors

A TiN/$HfZrO_3$ (HZO)/TiN capacitor structure was grown by Golnaz Karbasian at University of California, Berkeley using an ALD process, followed by a spike anneal, to induce the FE orthorhombic phase in the HZO. Next, the TiN/HZO/TiN was

further patterned to create a series of circular capacitor structures with diameter of 100, 125, 150 and 175 μm. The first processing step removed the top TiN layer to expose the HZO using piranha etch (DI:H_2O_2 (30%):NH_4OH (29%) at 55 ^{o}C) for 8 minutes. To protect the dielectric in the smaller capacitor structures, a PMMA/MMA bilayer (MicroChem, PMMA C2 resist, 130 nm thickness and MMA(8.5) MAA EL 9, 320 nm thick) exposed using an electron beam to protect circles of diameter of 60, 90, 120 and 150 μm. The HZO that was not protected by the resist was then etched using an Oxford inductively coupled plasma reactive ion etcher (ICP-RIE) with a 6 minute CHF_3 etch (15 mTorr, 30 sccm CHF_3 flow rate, 200 W, 497 V DC bias) exposing the back TiN. Another e-beam lithography step was performed to define windows to the top of the HZO and to the bottom TiN, then Pd was evaporated and lift-off performed, leaving capacitor structures with an HZO dielectric. This process at Notre Dame was performed by doctoral student Pratyush Pandey.

5.2.2 Measurement of Polarization-Voltage Characteristics

Electrical characterization of packaged PZT capacitors (Radiant Technologies, 400 μm^2, 2 capacitors per package) were tested using a Keithley 4200-SCS Semiconductor Parameter Analyzer attached to a board provided with the capacitors (Radiant Technologies, RT040903) which allow for coaxial cables to be used to connect to the capacitor. HZO-based capacitors were contacted using a Cascade Microtech Model 12100 Probe Station, and measured with the same Keithley 4200-SCS Semiconductor Parameter Analyzer as the PZT capacitor. All tests of the HZO-based capacitors were performed by wafer probing in a dark, nitrogen-filled Cascade Microtech Summit 1200 probe station.

For FEs, one valuable plot is the polarization vs applied electric field (P-E). This data was acquired by applying a triangle waveform from 0 to +V to V to 0 V (shown Figure 5.4), while recording the current. The capacitive contribution to the current is

related to the triangle wave slew rate, so 10 V/s was chosen to allow for the capacitive current to be easily measured using this test setup. The P-E data was obtained by integrating the switching current from the data taken from this I-V measurement (see Chapter 1 for more details on acquiring P-E data).

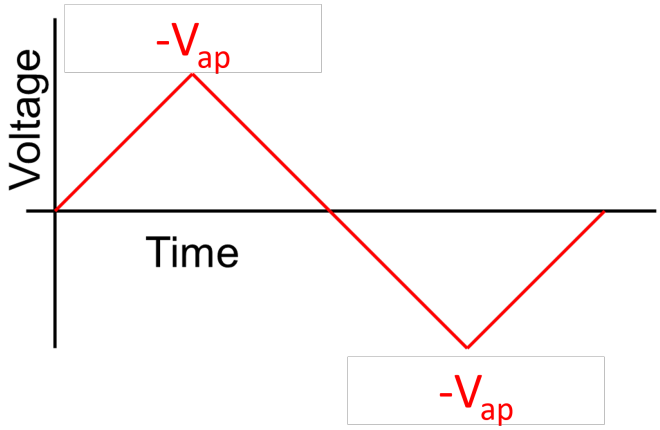

Figure 5.4. Triangle wave used to obtain the polarization vs applied electric field. Slew rate of 10.0 V/s chosen for all triangle waves in this work.

FEs were switched in this work using pulsed voltages. This study focused on pulse-width modulated signals, as the varying number of 50 ns pulses applied to partially switch the FE were found to cause HZO devices to fail during testing, likely the many fast changes in applied field caused punch-through, causing the device to short through the FE with a resistance on the order of 100 Ω. Pulsed width modulation was accomplished by using a pulse measurement unit (PMU) to create voltage pulses of varying time periods, with which the FE was switched.

In order to acquire the data required to ensure the FE switching component can be

isolated from the I-V data collected, the pulse sequence shown in Figure 5.5 was used. This pulse sequence consists of two negative triangle pulses to reset the device to its $-P$ polarization state, the second pulse provides a more reproducible reset condition. The positive, pulse width modulated, pulse was then applied, partially switching the FE. Two negative triangle pulses are then applied, the first switches the device from its partially polarized state to the $-P$ polarization. The I-V measurement of this first step has the capacitive, resistive and FE contributions to the current. The second triangle wave takes data of just the resistive and capacitive contributions to I-V since the polarization has been reset in the first triangle pulse. By subtracting the I-V of the second triangle pulse from the first, only the FE contribution to the current remains, and from this, the partial polarization in $\mathrm{C/cm^2}$ by integrating the current difference over a single cycle.

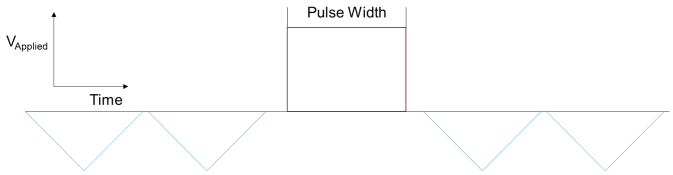

Figure 5.5. The pulse sequence used for pulse width modulated partial switching of FEs. The first two triangle waves set the FE to the $-P$ polarization. The positive pulse (of varying width) then partially switches the polarization to some value greater than $-P$. The third triangle wave then switches the FE back to $-P$, with the forth triangle wave providing data to isolate the capacitive and resistive current from the switching current. Note: the amplitude of the triangle pulses is greater than the coercive voltage of the FE.

5.3 Measurements of Partial Polarization of PZT

5.3.1 PZT Partial Switching

To confirm that partially switching a FE using the voltage pulses generated by our test setup, we first attempted to partially switch, PZT, for which partial switching data already exists.[112, 109, 111] First, the I-V response to a triangle wave (3000 V/s slew rate, 5 V magnitude, shown Figure 5.6) was taken to ensure that the PZT is well-behaved (*i.e.*, does not require a "wake-up" step before the device response stabilizes), locate the coercive voltage, and acquire the data to obtain the P-E curve (Figure 5.7). From the I-V data in Figure 5.6, it is apparent that the PZT fully switches by the time that ± 3.5 V is applied to the PZT capacitor. This sets 3.5 V as the upper bound for the amplitude of the partial switching voltage, as above this voltage, switching times on the order of 1 ns, too fast for the test setup described above to measure.

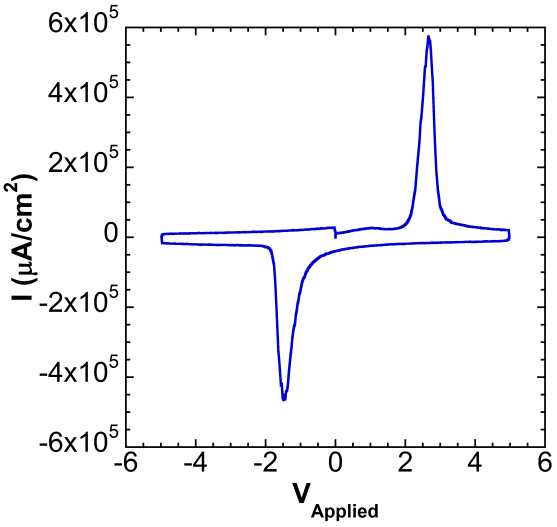

Figure 5.6. I-V of a PZT FE capacitor (area 400 μm^2 resulting from a 5 V triangle wave with a 3000 V/s sweep rate, showing the switching current visible at approximately $\pm$2 V. Measurements by C. Alessandri and E. Kinder.

The P-E diagram (Figure 5.7) indicates that, when fully switched, the remnant polarization of the FE is near $\pm$30 μC/cm^2. The PZT capacitor was switched many ($>$ 500) times without failing (*i.e.* becoming a short), indicating that a PZT-based device could survive at least that many programming steps.

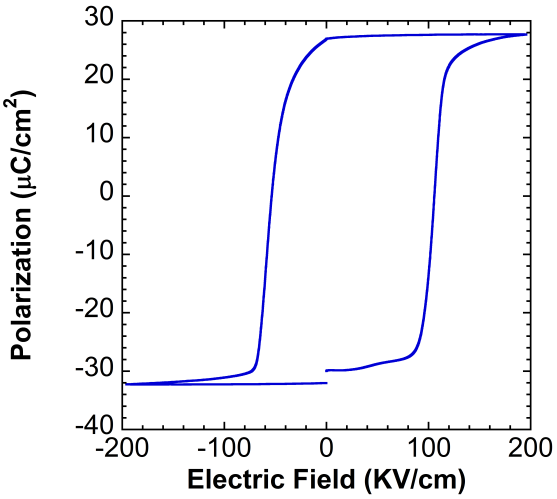

Figure 5.7. P-E calculated from integrating the switching current of the PZT capacitor in Figure 5.6.

Using the pulsed bias sequence discussed in Figure 5.5, the PZT capacitor was placed into a partially switched state. Figure 5.8 shows the switching current resulting from the PZT capacitor switching from the partially switched state to the $-P$ state. As the pulse width increases, the amplitude and width of the polarization current peak increases, indicating that the longer the voltage pulse, the more the FE is switched, until the fully switched state is reached.

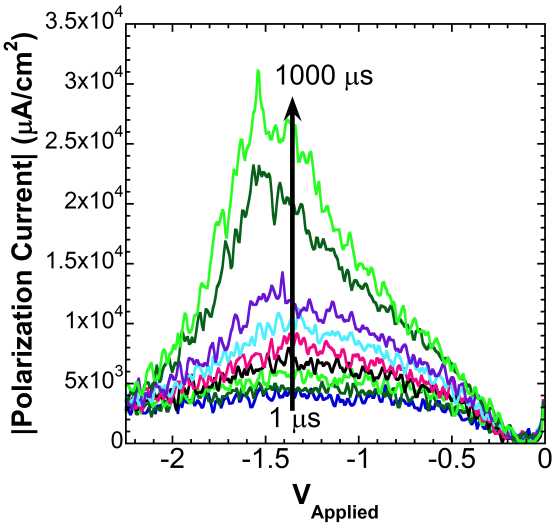

Figure 5.8. I-V curve of a PZT capacitor switching from a partially switched state to the $-P$ polarization state. The partially switched state has been obtained using a 4 V pulse of varying width.

By integrating the switching current in Figure 5.8, we are able to determine by how much the polarization was changed *via* the pulsed bias, shown in the P-E plot, see Figure 5.9. This change in polarization is measured from the $-P$ state, meaning that if a pulse is applied long enough such that the entire film changes to the $+P$ state, the total change in polarization that is measured will be $2P$.

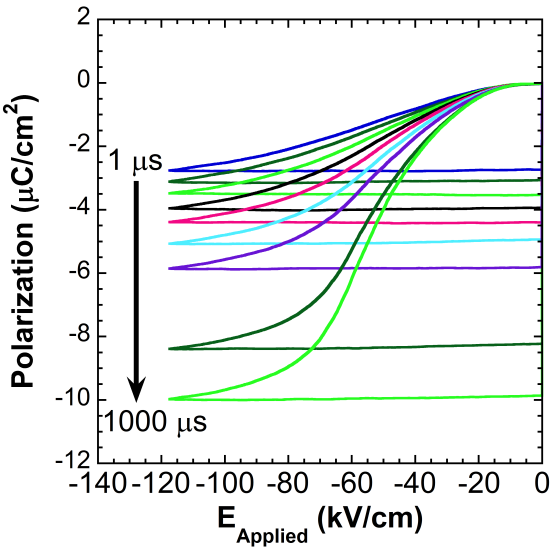

Figure 5.9. Polarization vs E curve of a PZT capacitor switched using a variable width 4 V pulse. The hysteresis between the forward and backward sweeps indicates the change in polarization from the applied pulses.

This brief study of partial switching of a commercially-available PZT capacitor provided insight into the ability of the Keithley 4200A-SCS to partially switch an electrolyte, as well as serving as a testbed for partial switching techniques. These techniques were then applied to HZO-based devices. This is an important step because HZO has yet to be studied elsewhere for a partial-switching application.

5.3.2 HZO Partial Switching

Following the confirmation that pulse-width modulated partial switching strategy works, using PZT as a model, FE capacitors with HZO as a dielectric were then measured. The first few 3.5 V triangle wave measurements show that there are four current peaks in the I-V (Figure 5.10), two for the positive branch and two for the negative. By comparison, PZT only had one current peak per branch, indicating

that there was one bias about which the FE switched. The presence of multiple peaks when switching HZO has been previously observed by Schenk *et al.*, and was determined to result from the distribution of coercive fields (*i.e.* different FE domains have different coercive fields).[113] This distribution is thought to result from a non-uniform distribution of defects, such as oxygen vacancies, throughout the film.[113] These vacancies tend to reduce the coercive field for the domain in which they reside, so the low-field peak is due to the highly defective domains switching, while the higher-field peak is the switching of the less defective domains.[113]

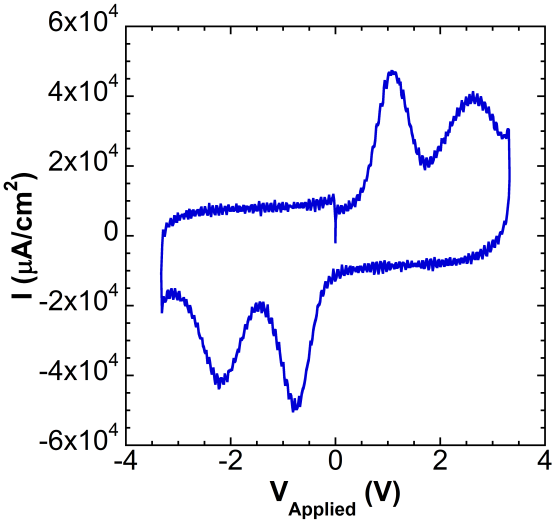

Figure 5.10. Current vs electric field curve of a HZO capacitor resulting from a triangle wave from 0 to -3.5 to 3.5 to 0 V showing two switching events.

In the course of applying 100 cycles of a 3.5 V triangle wave, the two current peaks merge into a single peak, see Figure 5.11. This phenomenon is referred to as "wake-up". According to Schenk *et al.*, defects within the HZO are mobile and become

more evenly distributed throughout the domains as the HZO capacitor is repeatedly switched.[113] A wake-up cycling procedure homogenizes the coercive voltage and stabilizes the run-to-run variations. It should be noted that more than half of the HZO devices failed within this wake-up step. The failure mechanism, which is proposed to be caused by conductive filamentary growth through the dielectric[114], causes the device to short the two capacitor electrodes, with a resistance on the order of 100 Ω.

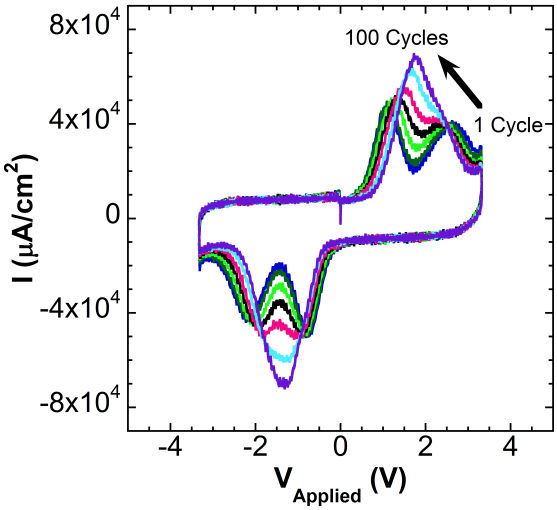

Figure 5.11. Successive current vs voltage curves of the HZO capacitor resulting from a triangle wave from 0 to -3.5 to 3.5 to 0 V showing the evolution from a bimodal to single mode distribution of coercive voltage. Measurements by C. Alessandri.

The P-E curve obtained by integrating the FE switching current from the 1st and 100th triangle wave cycle (Figure 5.12) shows the difference in P-E curves as the HZO wakes up. By fully switching the FE using a 3.5 V triangle wave, a remnant polarization of $\pm 1.5\ \mu C/cm^2$ can be obtained in this device, which corresponds to a

sheet charge density of 1.0x10^{13} cm^{-2}.

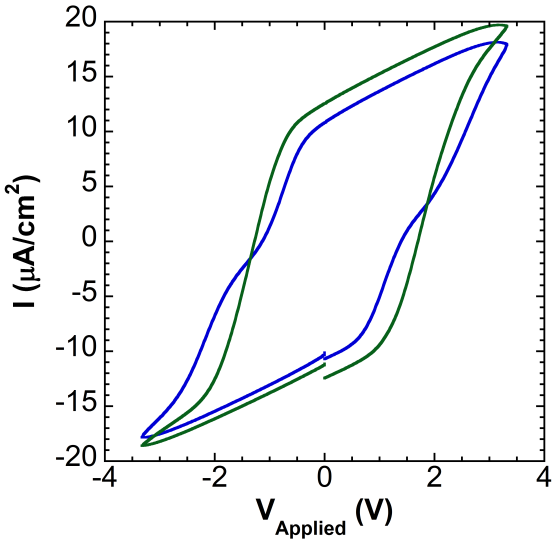

Figure 5.12. Polarization vs electric field curves of the HZO capacitor showing the difference between the first cycle (blue) and after 100 cycles (green), demonstrating the wake-up effect.

Following wake-up consisting of 100 cycles of the 0 to -3.5 to 3.5 to 0 V triangle wave, the pulse train shown in Figure 5.2 was applied to the HZO capacitor, with varying pulse width as well as pulse amplitude. From this data, we are able to obtain how the polarization changes with programming voltage amplitude pulses and pulse width fit to Equation 5.3 (values shown Table 5.1). By using a voltage distribution model, we are able to predict the response of the HZO capacitor to a pulse of width between 1-100 μs and 1-3 V (Figure 5.13). The fit to the model indicates that the maximum change in polarization is 1.12 $\mu C/cm^{-2}$, with the mean coercive voltage of the distribution of 4.76 V. The value of T_0 ($8.513x10^{-7}$ s) indicates that for times

below 1 μs, a significant portion of the partial switching is due to the slew rate, so to better physically characterize this sample at times approaching 1 ns, a pulse generator with a faster slew rate is required.

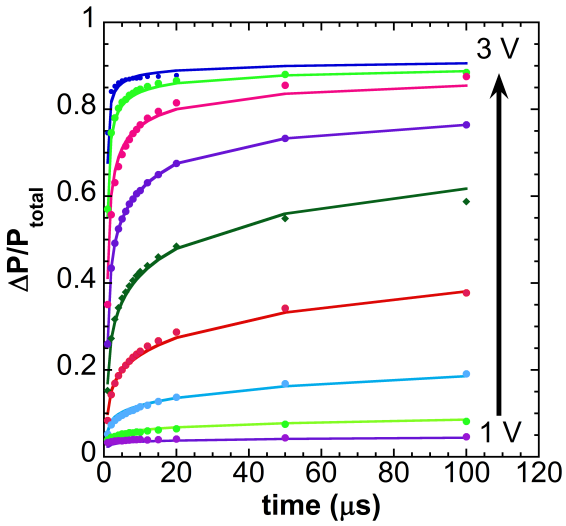

Figure 5.13. Polarization vs time curves of the HZO capacitor switched using pulses of varying width and voltage, with the fitting to the model described in Equation 5.3.

TABLE 5.1

VALUES OBTAINED BY FITTING TO DATA OBTAINED FROM THE HZO CAPACITOR

	Value	Unit
τ_0	$42.1x10^{-8}$	s
τ_1	$4.59x10^{-13}$	s
α	0.9907	
T_o	$8.51x10^{-7}$	s
β	0.434	
γ	42.85	
V_m	4.76	V
P_{Max}	1.12	$\mu C/cm^2$

5.3.3 RPU Device Considerations

While we showed that 12 nm HZO was able to be partially switched, one fabrication concern is the footprint of the FE-based RPU. The requirement by Gokmen and Vlasov is that the device area should be less than 200 nm x 200 nm.[6] If the domain size is assumed to be approximately the square of the thickness of the film, then a domain will be on the order of $\sim$100 nm^2. If we are able to fabricate a device such that 1 domain switching is equal to one level change, then a planar device will not be suitable for this application, as 1000 domains, 100 nm^2 in area will not fit in the 200 nm x 200 nm area requirement. This indicates that in order to fabricate a FeRPU without relaxing design constraints, a vertical structure likely the most favorable design (Figure 5.1, right schematic).

In order to determine the aspect ratio required of a vertical device, first, the target conductance of the device, with no FE polarization must be determined. Gokmen and Vlasov require that the minimum and maximum conductance be 9 nS and 71 nS, respectively. Because for such a device, we will want to use just one half of the remnant polarization (*i.e.* just the positive or just the negative polarization), meaning that at $P = 0$, we must be either at a minimum or maximum of conductance. By assuming the device will operate such that the minimum conductance is at $P = 0$, and assume a value of n_0 of 1x10^{11} cm^{-2}, the W/L of the device must be 0.38. A device with 400 nm channel width (the perimeter of a 200 nm x 200 nm pillar) would require a 1 micron long channel. Physically this device's channel would consist of a pillar with a 200 nm x 200 nm base that is 1 μm tall. Such a pillar would have a surface area of 400,000 nm^2, which assuming 100 nm^2 per domain, could have as many as 4000 domains per device. These calculations just set the mean value, while the maximum and minimum will depend on the polarization of the FE and how the interface between the channel and the ferroelectric will effect the FE polarization's influence on the channel. If the polarization of the FE is too large, a non-FE dielectric can be placed between the channel and FE to lessen the polarization's impact.

A symmetric change in polarization for increasing and decreasing polarization is desired for the FeRPU. The model discussed above indicates that near full polarization, there is a highly asymmetric response, for example near $\Delta P/P = 0.8$, a 2.5 V, 1 μs pulse in the direction of the remnant field will change the polarization by +2.0%, however the opposite pulse will change polarization by -6.9%. However, closer to $P = 0$ ($\Delta P/P = 0.5$), the response is more symmetrical. For example, at $\Delta P/P = 0.6$, a 2.5 V, 1 μs pulse in the direction of the remnant field will change the polarization by +14.2%, however the opposite pulse will change polarization by -13.9%. This, coupled with the linear response in conductance to change in polarization means that the proposed RPU should operate symmetrically in this linear polarization response

region.

5.4 Conclusions

In this Chapter, we showed that we can, using voltage pulsing, partially switch the remnant polarization of a FE film. PZT capacitors were tested to show how FE polarization is measured. Pulsed measurements were used to set intermediate partial polarization states. HZO capacitors were characterized using the same procedures with a FE thickness of 12 nm. We report for the first time the partial switching characteristics of an HZO capacitor, model its behavior using a distribution of switching voltages.

In order to fully realize a FeRPU, several hurdles must be overcome. First, developing a process to grow a thin FE directly onto a channel material (or vice-versa) is required in order to make a FeFET. Next, the operating voltage must be scaled down, either by thinning the FE, or by selecting a FE with a lower coercive field. As well, the device area must be scaled down to the 0.04 μm desired for an RPU. Device longevity is also an issue, as an RPU will ideally be partially switched throughout the deep neural network's learning process, and a single device failure could cause failure of the whole neural network. While there are still several steps before a fully functioning FeRPU, this work shows, through the first demonstrations of partial switching of a thin FE (HZO), and the modeling of partial FE switching based on a coercive voltage distribution, that building such a device is possible.

CHAPTER 6

CONCLUSIONS

This dissertation has demonstrated multiple novel ways of using EDL-induced sheet charges to open up new applications in the field of nanoelectronics. For example, in Chapter 2, we showed that the EDL retention time can be tuned by six orders of magnitude simply by increasing the T_g of the electrolyte by 100 ^{o}C. This means that EDL doping can be achieved at room temperature without the continuous application of a bias, and more interestingly, the EDL can be dissipated (and therefore the device can be "deprogrammed") with time. Although not demonstrated here, deprogramming by heat and exposure to water should also be possible because both will increase the mobility of the polymer and hence the ions in the EDL. Data stored in the charge state of an EDL that has been "locked" will remain stored for at least the time constant of the system, which could exceed the results shown in this work by engineering the polymer structure. If the data needed to be erased at a later time, which could potentially be accomplished by an on-chip heater that increases electrolyte temperature above the T_g, the EDL would dissipate in milliseconds without the need to overwrite each memory element individually. In addition, an electrolyte utilizing the ion locking strategy outlined in this work could be used to obscure the function of a given circuit by enabling devices that could be programmed to n- or p-type to define the circuit, then deprogrammed to an undoped state, making reverse engineering more difficult and enabling hardware that can be disabled on the hardware level instead of the software level.

One drawback to EDL gating/doping is the speed of the ions. At room temperature, the complete formation of the EDL can require milliseconds, as shown in Chapter 4. One way to speed-up the formation is to apply a driving force (*i.e.* applied gate voltage) that is larger than the electrochemical voltage window of the electrolyte. However, this large voltage could only be applied for a short time so that electrochemistry does not have time to occur. In Chapter 3 we investigated how SPE-gated MoS_2 FETs with varying channel thickness respond when operated at biases exceeding the electrochemical window by a factor of 10 (*i.e.*, $\pm$ 40 V). However, instead of exposing the device to short pulses of high field, long-term exposure is explored to characterize the signature of electrochemical response and volumetric changes caused by ion intercalation. These results represent an upper bound and will inform future pulsed measurements. We show that for thinner ($<$ 50 MoS_2 layer) channels, the stress due to ion intercalation fractures the MoS_2 channel. However, one device with a 120-layer thick channel could be repeatedly cycled over the large voltage range without failing to open circuit even though the thickness increases by 400% in some areas of the channel. In addition, the results show how MoS_2 devices will fracture and fail at biases below which the electrolyte itself has not undergone dielectric breakdown.

The transfer of graphene FETs onto PEO:$LiClO_4$ presented in Chapter 4 highlights a transfer process that demonstrates the feasibility of placing pre-fabricated 2D crystal FETs directly onto a SPE. To our knowledge, this is the first demonstration of such a transfer; however, the device yield is low. Although only the transfer characteristics of graphene FETs backgated with SPE were explored, this is an important demonstration if other 2D materials are to be backgated with a solid electrolyte. One advantage to this type of gating is for the contact itself to be heavily doped by the ions, which could open up possibilities for efforts in contact engineering.

The ferroelectric capacitor testing discussed in Chapter 5, while not a ground-

breaking implementation of partial switching ferroelectrics on its own, is important to understanding how partial switching can be used for other applications. Moreover, it is the first step to developing a resistive processing unit (RPU). In Chapter 5, partial switching of $HfZrO_2$ (HZO) is shown for the first time. This is important because HZO can be grown as thin as 12 nm without losing its ferroelectric properties. As discussed in Chapter 5, the thinner the ferroelectric, the higher the number of domains in the film. The greater the number of domains, the greater the number of possible levels in a partially-switched ferroelectric device, such as an RPU. This maximizes the number of available states that an RPU implementing HZO can take.

The deposition of gate dielectrics on 2D crystals to form a traditional MOS structure represent a significant developmental hurdle. This is due to the lack of dangling bonds on the surface of 2D crystals, which would normally provide nucleation sites for dielectric growth. By instead using a SPE, which can be deposited as a pinhole-free, solid film on a 2D crystal by solvent casting, material and device properties that require a topgate can be acquired without the process development required for a high-k dielectric. Thus, SPEs enable materials properties to be evaluated before dielectric and metal deposition recipes are developed. In this work, we have furthered the state of the art of electrolyte gating by 1) tuning the thermal properties of the SPE to tune the lifetime of the EDL, 2) exploring the effect of large biases which will inform future pulse measurements, and 3) developed a process for electrolyte backgating which could enable SPEs to be used for new types of device architectures.

In addition to depositing high-k dielectrics on 2D crystals, it is also difficult to substitutionally dope 2D materials. Not only do the doping processes require further refinement, but the dopants themselves will alter the band structure of the 2D material in ways yet to be understood. By using either an ion-locked SPE or a ferroelectric in place of a dielectric, doping can be mimicked by the fixed charge provided by the locked-in EDL or the remnant polarization, respectively. These

approaches allow researchers to overcome the challenges presented by traditional doping strategies. Because SPEs and ferroelectrics can induce sheet carrier densities of $> 10^{13}$ cm^{-2}, it is possible to degenerately dope 2D materials, due to the thin body of the device. An added feature is that doping can be reconfigureable; that is, n- and p-type doping can be achieved by reversing the polarity of the applied bias. This feature cannot be achieved by a permanent, substitutional dopant.

The ions present in SPEs cause processing concern for VLSI technology, because the ions could lead to unwanted doping. However, there exist other examples in CMOS technology where ions have been successfully contained, such as Cu ions in Si devices and ions in resistive random access memory (RRAM). In contrast to SPEs which are now only being explored as tools in basic materials research, ferroelectrics are already available in commercial FeRAM devices sold by several companies, and are therefore more attractive in the near-term for technology development. The availability of ferroelectric processes that can be integrated with common Si-based devices implies that a technology based on ferroelectrics would require a small technological step compared to the large leap that would be required for SPE implementation. Thus, it is more feasible that the partial switching results reported in this work could be applied to devices such as a 2- or 3- terminal analog memory, as well as the resistive processing unit application outlined by IBM.

APPENDIX A

GENERAL EXPERIMENTAL PROCEDURES

A.1 Atomic Force Microscopy

Atomic Force Microscopy (AFM) is a form of scanning probe microscopy in which a probe with a small ($\sim$ 50 nm) tip makes physical contact with the surface to be measured. By reflecting a laser off the back of the tip and onto a detector, the tip deflection can be tracked, as the tip is rastered across the sample surface, which resolves to a 3D image of the sample surface.

For this work, the Bruker Dimension Icon AFM was used. Images were taken using the Scanasyst mode, using a Scanasyst-Air tip, which is a SiN tip on a Si lever.

A.2 Differential Scanning Calorimetry

To measure the phase transitions within polymers, differential scanning calorimetry (DSC) is used. In this work, a Mettler Toledo DSC-1, calibrated using an indium standard, was used. DSC works by measuring a sample and a reference, typically the reference is simply an empty DSC sample pan, to remove any effect from the pan from the measurement. The temperature of the sample and reference is swept, and the difference between the power required to change the temperature of the reference vs the sample is recorded. As phase transitions occur, the latent heat required can be seen as an increase in the heat required to change the temperature of the sample.

A.3 Fourier Transform Infrared Spectroscopy of Polymer Films

Fourier Transform Infrared Spectroscopy (FTIR) is a method of absorption spectroscopy that is used to determine the chemical bonds within a sample that have a dipole moment (IR active bonds). The sample absorbs IR radiation at the energy of the vibration modes of the bonds in the samples, meaning that the decrease in transmittance correlates to the bonds within the sample. FTIR gives a result in wavenumbers (cm^{-1}), with each bond having a characteristic peak. From these data, the chemical bonds within the measured sample can be determined.

In order to measure a polymer film using FTIR, it is recommended that an Attenuated Total Reflectance module be utilized. This module uses the attenuation of the total internal reflection within a crystal, on top of which the sample is mounted, to determine the FTIR spectrum without the light from the source having to pass through the sample. This allows for a polymer sample to be deposited on an opaque substrate, such as a Si wafer.

In this work, all measurements were taken using a Jasco FT/IR-6300 with a single-reflection micro-ATR

A.4 CO_2 Cleaning of Graphene

It has been shown by Gong *et al.* that annealing graphene in a CO_2 environment can remove resist residue without damaging the underlying graphene.[115] As part of my contribution to the ACS nano paper by Xu et al., I set-up this CO_2 cleaning procedure and optimized it for the Notre Dame cleanroom.[73]

To clean the graphene FET channel of resist residue, an anneal in a CO_2 environment is performed. A tube furnace connected to CO_2 (99.99%) and N_2 (99.999%) gases. The sample is loaded into a sample boat, and then placed in the tube furnace (at room temperature). Once the sample is in the furnace, the tube is purged with

N_2 for 15 minutes at a flow rate of 300 sccm. This ensures that the tube is completely dry and free of other gasses that may react with the sample surface. Following the N_2 purge, the tube is then purged with CO_2 for 30 minutes at 100 sccm.

After the tube is purged with CO_2, the flow rate of CO_2 is reduced to 10 sccm while the furnace is heated to the target temperature of 500 ^oC at a rate of 20 ^oC/min. The furnace is then kept at 500 ^oC with the 10 sccm CO_2 flow for 30 minutes to etch the resist residue. To end the resist etch step, the CO_2 flow is replaced by a 300 sccm N_2 purge while the furnace is allowed to cool back to room temperature. Following this cleaning procedure, AFM is used to ensure that the resist residue has been removed, while Raman spectroscopy is used to confirm that the graphene has not been oxidized or made defective by the process.

APPENDIX B

SUPPORTING INFORMATION FOR CHAPTER 2

B.1 Device Fabrication

To form the bi-layer resist stack used to mask the channel area, the sample was pre-cleaned in a 70 ^{o}C acetone bath, rinsed with isopropanol and deionized water, and baked at 200 ^{o}C for 2 min to dehydrate the surface. A 3 μm polymethylglutarimide-SF9 (PMGI-SF9, MicroChem) layer was spin-coated onto the surface, followed by a 180 ^{o}C, 5 minute hard bake. After cooling on a metal benchtop, a 1.2 μm-thick layer of MEGAPOSIT SPR700-1.2 (Dow Electronic Materials) was spin-coated, followed by a 90 ^{o}C, 1 minute soft bake. Following an exposure of 70 mJ/cm^2, a 1 minute post-exposure bake was completed at 115 ^{o}C. The sample was developed in AZ917 Metal Ion Free developer (Integrated Micro Materials), followed by a deionized water bath. The graphene channel was defined using an oxygen plasma etch in a PlasmaTherm 790 Series Reactive Ion Etcher (RIE), with an RF power of 150 W and a DC bias of 330 V. A 60 s etch was sufficient to etch the graphene not protected by the bilayer resist structure, thereby isolating the device channels. Following the etch, the photoresist was removed in a 70 ^{o}C bath of resist remover (mr-Rem 400, Microchem).

This same bilayer resist strategy was also used to pattern the resist for source/drain contact deposition, followed by electron beam evaporation of 5 nm Ti (as an adhesion layer, base pressure 2.0 x 10^{-6} Torr, 1 Å/s deposition rate) and 245 nm Au (base pressure 1.0 x 10^{-6} Torr, 2 Å/s deposition rate). Hot acetone (T = 70 ^{o}C) was used for lift-off, with an isopropanol rinse. A hot mr-Rem 400 (T = 70 ^{o}C) bath, followed

by a room temperature mr-Rem 400 bath (to prevent photoresist redeposition) and an isopropanol rinse was used to remove resist residue.

B.2 DSC Measurements

Because the electrolytes do not recrystallize on the time scale of the heat/cool/heat measurement shown in Figure 1, the T_m cannot be captured during the second heating scan; therefore, the first heating scans are considered in Figure S1. The first heating scan for samples that were stored at room temperature for 27 days after heating to 250 ^{o}C are shown in Figure S1(a). While pure PVA shows the same melting peak in the first scan as the second scan, meaning that pure PVA crystallizes on the timescale of the DSC measurement, melting features are also apparent in the first heating scan for all samples that contain $LiClO_4$. Two peaks are observed in the 100:1 sample, the larger of which is likely pure PVA. A new endothermic peak appears between 50 and 150 ^{o}C in each of the four $LiClO_4$-containing samples. This, along with the suppression and eventual loss of the PVA melting peak with increasing salt concentration, could indicate the formation of a new $(PVA)_X$:$LiClO_4$ complex. This conclusion is supported by the phase diagram of a similar electrolyte, PEO:$LiClO_4$, which has two such complexes: $(PEO)_3$:$LiClO_4$ and $(PEO)_6$:$LiClO_4$. However, to our knowledge, the phase diagram of PVA:$LiClO_4$ has not been reported.

Unlike the samples with other salt concentrations, the 8:1 sample shows a noisy, repeatable, endothermic feature in the range of 180 - 220 ^{o}C. The melting point of pure $LiClO_4$ is 236 ^{o}C, and it is possible that this feature represents the melting of $LiClO_4$ that has phase separated from the PVA. Whereas PEO can accommodate higher lithium concentrations (up to 3:1 for $LiClO_4$)[1, 29] these results suggest that $LiClO_4$ is less soluble in PVA than PEO.

Because recrystallization does not occur on the time scale of the DSC measurement for the samples containing $LiClO_4$, additional DSC measurements are made

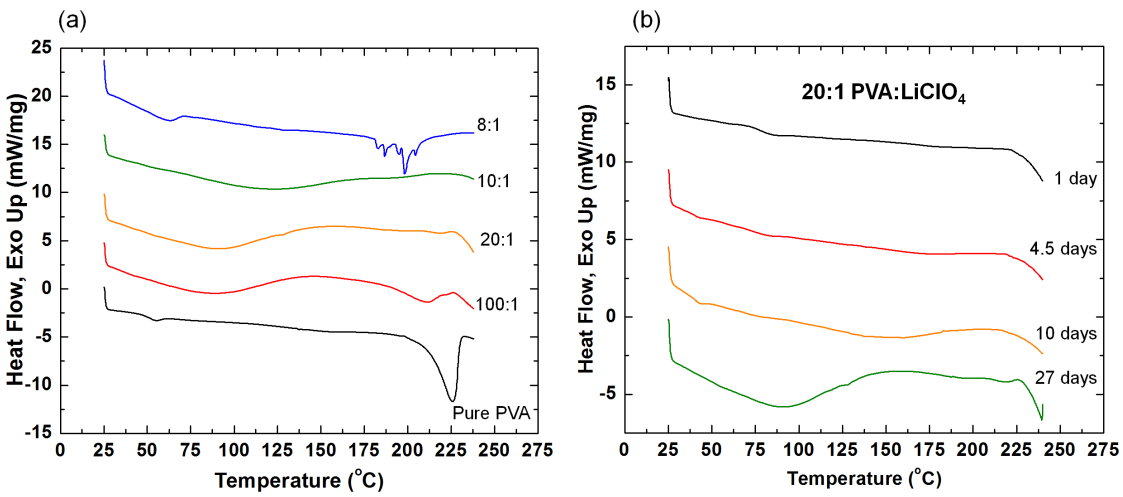

Figure B.1. (a) First DSC heating segments showing the T_m of electrolytes at varying $LiClO_4$ concentrations. Note, these samples were heated to T = 250 ^{o}C, stored at room temperature for 27 days, and then the data were acquired. (b) First heating segments of $(PVA)_{20}$:$LiClO_4$, with the time on the plot indicating the time after the sample was heated to T = 250 ^{o}C. Data are offset on the y axis for clarity.

after the 20:1 sample is heated to T > T_m and allowed to recrystallize at room temperature in the DSC pan for between 1 and 27 days, shown in Figure S1(b). A melting feature begins to appear at 10 days (Figure S1(b)), and increases in magnitude at 27 days. The results show that the 20:1 sample requires at least 4.5 days at room temperature for recrystallization to become detectable by DSC. Considering the DSC data for all the lithium concentrations, the 20:1 sample is chosen for gating the devices because the melting temperature is still relatively low (*i.e.*, $T_m^{peak} \approx 85^o$C for 20:1 compared to $T_m^{peak} \approx 125$ ^{o}C for 10:1 in Figure S1(a)), which allows for a lower programming temperature. While the midpoint of the 20:1 feature is $\approx 85^oC$, the feature is broad and extends to $\approx 125^oC$, meaning that the sample is semi-crystalline immediately following programming at T = 100 ^{o}C. In addition to the comparatively lower T_m than the other concentrations, the 20:1 concentration is a good choice for this study because the polymer to salt molar ratio has been used

for other electrolytes, such as $(PEO)_{20}$:$LiClO_4$, making it a good choice for bench marking performance.[5]

B.3 Hall Measurements

Hall measurements were taken using the van der Pauw method outlined in the Experimental Details portion of this work. While the current was flowed through two opposing contacts (*i.e.* 1,3 or 2,4), then the voltages were measured on the remaining 2 pads (2,4 or 1,3). The Hall voltage was then computed using the van der Pauw method. From this, the sheet carrier density (n_s) was calculated using the equations below, where e is the elementary charge, and the calculated biases are found by subtracting the values measured with the magnet in the North and South configuration.

$$V_H = \frac{V_{13} + V_{24} + V_{31} + V_{42}}{8} \tag{B.1}$$

$$n_s = \frac{I_{Applied} B_{Applied}}{e V_H} \tag{B.2}$$

TABLE B.1

HALL DATA FROM VAN DER PAUW STRUCTURE

	Programming Bias	+2 V	+2 V	-2 V
	B-field (T)	$5.22\text{x}10^{-1}$	$5.22\text{x}10^{-1}$	$5.22\text{x}10^{-1}$
	Applied Current (A)	$1.00\text{x}10^{-4}$	$1.00\text{x}10^{-4}$	$2.00\text{x}10^{-5}$
North	V_{24}	$-6.52\text{x}10^{-4}$	$-6.86\text{x}10^{-4}$	$2.95\text{x}10^{-3}$
	V_{42}	$6.04\text{x}10^{-4}$	$6.38\text{x}10^{-4}$	$-2.95\text{x}10^{-3}$
	V_{13}	$-3.86\text{x}10^{-4}$	$-3.86\text{x}10^{-4}$	$-2.88\text{x}10^{-3}$
	V_{31}	$3.33\text{x}10^{-4}$	$3.33\text{x}10^{-4}$	$2.86\text{Ex}10^{-3}$
South	V_{24}	$3.74\text{x}10^{-4}$	$3.39\text{x}10^{-4}$	$-1.84\text{x}10^{-3}$
	V_{42}	$-4.21\text{x}10^{-4}$	$-3.89\text{x}10^{-4}$	$1.82\text{x}10^{-3}$
	V_{13}	$6.36\text{x}10^{-4}$	$6.36\text{x}10^{-4}$	$1.72\text{x}10^{-3}$
	V_{31}	$-6.87\text{x}10^{-4}$	$-6.93\text{x}10^{-4}$	$-1.79\text{x}10^{-3}$
Calculated	V_{13}	$-1.02\text{x}10^{-3}$	$-1.02\text{x}10^{-3}$	$-4.60\text{x}10^{-3}$
	V_{24}	$-1.03\text{x}10^{-3}$	$-1.03\text{x}10^{-3}$	$4.79\text{x}10^{-3}$
	V_{31}	$1.02\text{x}10^{-3}$	$1.03\text{x}10^{-3}$	$4.65\text{x}10^{-3}$
	V_{42}	$1.03\text{x}10^{-3}$	$1.03\text{x}10^{-3}$	$-4.77\text{x}10^{-3}$
	V_{Hall}	$-5.12\text{x}10^{-4}$	$-5.13\text{x}10^{-4}$	$3.87\text{x}10^{-5}$
	$\lvert n_s \rvert$	$6.37\text{x}10^{13}$	$6.36\text{x}10^{13}$	$1.68\text{x}10^{14}$

APPENDIX C

SUPPORTING INFORMATION FOR CHAPTER 3

C.1 Leakage Current

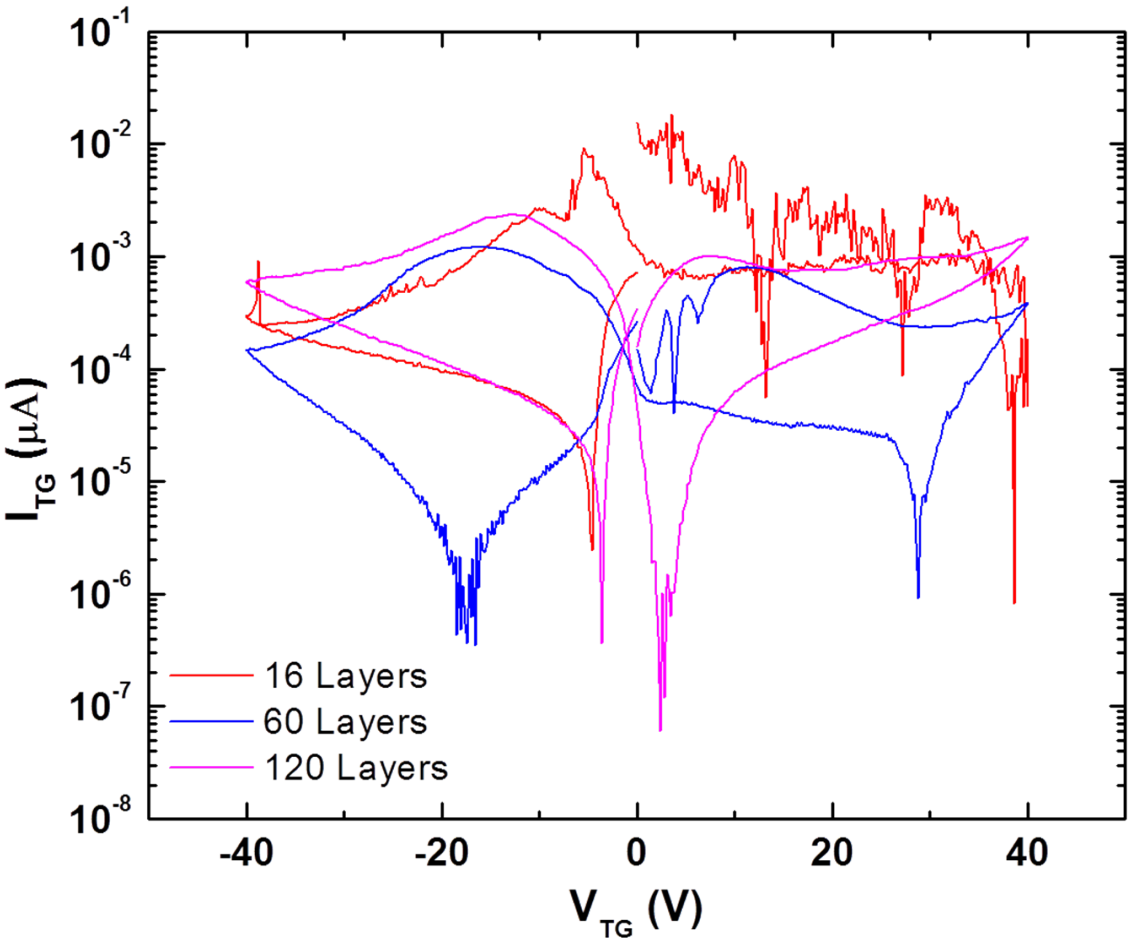

Figure C.1. Leakage current from the transfer characteristics of all MoS_2 FETs showing that there is no short between the channel and gate.

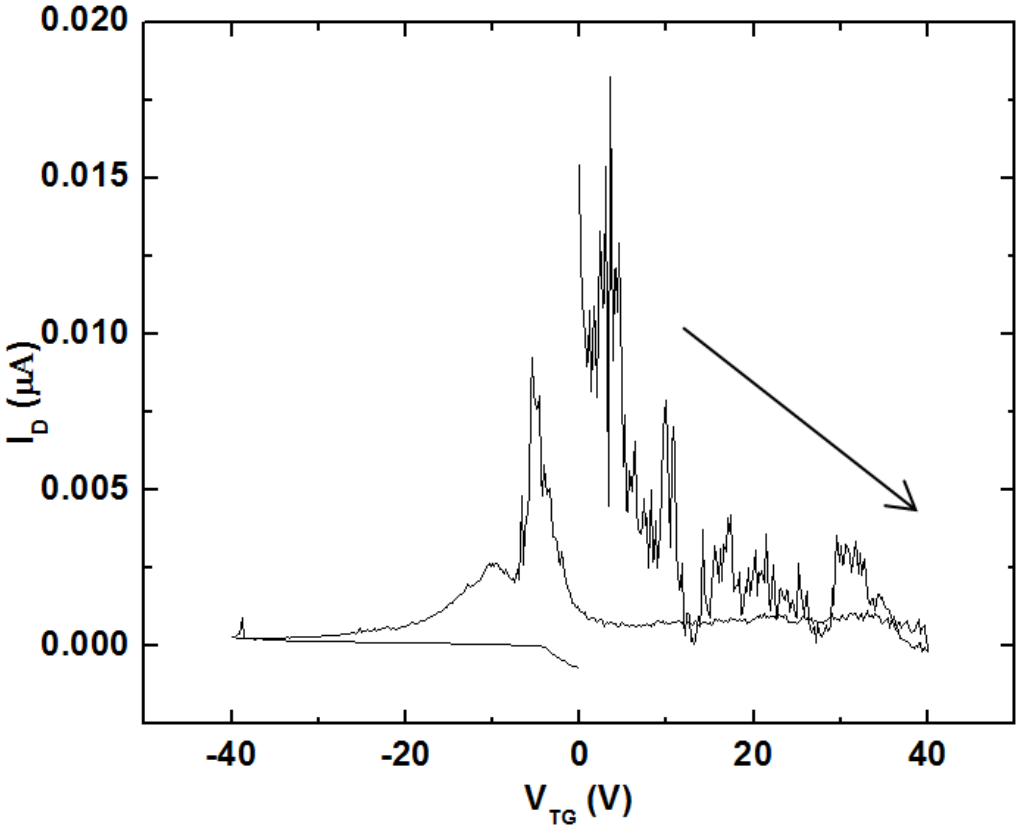

Figure C.2. Example of $I_D - V_{TG}$ data during device failure. Transfer characteristics of the 60-layer device during the sweep where the channel cracks sufficiently to no longer allow conduction. After the electrolyte was removed via solvent cleaning, AFM scans show that the MoS_2 channel was completely removed during cleaning. Sweep rate = 0.5 V/s; V_DS = 0.5 V

C.3 Raman Data

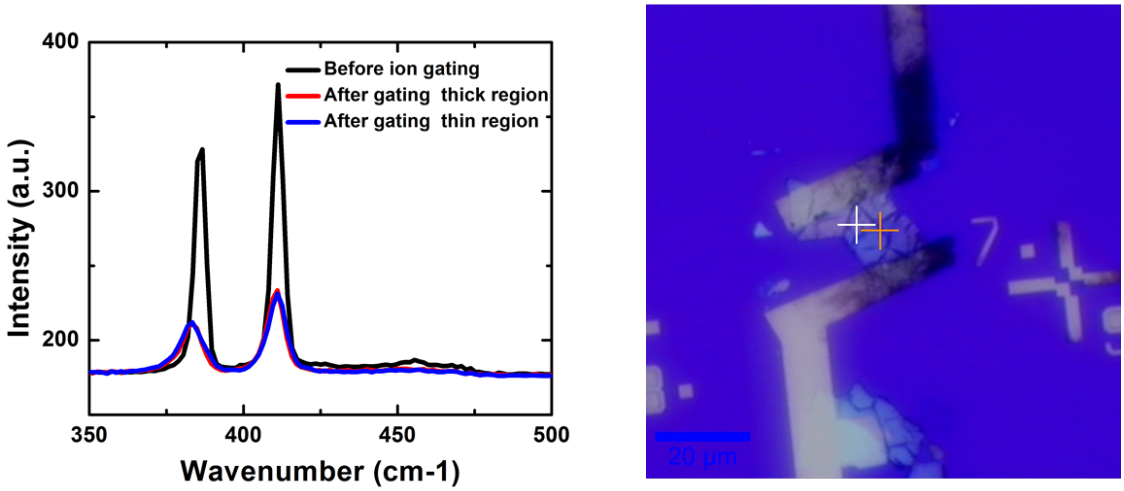

Figure C.3. Left) Raman spectra before and after voltage cycling. After cycling, two channel regions of varying thickness were measured (see corresponding AFM in Fig. 2d). (Right) Optical image of the physical area where the spectra were taken, as indicated by the crosshairs (the white crosshair indicates the thin region and the red crosshair indicates the thick region). There is no peak in the Raman spectra near 349 cm-1 indicating that the 1T MoS_2 phase is not present, however we are unable to tell if there is Li_2S in the sample, as the (typically weak) Raman signature of Li_2S is at 375 cm^-1, which is in the center of one of the MoS_2 peaks, meaning that MoS_2 and Li_2S cannot be distinguished by Raman spectroscopy alone. XPS, NMR or XRD could possibly be used to locate Li_2S.

C.4 Band Diagrams for Li^+ Intercalation

The change in the band diagram for the EDL gate capacitor (with the stack gate/PEO:$LiClO_4$/MoS_2/back gate) is important to model to properly understand how intercalated Li^+ can affect the MoS_2 device characteristics. The flat band dia-

gram (Figure C.4) consists of a 500 nm thick layer of electrolyte, on a 50 nm thick layer of MoS_2, on 300 nm of oxide. We assume a 4.2 eV as the band gap for PEO:$LiClO_4$, as measured optically on a similar electrolyte by Chapi *et al.*.[116] The Fermi level is set to the middle of the electrolyte as there is no net doping in the electrolyte. Because we are using a 50 nm thick MoS_2, we use the bulk band gap of 1.3 eV.[87] For the simulation, a light (10^{14} cm^{-3}) n-type doping is applied to model the initial n-FET behavior shown by the FET prior to electrolyte deposition. Ohmic contacts are assumed for both gate contacts, as the contact is just controlling the Fermi level in the insulator.

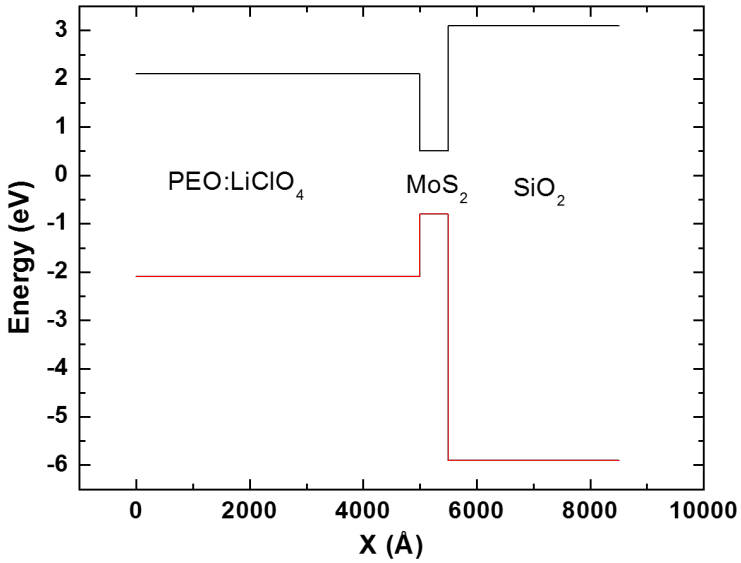

Figure C.4. Flat band diagram of the EDL FET gate capacitor.

The program 1D Poisson[7] was then used to calculate the band diagrams for both positive (C.5a) and negative (C.5b) applied gate biases for the structure described

above. For this model, the electrolyte was treated as a dielectric with no mobile ions in combination with equal and opposite sheet charges at the electrolyte interfaces. This mimics the effect of the majority of the voltage drop occurring across the EDLs. Though this is a simulation perpendicular to the channel, we know that the contact to the channel at the drain and source are Ti, which forms an n-type contact with a barrier of 0.28 eV, meaning that electrons will flow easily, while the contacts will act as a hole blocking layer.[117] This means the electron conduction shown in Figure C.5a will occur in the device, while the mobile holes in Figure C.5b will be blocked by the contact, meaning no current will flow. This is in agreement with the n-FET behavior seen in the first few sweeps of the 120-layer device.

The device is modeled post-Li intercalation by assuming that the Li^+ will induce electrons in the channel. This is modeled by increasing the doping level of the MoS_2 from 10^{14} to 10^{18} cm^{-3}. The same ± 1 V band simulations are run and in the +1 V case, there is not a large difference in the band diagram, other than the conduction band of the channel is closer to the Fermi level, which would manifest as an increase in current. However, for the -1 V case, because the MoS_2 is so highly doped, electron conduction still occurs, as is observed in Figure 3.1b. These band diagrams tell us that if the doping level of the MoS_2 is changing from 10^{14} to 10^{18} cm^{-3} during intercalation, then back to 10^{14} cm^{-3} as the Li undergoes an electrochemical reaction, we would expect to see transfer characteristics similar to Figure 3.1b.

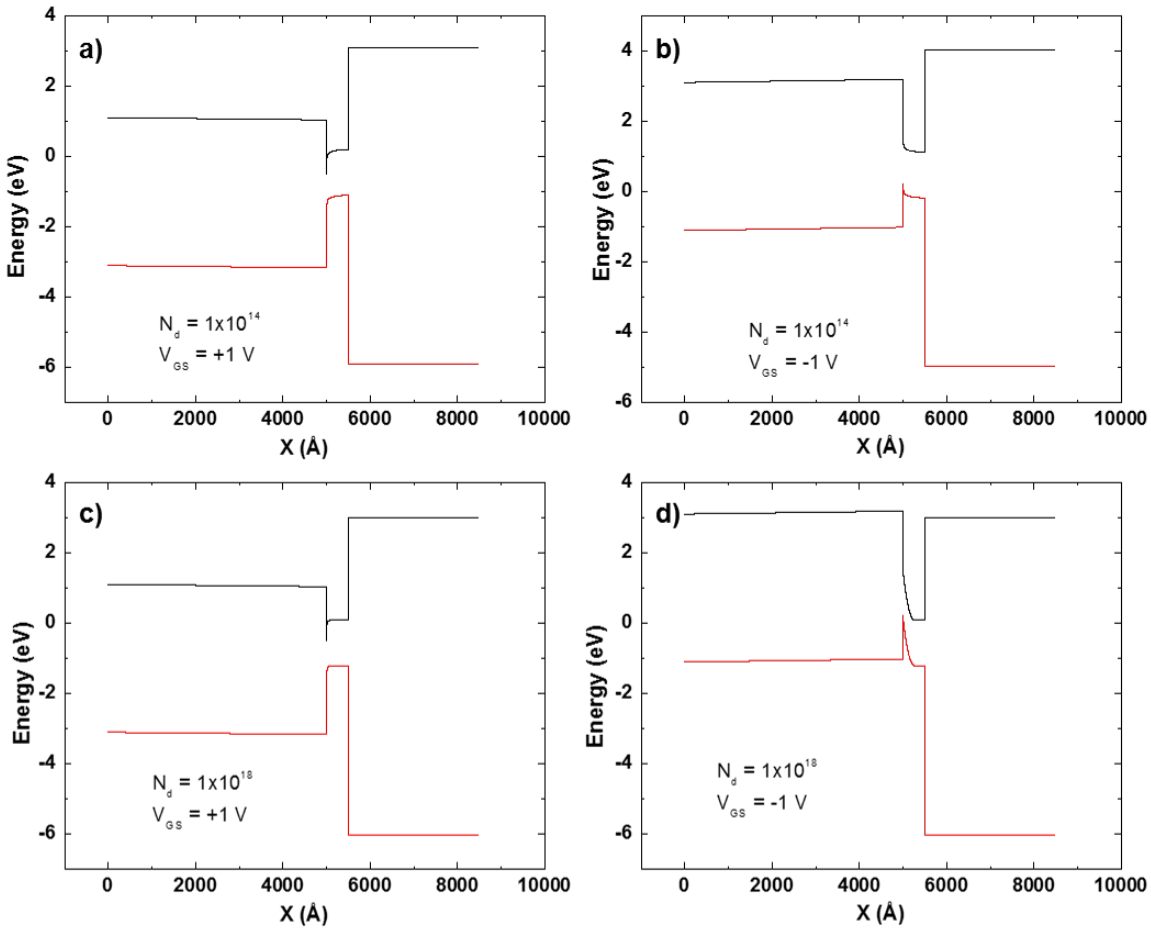

Figure C.5. Band diagrams of the MoS_2 EDL FET generated using 1D Poisson[7] for +1 V (a) and -1 V (b) applied to the gate of the device as-fabricated. The same band diagrams are also generated assuming that the intercalated Li causes a 4 order of magnitude increase in doping level for both $V_{GS} = +1$ (c) and -1 V (d).

APPENDIX D

SUPPORTING INFORMATION FOR CHAPTER 4

Figure D.1 has cartoons demonstrating the band diagrams in the operation of the electrolyte gate. Graphene is drawn as the E-k diagram showing the Dirac cone, so electron and hole conduction can be identified. The Dirac point of graphene is set to the middle of the band gap at $V_G = 0$ V, as the mobile ions in the electrolyte tend to shift the Dirac point of graphene towards zero. This occurs because when the fermi level of graphene is not at the Dirac point, there are charges at the surface, which attract oppositely charged ions until the graphene surface is neutral. At zero gate bias, the electrolyte's band is flat, due to the lack of EDLs, however when a bias is applied, the EDLs can be seen in the electrolyte as the sharp band bending at the interfaces, with a positive bias driving Li^+ towards the channel, inducing electrons in the channel (Figure D.1, center). At negative gate biases, ClO_4^- is driven towards the channel, inducing hole conduction in the graphene (Figure D.1, right).

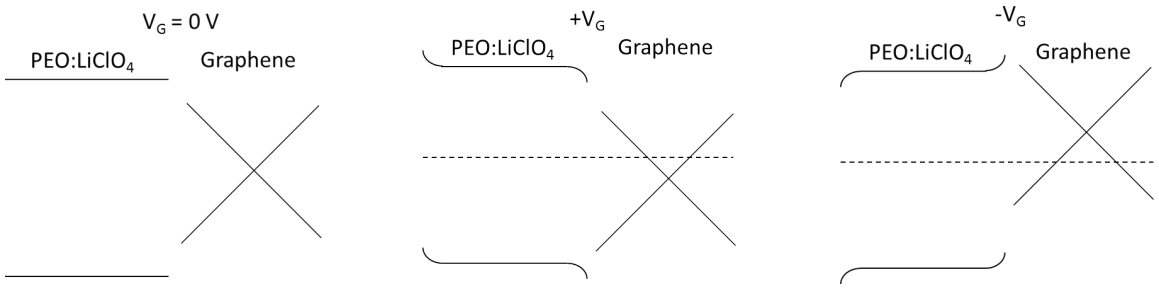

Figure D.1. Diagram describing the electrolyte and graphene band diagram at (left) zero applied gate bias, (center) positive gate bias, and (right) negative applied gate bias.

APPENDIX E

SUPPORTING INFORMATION FOR CHAPTER 5

To better understand how the remnant polarization of the ferroelectric in a FeFET changes the band diagram, a gate stack of 12 nm HZO/25 nm Si/90 nm SiO_2 is simulated using 1D Poisson.[7] For our simulation, the band gap, conduction band offset, and the dielectric constant were chosen to be the average of HfO_2 (5.7 eV, 1.5 eV and 30 respectively) and ZrO_2 (5.5 eV, 1.4 eV, and 25 respectively), 5.6 eV, 1.45 eV, and 27.5, respectively.[118, 119]

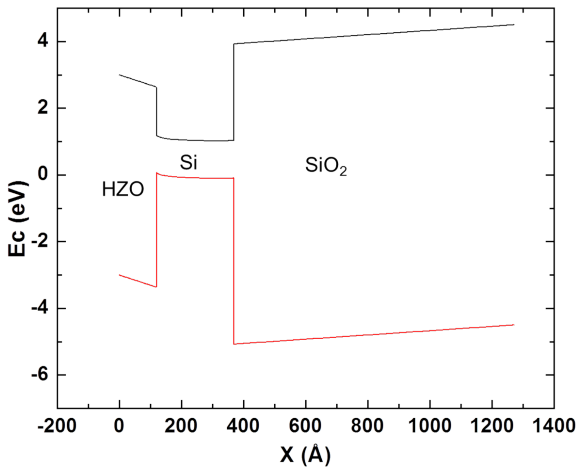

Figure E.1. Band diagram of HZO/Si/SiO_2 with zero remnant polarization.

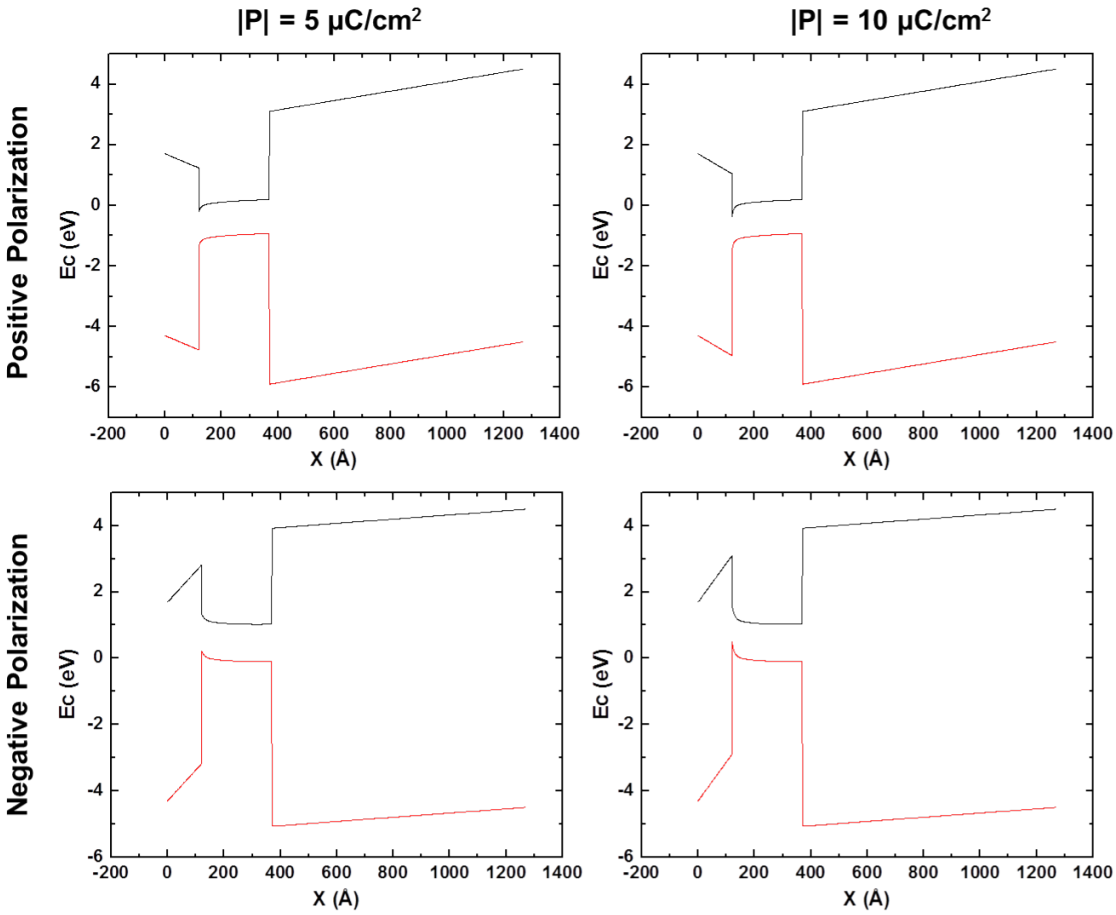

Figure E.2. Band diagram of HZO/Si/SiO_2 with remnant polarization of -10, -5, 5 and 10 μC/cm^2.

APPENDIX F

CO-AUTHOR PUBLICATIONS

Along with the work presented in this document, I was also co-author on several other publications (text of the papers attached below the descriptions):

E. W. Kinder, A. Fuller, Y. C. Lin, J. A. Robinson and S. Fullerton-Shirey, "Increasing the Room-Temperature Electric Double Layer Retention Time in Two-Dimensional Crystal FETs," in *ACS Appl. Mater. Interfaces*, 2017, Vol 9, Issue 29, pp. 25006-25013.

For this work, my contribution was electrolyte preparation, device fabrication, electrical measurements, FTIR measurements and DSC measurements, in addition to preparing the manuscript.

S. Fathipour, H. Xu, **E. Kinder**, S. Fullerton-Shirey, and A. Seabaugh, "Investigation of aging and restoration of polyethylene-oxide cesium-perchlorate solid polymer electrolyte used for ion doping of a WSe_2 field-effect transistor," in *Device Research Conference - Conference Digest, DRC*, 2014, pp. 125126.

In this work, I contributed by preparing and depositing the electrolyte, as well as assisting in interpreting data.

H. Xu, S. Fathipour, **E. W. Kinder**, A. C. Seabaugh, and S. K. Fullerton-Shirey, "Reconfigurable Ion Gating of 2H-$MoTe_2$ Field-Effect Transistors Using Poly(ethylene oxide)-$CsClO_4$ Solid Polymer Electrolyte," *ACS Nano*, vol. 9, no. 5, pp. 490010, May 2015.

My contribution to this work consisted of preparing and depositing the electrolyte, as well as assisting in fabrication.

K. Xu, H. Lu, **E. W. Kinder**, A. Seabaugh, and S. K. Fullerton-Shirey, "Monolayer Solid-State Electrolyte for Electric Double Layer Gating of Graphene Field-Effect Transistors," *ACS Nano*, p. acsnano.6b08505, May 2017.

For the above work, my contribution consisted of developing and performing a cleaning method for graphene using CO_2 (See Appendix A for details).

ACS APPLIED MATERIALS & INTERFACES

Research Article

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Increasing the Room-Temperature Electric Double Layer Retention Time in Two-Dimensional Crystal FETs

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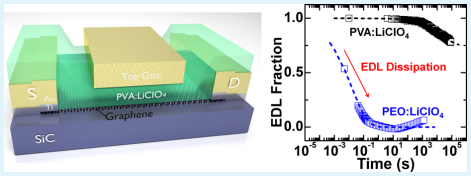
Supporting Information

ABSTRACT: Poly(vinyl alcohol) (PVA) and $LiClO_4$, a solid polymer electrolyte with a glass transition temperature (T_g) of 80 °C, is used to electrostatically gate graphene field-effect transistors. The ions in PVA:$LiClO_4$ are drifted into place by field-effect at $T > T_g$, providing *n*- or *p*-type doping, and when the device is cooled to room temperature, the polymer mobility and, hence ion mobility are arrested and the electric double layer (EDL) is "locked" into place in the absence of a gate bias. Unlike other electrolytes used to gate two-dimensional devices for which the T_g, and therefore the "locking" temperature, is well below room temperature, the electrolyte demonstrated in this work provides a route to achieve room-temperature EDL stability. Specifically, a 6 orders of magnitude increase in the room temperature EDL retention time is demonstrated over the commonly used electrolyte, poly(ethylene oxide) (PEO) and $LiClO_4$. Hall measurements confirm that large sheet carrier densities can be achieved with PVA:$LiClO_4$ at top gate programming voltages of ±2 V ($-6.3 \pm 0.03 \times 10^{13}$ cm^{-2} for electrons and $1.6 \pm 0.3 \times 10^{14}$ cm^{-2} for holes). Transient drain current measurements show that at least 75% of the EDL is retained after more than 4 h at room temperature. Unlike PEO-based electrolytes, PVA:$LiClO_4$ is compatible with the chemicals used in standard photolithographic processes enabling the direct deposition of patterned, metal contacts on the surface of the electrolyte. A thermal instability in the electrolyte is detected by both *I*−*V* measurements and differential scanning calorimetry, and FTIR measurements suggest that thermally catalyzed cross-linking may be driving phase separation between the polymer and the salt. Nevertheless, this work highlights how the relationship between polymer and ion mobility can be exploited to tune the state retention time and the charge carrier density of a 2D crystal transistor.



KEYWORDS: *poly(vinyl alcohol), $LiClO_4$, graphene, polymer electrolyte, field-effect transistor*

1. INTRODUCTION

Electric double layer (EDL) gating of field-effect transistors (FETs) using an electrolyte has been demonstrated for a variety of channel materials including polymer semiconductors,[1,2] two-dimensional (2D) crystals,[3−5] and metal oxides[6] using both ionic liquids[5,7,8] and polymer electrolytes.[3,4,9,10] EDLs are created when cations and anions in the electrolyte respond to an applied field that drifts the ions to the electrolyte−gate and electrolyte−channel interfaces, where they induce image charges in the gate and channel. The close proximity of the ion to its image charge induces gate capacitance ranging from 10 to 34 $\mu F/cm^2$.[1,4,11−13] Sheet carrier densities exceeding 1×10^{13} cm^{-2} have been demonstrated for both electrons and holes in graphene[4] and 2D crystal semiconductors.[3,14,15] The accumulation of ions near the channel and gate electrodes in combination with the charge neutral bulk of the electrolyte means that approximately half of the applied voltage drops across each of the two EDLs. This is physically equivalent to moving the gate to within approximately 1 nm of the channel. Electrostatic gating via ions is especially useful for 2D crystal semiconductors because it will not change the band structure, unlike traditional methods such as substitutional doping.[16]

Ionic liquids and solid polymer electrolytes (SPEs) are the most commonly used electrolytes for electrostatic gating. Ionic liquids are liquid-phase salts, whereas polymer electrolytes contain salt dissolved in a polymer. One advantage of polymer electrolytes is that, depending on the molecular weight, they can be solids at room temperature. In addition, they are easy to

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deposit by spin-coating or drop-casting onto 2D devices. If moisture is carefully controlled, SPEs are poor electrical conductors that can maintain low gate leakage currents (<10 pA/μm^2).[3]

It has been shown that by cooling a SPE to below its glass transition temperature (T_g), ionic motion in the electrolyte can be arrested, "locking" the ions in place, effectively doping the 2D channel with the EDL.[3,17] This strategy of exploiting the temperature-dependent mobility of the polymer to dope the channel of a FET device has proven useful for exploring new regimes of transport in 2D materials; however, the electrolyte gates reported to date are primarily based on PEO with a T_g well below room temperature. The reason for choosing PEO is that research on polymer electrolytes has been almost exclusively driven by the battery community for which fast ion transport and therefore the lowest possible T_g is desired. The low T_g requires the device to be cooled below room temperature to lock the ions into place.[4,18] For ion doping to be used in a practical device operating near room temperature, the ions would have to be drifted into place at a temperature greater than room temperature, then cooled to room temperature to fix the position of the ions. Specifically, by creating the EDL using a polymer electrolyte with T_g > 23 °C, a static doping profile can be obtained at room temperature in the absence of a gate bias. In this way, devices can be programmed *n*- or *p*-type, or *p*−*n* junctions can be created at $T > T_g$, and the resulting doping profiles can be maintained at room temperature without the need for constant biasing. It is also conceivable that these programmed devices could be engineered to be deprogrammed by specific triggers giving rise to new applications in hardware-based security. Such security could safeguard information by automatically erasing data stored in the EDL when tampered with, or when prompted to by the user.

In this study, we replace the commonly used polymer, poly(ethylene oxide) (PEO), with poly(vinyl alcohol) (PVA). While the T_g of PEO electrolytes can vary depending on the type and amount of salt, the T_g typically ranges from −36 to −8.5 °C (for ether oxygen to Li ratios of 100:1 and 4:1, respectively).[19] In contrast, the T_g of pure PVA is approximately 85 °C.[20] Although PEO and PVA are chemically similar, moving the oxygen from the main chain backbone in PEO to the side chain in PVA increases T_g by over 100 °C. In this work, we demonstrate that EDLs created using PVA:$LiClO_4$ at 100 °C can be locked into place at room temperature while maintaining high sheet carrier densities ($n_s \approx 1 \times 10^{14}$ cm^{-2}) for 160 min. This is a 6 orders of magnitude improvement in EDL retention time over PEO:$LiClO_4$ at room temperature.[18] In addition to the increase in room temperature EDL retention time, we also demonstrate, for the first time, the deposition of a photolithographically defined metal top gate deposited directly onto the electrolyte surface.

2. EXPERIMENTAL DETAILS

2.1. Electrolyte Preparation and Characterization. Electrolytes were prepared by dissolving poly(vinyl alcohol) (PVA, Mw = 100 000 g/mol, Polymer Standards Service) and lithium perchlorate ($LiClO_4$, Sigma-Aldrich, 99.9%) in 80 °C deionized water to form 1.0 wt % solutions with vinyl alcohol to Li ratios of 8:1, 10:1, 20:1, and 100:1.

Samples for differential scanning calorimetry (DSC) measurements were prepared under ambient conditions by depositing a portion of the PVA:$LiClO_4$:water solution in a Teflon beaker and heating it to 105 °C to evaporate the solvent. Eight to ten mg of the resulting film was placed in a 40 μL aluminum DSC pan (PerkinElmer), heated to 200 °C to soften the film, and pressed to create a hermetic seal. DSC measurements were taken using a Mettler-Toledo DSC1, calibrated with an indium standard. Samples were measured in the temperature range of 25−225 °C at a heating rate of 10 °C/min and cooling rate of 5 °C/min. Heat/cool/heat scans were acquired, where the first heating scan removed the thermal history of the samples.

Samples for FTIR analysis were prepared by dropcasting approximately 1 mL of the electrolyte solution onto a glass slide. The samples were then left in ambient until all the solvent had evaporated, leaving an electrolyte film on the glass slide. Two of the samples were then heated to 100 °C for 40 and 180 min, respectively. FTIR spectra were then acquired using the ATR module of a Jasco FT/IR-6300.

2.2. Device Fabrication. Devices were fabricated using a bilayer resist and the lithography processing details are outlined in the Supporting Information. Devices were fabricated on both CVD-grown graphene deposited on a Si/SiO_2 substrate (Supermarket Graphene, 10 nm SiO_2), and epitaxially grown graphene on SiC.[21] CVD graphene on Si/SiO_2 was used for devices in which both top and back gates were required, whereas epitaxial graphene on SiC was used because of the high quality and wide area of the material. Despite its low on/off ratio, graphene was used in this study to test the electrolyte because of its wide-area and high-quality.

A Bruker Dimension Icon atomic force microscope (AFM) in ScanAsyst mode was used to characterize surface residue after photolithography. ScanAsyst Air tips were used, which have a Si cantilever and a SiN lever.

The electrolyte with a vinyl alcohol to lithium ratio of 20:1 was chosen as the electrolyte gate for the devices in this study. $(PVA)_{20}$:$LiClO_4$ was deposited on the devices by dropcasting approximately 0.5 mL of 1 wt % solution on a 1 × 1 cm sample, and the solvent evaporated under ambient conditions. The sample was heated on an 80 °C hot plate for 3 min to drive off remaining solvent, leaving a film approximately 1 μm thick, as measured by AFM. Metal top gates were deposited directly onto the electrolyte using the same process to deposit source/drain contacts (described in the Supporting Information). A 150 nm Au top contact was evaporated onto the electrolyte and lift-off was performed using acetone and isopropanol.

2.3. Device Measurements. Electrical measurements were acquired in a dark, nitrogen-filled Cascade Summit 11861 probe station, using an Agilent B1500A semiconductor parameter analyzer. The temperature of the device was controlled by a Temptronic TP03000 temperature controller to within ±0.1 °C. To record temperature-dependent transfer characteristics, we held the samples for 10 min at each target temperature to allow the device to reach thermal equilibrium before the measurement.

To establish an EDL at the interface between the electrolyte and the channel (i.e., to program the device), we first heated the sample to the programming temperature (T_{Pr}) of 100 °C. Because T_{Pr} is higher than the glass transition temperature of the electrolyte (T_g), the ions are mobile and the EDL can be established. While holding the temperature at T_{Pr}, the programming bias (V_{Pr}) was applied to the top gate for 10 min (V_{DS} = 100 mV), driving ions to the surface of the channel and establishing the EDL. The device was then cooled (with V_{Pr} still applied) to 23 °C at a cooling rate of 0.7 °C/min. Because the T_g of the electrolyte is higher than room temperature, the polymer mobility (and therefore ion mobility) is reduced and the device is considered to be programmed. With the EDL "locked" into place at room temperature, the gate bias can be removed while maintaining a static doping density.

Retention time, defined as the time at which a programmed EDL begins to dissipate, was measured using devices fabricated on a graphene/SiC substrate. First, the device was heated to 100 °C and top gate transfer characteristics were taken to locate the Dirac point and record the bias-dependent current values. Next, the device was programmed to V_{Pr} = +2 V while monitoring the drain current (V_{DS} = 100 mV). At time = 0 s, the top gate was grounded, and the I_D measurements continued for 36 h. In one case, V_{DS} = 100 mV was continuously applied, and in another case, V_{DS} = 100 mV was pulsed

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for 10 ms every 10 s. The decay of I_D quantifies the dissipation of the EDL over time.

Sheet carrier density measurements were made on a top-gated van der Pauw device with V_{Pr} = −2, + 2 V. Devices were fabricated on a 1 × 1 cm piece of epitaxially grown graphene on SiC. Contacts (5 nm Ti/145 nm Au) were deposited on the corners via a shadow mask. The electrolyte was deposited using the same method as described above, and a metal top gate (5 nm Ti/145 nm Au) was deposited directly on the electrolyte using a shadow mask. A Nanometrics HL5500PC Hall Effect measurement system was used to quantify the sheet carrier density via the van der Pauw method.[22]

After the programming procedure was completed and the sample was cooled to room temperature, five consecutive measurements were taken within 10 min (this was done two separate times for the +2 V case, and once for the −2 V case). Error was calculated as one standard deviation from the mean of these measurements. The main contribution to the error arises from variations in the quality of the contact between the probes and the device contact pads.

3. RESULTS AND DISCUSSION

To program the device *n*- or *p*-type, the programming temperature, T_{Pr}, must be larger than the glass transition temperature (T_g) of the PVA electrolyte. This ensures that the ions have sufficient mobility to respond to the applied field and establish an EDL. The T_g is measured directly using DSC to set the lower bound for the T_{Pr}. DSC data from the second heating segment of a heat/cool/heat cycle are shown in Figure 1 for

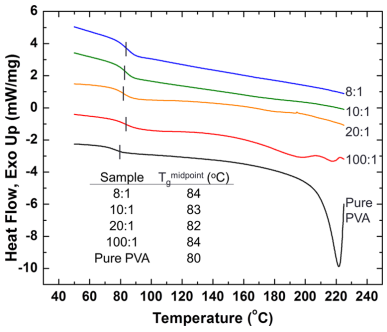

Figure 1. Second heating segments of DSC heat/cool/heat scans for pure PVA and PVA with varying vinyl alcohol to lithium ratios. The midpoints of the glass transitions are indicated with vertical lines on the plot, and the corresponding values are listed in the table. The heating rate is 10 °C/min. Data are offset on the *y*-axis for clarity.

pure PVA along with four electrolytes with varying $LiClO_4$ concentrations, with the transitions corresponding to T_g highlighted by vertical lines. The T_g of pure PVA is 80 °C, which agrees with a previous report.[23] Although the $LiClO_4$ concentration varies over a large range (i.e., vinyl alcohol to lithium ratios from 100:1 to 8:1), all of the corresponding T_g values remain within 4 °C of pure PVA, indicating that the mobility of PVA is not significantly affected by $LiClO_4$. This contrasts PEO-based electrolytes for which the T_g increases from −55 °C for pure PEO to −8.5 °C with an ether oxygen to lithium ratio of 4:1.[19]

The endothermic feature present in the majority of samples shown in Figure 1 at T > 230 °C corresponds to the decomposition temperature (T_d) of the PVA.[24] Therefore, T_g and T_d set the lower and upper bounds for T_{Pr} to between 80 and 225 °C, respectively. T_{Pr} must be sufficiently higher than T_g to establish the EDL, but not too high to thermally degrade the electrolyte. Therefore, 100 °C is chosen as the initial T_{Pr}, meaning that the operating temperature, 23 °C, will be more than 50 °C below T_g. Similar studies using PEO-based electrolytes for "locking" the EDL show that a lock-in temperature that is 20 °C below T_g is sufficient to create a static EDL in the absence of a gate bias.[3,17]

The melting point of pure PVA appears as a well-defined endothermic peak in Figure 1 at T = 225 °C, with a crystal fraction of 0.28. However, the samples containing $LiClO_4$ either show no melting feature, or a weak melting feature in the case of a low salt concentration of 100:1. This result indicates that $LiClO_4$ slows the recrystallization kinetics of PVA to the extent that it does not recrystallize on the time scale of the DSC measurement, similar to what has been shown before for PEO:$LiClO_4$.[25] The recrystallization kinetics are measured and discussed in the Supporting Information. On the basis of these data, the 20:1 concentration is chosen for this study.

When polymer electrolytes are used to explore transport in 2D materials, the deposition of the electrolyte is typically the last processing step and the device is gated by touching the electrolyte surface near the device with the gate probe. This approach can lead to significant differences between measurements on the same device because the probe tip is not anchored onto a contact pad, meaning that the probe shifting over time can change the contact area and physically move the electrolyte in such a way that induces noise in a measurement. Another method is to use a side gate; however, the primary drawback is a longer EDL formation time compared to a top gate because the side gate is often located several microns or tens of microns away from the channel, while a top gate can be located at a distance less than one micron above the channel, providing less resistance and faster ion response. Most polymer-based electrolytes cannot be lithographically processed because they are soluble in the solvents and developers traditionally used in photolithography (e.g., acetone, water, isopropyl, and TMAH-based developers), and as such, a patterned top gate cannot be deposited. PVA:$LiClO_4$, however, is insoluble in these solvents at room temperature. This insolubility permits photolithography and lift-off to be completed directly on the surface of the PVA:$LiClO_4$, thereby enabling a patterned metal top gate to be deposited directly on the electrolyte. Although not demonstrated in this work, an oxygen plasma etch could be utilized to pattern the electrolyte (i.e., the electrolyte not protected by the metal top gate could be removed). Figure 2a is a 3D schematic of the FET device fabricated in this study, which includes the patterned metal top gate (cross-section shown in Figure 2b). Figure 2c is an optical image of a fabricated device on CVD graphene, where the top gate is located on the surface of the electrolyte and the source and drain contact pads are visible underneath the optically transparent electrolyte.

The goal of the first I−V measurements was to confirm that the ions in the electrolyte are immobile at room temperature, and mobile at T_{Pr}. Temperature-dependent transfer characteristics, shown in Figure 3, were taken on a device fabricated on transferred CVD graphene on Si/SiO_2 that has not been previously programmed. For measurements at T = 25 °C (55 °C below T_g), the ions in the electrolyte are immobile, meaning that the electrolyte is simply acting as a thick (∼1 μm) dielectric. As the device temperature increased and approaches T_g, the polymer mobility begins to increase thereby increasing ion mobility. An EDL forms at the electrolyte/channel interface

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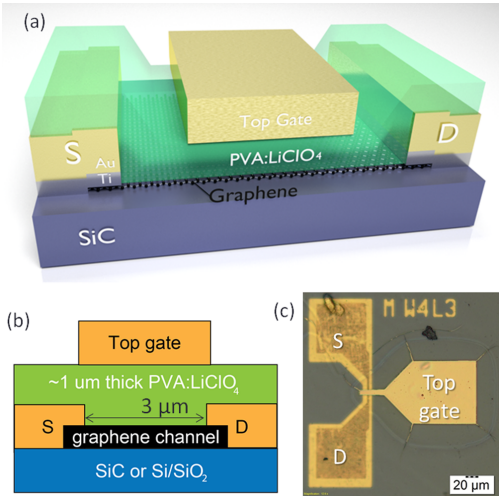

Figure 2. (a) 3D Schematic and (b) cross-section of the electrolyte-graphene FET fabricated for this work and (c) an optical image of a fabricated device using CVD graphene on Si/SiO_2 with a patterned metal top gate deposited on the electrolyte, with the source/drain contacts visible beneath the transparent electrolyte.

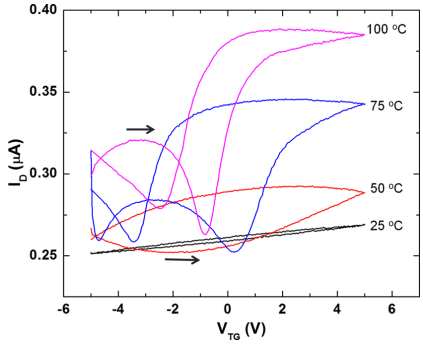

Figure 3. Transfer characteristics of a CVD graphene FET gated with $(PVA)_{20}$:$LiClO_4$ showing an increase in gate control and hysteresis with increasing temperature. V_{DS} = 0.1 V, sweep rate = 0.5 V/s, 10 min between sweeps. Gate leakage is below 10 pA for all points in this measurement.

in response to the applied bias, thereby improving gate control detected as an increase in the drain current with increasing temperature. This is seen in Figure 3 as an increase in current modulation of a CVD graphene FET gated with $(PVA)_{20}$:$LiClO_4$. At V_{TG} = 5 V, the current increases by 0.01, 0.07, and 0.11 μA for 50, 75, and 100 °C, respectively. Because graphene has no bandgap and is semimetallic, the off current is high ($\approx$ 0.25 μA) and the on/off ratio is less than 2 μA at T = 100 °C.

Along with increased gate control, hysteresis increases with temperature as the ions become more mobile (Figure 3). The hysteresis originates from the low polymer mobility at $T < T_g$ and therefore a sluggish response of the ions to the changing gate bias. As the gate bias is swept at 0.5 V/s, the slow ion motion leads to a lag between the applied field and the ion response resulting in two Dirac points: one for the forward sweep direction and a second for the reverse sweep. As the temperature further increases above T_g the hysteresis loop begins to close, and the separation between the two Dirac points decreases. If the ionic mobility were increased, or the top gate sweep rate were reduced to the point where the ions could respond to the field in the sampling time of the instrument, then the hysteresis would be reduced or eliminated.[3]

To measure the sheet carrier density induced by the electrolyte and the mobility of the channel, Hall measurements are made using a gated van der Pauw device. To measure the electron and hole carrier density, the device is programmed using V_{Pr} = ± 2 V. The sheet carrier densities, tabulated in Table 1 (with error equal to one standard deviation and data provided in Table S1), exceed 1×10^{13} cm^{-2} for electrons and 1×10^{14} cm^{-2} for holes, which is comparable to carrier densities reported for similar electrolytes.[4,26] The electron and hole mobilities are also consistent with previous reports for graphene FETs gated with PEO at the same $LiClO_4$ concentration as this study.[18] As expected, the mobility values are low because mobility decreases with increasing n_s because of carrier scattering.[27,28]

Table 1. Sheet Carrier Density and Mobility Acquired via Hall Measurement of a van der Pauw Structure on Epitaxial Graphene on SiC

V_{Pr} (V)	sheet carrier density (cm^{-2})	mobility (cm^2 $V^{-1}s^{-1}$)
+2	$-6.3 \pm 0.03 \times 10^{13}$	443 ± 12
−2	$1.6 \pm 0.3 \times 10^{14}$	41 ± 4.2

After confirming that the sheet carrier densities are large for both electrons and holes, we directly measured the time that the EDL can be retained in a programmed state, defined as the EDL retention time. A $(PVA)_{20}$:$LiClO_4$-gated FET, fabricated on epitaxially grown graphene on SiC, is programmed to V_{Pr} = +2 V at T = 100 °C for 10 min. This long programming time was not optimized for this system, it was simply chosen as a starting point to provide time for the EDL to equilibrate to the maximum drain current, corresponding to the fully established EDL. Under a gate positive bias, an EDL is formed between the Li^+ ions near the channel and the electrons induced in the channel, resulting in n-type doping of the channel. The device is then cooled to room temperature under bias to lock the EDL in place. Following the programming and cooling steps, the top gate is grounded and I_D is monitored as a function of time, shown in Figure 4, superimposed on the transfer characteristics of the device taken previously at T = 100 °C. The drain current remains constant for the first 1000 s, indicating that the full EDL has been retained during this time in the absence of an applied bias.

To quantify the fraction of the EDL that is maintained over time, we normalized the $I_D(t)$ data by the current of the fully dissipated EDL using eq 1. The EDL will be fully dissipated at V_{TG} = 0 V and 100 °C, and therefore the drain current at this voltage, I_0, is first subtracted from the time-dependent $I_D(t)$ data. Next, each data point is divided by the difference in the current between the fully established EDL and the fully dissipated EDL (i.e., $I_D(t = 0) - I_0$). Thus, a value of $I_D^{Norm}(t)$ equal to 1 corresponds to the maximum EDL and 0 corresponds to no EDL.

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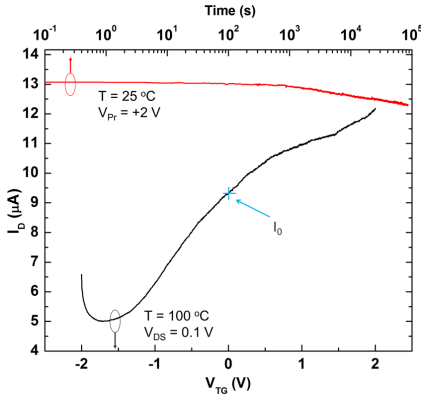

Figure 4. Top gate transfer characteristics of a epitaxial graphene FET on SiC with $(PVA)_{20}$:$LiClO_4$ at T = 100 °C (black trace, bottom axis, 0.5 V/s sweep rate); I_0 is the current at V_{TG} = 0 V which is used in eq 1, identified on the plot with a blue cross. Room-temperature I_D vs time data (red trace, top axis) for the same device following programming (V_{Pr} = +2 V) is also shown, with t = 0 s defined as the time at which the top gate is grounded. V_{DS} = 0.1 V for both cases. Gate leakage is less than 20 pA for all points in this measurement.

$$I_D^{Norm}(t) = \frac{I_D(t) - I_0}{I_D(t=0) - I_0} \quad (1)$$

The normalized data for $(PVA)_{20}$:$LiClO_4$ are plotted in Figure 5 along with normalized data for $(PEO)_{20}$:$LiClO_4$ measured and analyzed in the same way on epitaxially grown graphene FETs.[18] Notice that two types of measurements were made on the PVA devices: the first with a constant V_{DS} = 100 mV applied, and the second with 10 ms pulses of V_{DS} = 100 mV applied every 10 s. The rationale for the pulsed measurements is to verify that Joule heating is not responsible for the dissipation of the EDL. If Joule heating were causing the dissipation, then the continuous measurement, which has 1000x larger power dissipated than the pulsed case, would have a shorter EDL retention time. The results are the same for the continuous and the pulsed measurements and they show that ~75% of the EDL is retained for more than 4 h.

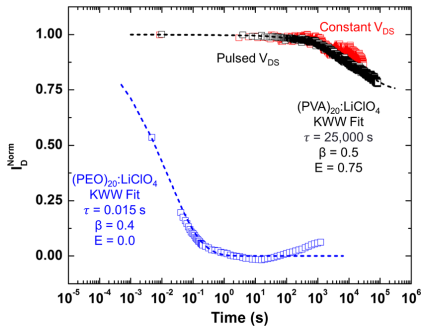

Figure 5. Normalized I_D versus time at room temperature after programming an epitaxial graphene FET on SiC with V_{Pr} = +2 V. All terminals are grounded at time equals zero; therefore, the decay in the data indicates the dissipation of the EDL. Measurements for which V_{DS} is held constant for $(PVA)_{20}$:$LiClO_4$ are shown in red, and pulsed are shown in black. Constant V_{DS} measurements for $(PEO)_{20}$:$LiClO_4$ are shown in blue from Li et al.[18] The PEO and pulsed PVA data are fit to the Kohlrausch–Williams–Watts (KWW) eq 2, indicated by the dashed lines. The KWW fitting parameters are provided on the plot. V_{DS} = 0.1 V for all measurements.

The normalized I_D versus t data can be fit to a stretched exponential equation, Kohlrausch–Williams–Watts (KWW), which is used to describe relaxation in polymers[29]

$$I_D^{Norm} = E + (1 - E)\exp\left[-\left(\frac{t}{\tau}\right)^{\beta}\right] \quad (2)$$

where E is the fraction of the decay that occurs outside the time window of the measurement, τ represents the EDL dissipation time, and β is a stretching parameter which describes the distribution of dissipation times. The stretched exponential fit to eq 2 for both $(PVA)_{20}$:$LiClO_4$ (pulsed data only) and $(PEO)_{20}$:$LiClO_4$[18] are also included in Figure 5 (dashed lines). In contrast to $(PEO)_{20}$:$LiClO_4$, I_D for $(PVA)_{20}$:$LiClO_4$ does not decay to zero in the time window of the measurement because the EDL has not fully dissipated during this time, and therefore E will assume a nonzero value (~0.75). In contrast, the EDL of $(PEO)_{20}$:$LiClO_4$ dissipates on the time scale of milliseconds, and the full decay is captured in the window of the measurement. The stretching exponent, β, is similar for both systems (0.4 to 0.5), indicating a similar distribution of relaxation times. Note that if the data could be described by a single exponential then β = 1, indicating that the EDL dissipates uniformly with a single time constant, τ. A comparison of the transient current data in Figure 5 for $(PEO)_{20}$:$LiClO_4$ and $(PVA)_{20}$:$LiClO_4$ shows that the retention time of the EDL can be increased by 10^6x by increasing the T_g of the polymer by 100 °C.

The retention time demonstrated in this study does not represent a fundamental limit. It is reasonable to conclude that the retention time can be tuned by tailoring the architecture of a polymer electrolyte to tune the T_g. It is also noteworthy to consider that the EDL dissipation times reported here are accelerated because the top gate is grounded during the measurement, effectively discharging the device like a shorted capacitor. If the top gate were floated instead of grounded, the image charges in the gate and channel would continue to attract the oppositely charged ions, and this Coulomb force will extend the lifetime of the EDL. It is possible that this type of floated gate strategy could be integrated into devices that require long EDL dissipation times. It is important to note that the EDL programming/deprogramming approach demonstrated here is not limited to graphene, but can be extended to any 2D material for which charge in the channel can be modulated using an EDL. This includes transition metal dichalcogenides, such as MoS_2 or WSe_2, for which the on/off ratio would be increased by the presence of a band gap.

Although the data presented above show that the PVA-based electrolyte can significantly increase the EDL retention time, the electrolyte is not thermally stable. This result is illustrated in Figure 6 where backgate transfer characteristics on a CVD graphene FET are reported as a function of temperature. The Dirac point shifts to increasingly negative V_{BG} and the current at the Dirac point increases with increasing temperature. The shift in the Dirac point indicates n-type doping, which could result from PVA cross-linking over time. First, because the device is kept in a dry environment during testing and storage,

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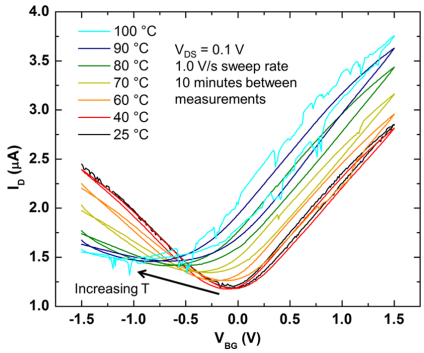

Figure 6. Back gate transfer characteristics of a CVD graphene FET on SiO_2 with $(PVA)_{20}$:$LiClO_4$ at increasing temperatures. The left and upward shift of the Dirac point indicates that *n*-type doping is occurring. Back gate leakage is less than 1 nA for all points in this measurement.

the water content of the film is likely being reduced, especially at higher temperatures. Decreasing water content can promote cross-linking in PVA.[30] Second, a reaction involving the PVA could be occurring at higher temperatures. Because $LiClO_4$ is used as a catalyst in reactions involving alcohols,[31−33] it is possible that similar reactions are occurring in the PVA:$LiClO_4$ film, possibly leading to chemical or physical cross-linking of the PVA. This cross-linking can give rise to phase separation between the polymer and the salt, and pure $LiClO_4$ will heavily dope the graphene *n*-type.[34] The presence of phase separation is supported by FTIR measurements of PVA:$LiClO_4$ films which have been heated to 100 °C, shown in Figure 7a. In agreement with previous reports,[35] these spectra show the signature peaks for PVA, but when the salt is added, they also include a peak at 1630 cm^{-1}, a signature of pure $LiClO_4$.[36] The size of this peak increases with increasing annealing time at T = 100 °C.

To provide more information on whether or not the PVA is being thermally cross-linked, six consecutive DSC heating scans were taken from 25 to 100 °C with a 10 min hold at 100 °C to replicate the conditions in Figure 6. These measurements track the T_g as a function of temperature, and the results are shown in Figure 7b. The first run eliminated thermal history and is therefore not shown in the figure. Scans two through six show that the T_g increases with repeated heat exposure, suggesting that the PVA is thermally cross-linking. In combination, the DSC and FTIR data suggest that the electrolyte cross-linking is driving phase separation between the PVA and the $LiClO_4$, and that the pure $LiClO_4$ is causing irreversible *n*-type doping of the graphene devices. On the basis of the data collected, there is no indication that the cross-linking occurs at room temperature, but is instead thermally activated.

Because this reactivity, as well as the anhydrous cross-linking, are both likely specific to this electrolyte, by selecting a polymer/salt combination that will not have these drawbacks, this issue can likely be overcome. Regardless, this work demonstrates that large sheet carrier densities can be established and maintained for hours at room temperature by choosing an electrolyte with T_g higher than room temperature.

4. CONCLUSION

The EDL retention time of a 2D crystal FET can be increased by increasing the T_g of the electrolyte gate. Specifically, for an EDL with n_s = 6.3 ± 0.03 × 10^{13}, the room-temperature retention time can be increased 10^6x by replacing $(PEO)_{20}$:$LiClO_4$ with $(PVA)_{20}$:$LiClO_4$. The ability to induce ultrahigh charge carrier densities in a 2D device and lock-in the doping for a predetermined time could provide new device functionality that may be useful for novel devices using SPEs. In addition to modulating the retention time, the deposition of a photolithographically patterned gate directly on the electrolyte surface is demonstrated for the first time. Although polymer electrolytes have proven extremely useful for exploring transport in 2D materials, they are frequently gated using a probe tip to touch the surface of the electrolyte near the device, an impractical approach for device application, or using a side gate, which slows the EDL formation. However, the demonstration of a lithographically defined top gate represents an initial step toward practicality. With adequate control of the polymer chemistry to provide sufficient thermal stability to avoid irreversible *n*-type doping, the approach of using "locked" EDLs to store information with the ability to deprogram on

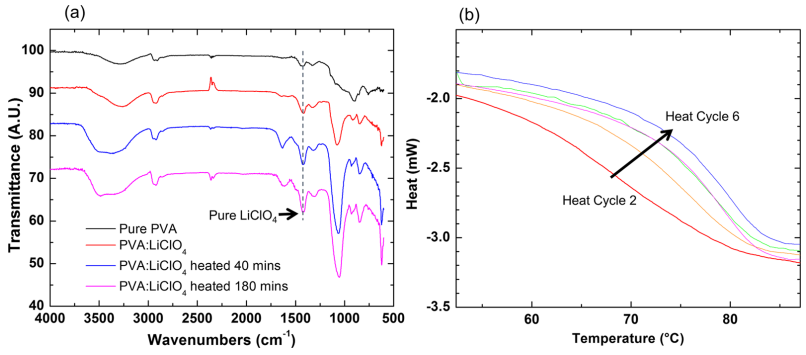

Figure 7. (a) FTIR spectra of $(PVA)_{20}$:$LiClO_4$ (and a pure PVA control), heated to 100 °C for varying times showing the growth of the 1630 cm^{-1} peak, indicating an increase in pure $LiClO_4$ as the sample is heated for longer time periods. (b) Heat scans 2−6 of repeated DSC measurements showing an increase in T_g as a function of heat exposure.

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command or at a specified time represents a new functionality for 2D, EDL-doped transistors.

■ ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acsami.7b03776.

Device channel formation; source/drain deposition; DSC data; Hall data of a programmed device (PDF)

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Notes

The authors declare no competing financial interest.

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Investigation of aging and restoration of polyethylene-oxide cesium-perchlorate solid polymer electrolyte used for ion doping of a WSe_2 field-effect transistor

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Transition metal dichalcogenides (TMDs) are of interest for tunnel field-effect transistors (TFETs) [1]. Their ultrathin body, absence of dangling bonds and native oxides, robustness to short channel effects, dielectric mediated mobilities, and the presence of a band gap are all favorable for use in TFETs. However, doping methods are needed for TMDs to create the *p-n* junction required for the TFET. Charge transfer doping [2] and ion-doping using solid polymers [3] are two approaches being explored. In this paper we show for the first time, the use of polyethylene oxide (PEO) and the salt, $CsClO_4$, to induce both *n* and *p* channel conductivity in exfoliated WSe_2 FETs.

The process flow for the electrolyte-gated WSe_2 FETs began with the exfoliation of the WSe_2 flakes (2Dsemiconductor.com) on 285 nm grown SiO_2. The back gate metal consisted of 5 nm Ti/ 100 nm Au. Source/drain contacts consisted of 1 nm of Ti followed by 90 nm Pd were patterned by electron beam lithography. A 1 wt% solution of $(PEO)_{76}$:$CsClO_4$ was prepared in acetonitrile, drop-casted on the wafer, and annealed for 3 minutes at 90 ˚C in an argon-filled glovebox. Top gate metal consisted of 5 nm Ti followed by 50 nm of Pd evaporated using a shadow mask. Before the top gate metal deposition, the sample was exposed to air.

Device characteristics before and after adding the electrolyte were compared. The electrolyte improved the drain current by more than an order of magnitude for the hole branch, and more than two orders of magnitude for the electron branch. This is due to the formation of an electric double layer at the semiconductor-solid polymer interface, which is the mechanism for charge formation in the TMD. The minimum subthreshold swing after adding the electrolyte was 83 mV/decade. Devices characteristics were initially almost hysteresis free and repeatable.

After storage in air for 44 days the characteristics of the device were observed to degrade, especially in the electron branch, and a significant hysteresis developed even when the characteristics were measured in a vacuum probe station at a pressure of 1.9×10^{-6} Torr. Three repetitions are shown for each measurement, and before each repetition all the contacts were set to 0 V for 4 minutes. In order to recover the device characteristics, the device was annealed at temperatures below (50˚C) and above (75˚C) the melting point of the electrolyte (T_m~60˚C) and cooled to room temperature at 2.5˚C/minute. Vacuum annealing both reduces the water concentration in the electrolyte and increases the crystal fraction. We will present our findings on how device performance can be recovered by vacuum annealing.

We will also discuss how ion doping can be implemented to form the degenerate *p-n* junction in the TMD TFET and lower the resistance of TMD ohmic contacts.

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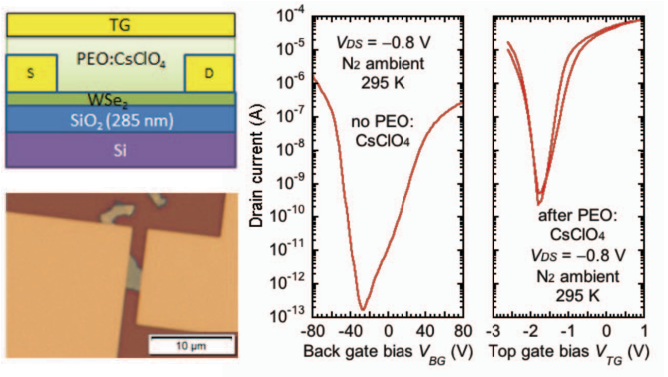

Figure 1: (a) Schematic cross section of a WSe_2 FET with polyethylene oxide (PEO) doped with $CsClO_4$, 1 μm thick. Mobile Cs^+ and ClO_4^- ions in the PEO are used to provide gate-controlled doping of the WSe_2 channel. Optical micrograph of the 11 nm thick and 3.1 μm wide WSe_2 exfoliated flake, and source/drain spacing of 2 μm. Transfer characteristics (b) before, and (c) after PEO:$CsClO_4$ and top gate formation.

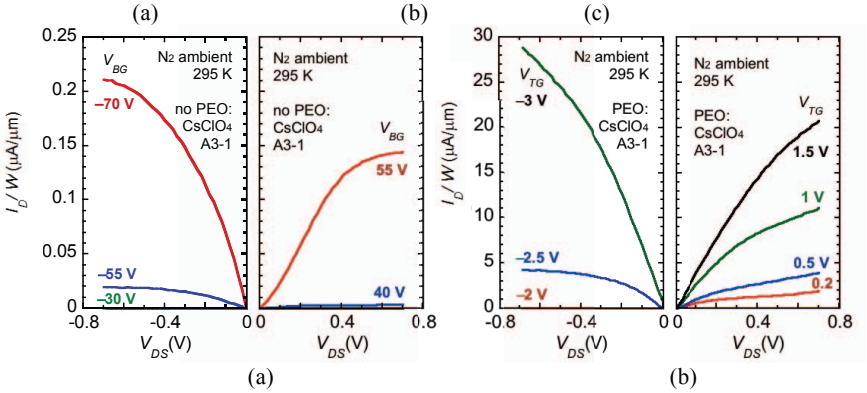

Figure 2: Common source characteristics showing the improved gate electrostatics provided by the solid polymer electrolyte. The current is more than an order of magnitude higher using the (a) PEO:$CsClO_4$ top gate dielectric vs. the (b) SiO_2 back gate dielectric.

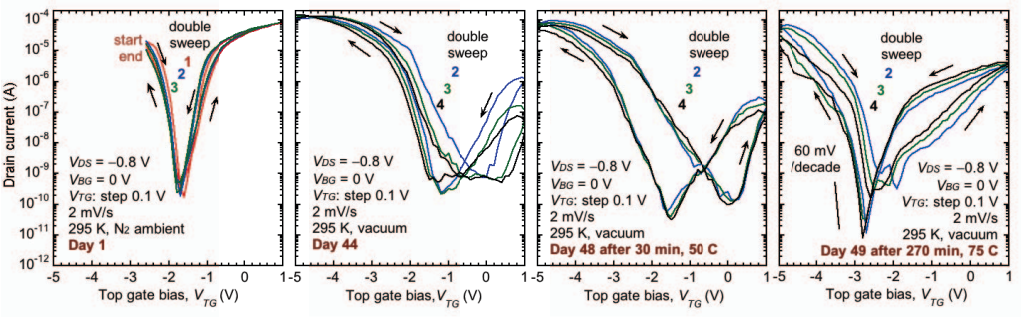

Figure 3: The transfer characteristics of the WSe_2 FET changes after storage in air for 43 days: (a) measurement after PEO:$CsClO_4$ and metal top gate deposition and (b) the same device 44 days later. Although a hysteresis is still present, annealing at 50 and 75 °C (below and above the melting temperature of the electrolyte) begins to restore the transfer characteristic characteristics shown in (c) and (d) respectively. Note the approximately 60 mV/decade subthreshold swing in (d).

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Reconfigurable Ion Gating of 2H-$MoTe_2$ Field-Effect Transistors Using Poly(ethylene oxide)-$CsClO_4$ Solid Polymer Electrolyte

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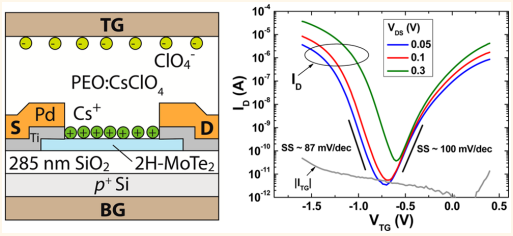
ABSTRACT Transition metal dichalcogenides are relevant for electronic devices owing to their sizable band gaps and absence of dangling bonds on their surfaces. For device development, a controllable method for doping these materials is essential. In this paper, we demonstrate an electrostatic gating method using a solid polymer electrolyte, poly(ethylene oxide) and $CsClO_4$, on exfoliated, multilayer 2H-$MoTe_2$. The electrolyte enables the device to be efficiently reconfigured between *n*- and *p*-channel operation with ON/OFF ratios of approximately 5 decades. Sheet carrier densities as high as 1.6×10^{13} cm^{-2} can be achieved because of a large electric double layer capacitance (measured as 4 $\mu F/cm^2$). Further, we show that an in-plane electric field can be used to establish a cation/anion transition region between source and drain, forming a p−n junction in the 2H-$MoTe_2$ channel. This junction is locked in place by decreasing the temperature of the device below the glass transition temperature of the electrolyte. The ideality factor of the p−n junction is 2.3, suggesting that the junction is recombination dominated.



KEYWORDS: field effect transistor · electrostatic gating · p−n junction · transition metal dichalcogenides · molybdenum ditelluride · polymer electrolyte · poly(ethylene oxide)

Transition metal dichalcogenides (TMDs) are two-dimensional (2-D), atomically thin crystals of broad interest for use in field-effect transistors (FETs),[1−4] tunnel field-effect transistors (TFETs),[2,5−7] and optoelectronic devices.[8−11] There are a growing number of experimental demonstrations of TMD FETs in materials such as MoS_2,[4,12−16] WSe_2,[17−22] and $MoTe_2$.[23−27] For TFETs, TMDs with a narrow band gap such as WSe_2 and $MoTe_2$, are needed to increase current drive.[5,7] Experimental demonstrations of back-gated TMD FETs are now being reported across a wide range of materials, including MoS_2,[12,13,15] WSe_2,[18,19,21] and $MoTe_2$.[23−26] For top gating, ionic liquids have been widely used to facilitate charge control in MoS_2,[16,28−30] WSe_2,[22,31,32] and $MoTe_2$[27] FETs. Solid polymer electrolytes have also been used as top gate dielectrics and applied to, for example, carbon nanotubes,[33,34] graphene,[35,36] MoS_2,[37] and WSe_2.[38] There are no prior reports of solid polymer gating of $MoTe_2$ which is intended here as a reconfigurable doping approach for TFET development.

Bulk 2H-$MoTe_2$ is an indirect band gap material, with a band gap in the range of 0.6 to 1.0 eV.[1,39−41] In monolayer form, a transition to a direct band gap is expected.[6,41] In contrast to the widely studied MoS_2 and WSe_2 FETs, $MoTe_2$-based FETs have gained attention only recently.[23−27] Ambipolar behavior has been reported for multilayer $MoTe_2$ FETs with ON/OFF ratio less than 4 decades,[23,26] and unipolar p-type behavior has been observed with an ON/OFF ratio greater than 6 decades.[24] The reported mobility is in the range of 0.3−20 $cm^2/(V\ s)$ for holes,[23−25,27] and 0.03−30 $cm^2/(V\ s)$ for electrons,[23,27] comparable to other TMDs.[1]

While TMD-based FETs appear promising, doping technologies for TMDs are still in a primitive stage. Traditional doping methods, such as ion implantation, are not

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suitable for atomically thin TMDs. Substitutional doping of MoS_2 with selenium during chemical vapor deposition has been shown to modulate the optical band gap by more than 10%, but transport data is lacking.[42] Nontraditional doping strategies, such as molecular doping and electrostatic doping using electrolytes, are being developed for TMDs.[18,30,43,44] For example, molecular doping using K or NO_2 has been demonstrated in WSe_2, where the doping mechanism is charge transfer between the dopant molecules and WSe_2.[18] A similar strategy using an amine-rich polymer, polyethylenimine, in multilayer MoS_2 led to successful *n*-type doping.[43] Besides molecular doping, electrostatic doping using ionic liquids and polymer electrolytes is an attractive alternative doping method for TMDs, at least for early device exploration.[27−38,44] Recently, by using an external gate voltage to drive ions to the surface of a TMD, ambipolar operation was demonstrated in multilayer MoS_2 using the ionic liquid 1-butyl-1-methyl pyrrolidiniumtris-(pentafluoroethyl)trifluorophosphate $[P14]^+[FAP]^-$.[44] Owing to the high gate efficiency of the electric double layer (EDL) formed at the interface between the electrolyte and WS_2, large n- and p-doping levels up to 9×10^{13} and 3.5×10^{13} cm^{-2}, respectively, have been reported from Hall measurements.[44] The huge charge carrier densities that can be induced by electrolyte gating makes possible the experimental observation of spin splitting in WSe_2.[31] Ionic liquids have been used to create a p−n junction in MoS_2 at 180 K, where the location of the junction can be tuned by the magnitude of the applied source-drain voltage.[30] One advantage of solid polymer electrolytes compared to liquid electrolytes is that a top gate can be evaporated onto the electrolyte surface, and it has recently been shown that poly(ethylene oxide) (PEO) can be patterned using electron-beam lithography.[45]

In the absence of a robust doping technology, we have implemented an ion-doping method based on prior work in organic semiconductors and graphene.[35,36,46] This method is generally applicable to TMD devices and enables reconfigurable n- and p-type doping and the ability to establish p−n junctions. Doping is achieved using a solid polymer electrolyte, PEO and $CsClO_4$, on 2H-$MoTe_2$. Typically, sheet carrier densities on the order of 10^{13} to 10^{14} can be expected due to the large EDL capacitance, ranging from a few to tens of $\mu F/cm^2$.[35,36,46,47] Such high carrier densities are not easy to achieve in normal metal-oxide gate stacks, especially when the channel is based on layered, van der Waals materials, where a high quality oxide is difficult to deposit.[19,48] The thickness of the 2H-$MoTe_2$ in this study is ∼6 nm (∼9 monolayers). While lithium-based salts are appropriate in the extreme case of monolayer TMDs,[37,38] Li^+ can intercalate into multilayer TMDs, degrading the semiconducting property and potentially fracturing the channel due to volumetric changes.[49,50] Therefore, we choose a salt with a large cation, $CsClO_4$, to prevent intercalation.

In this paper, we show that the PEO:$CsClO_4$− gated $MoTe_2$ FET can be efficiently reconfigured between n- and p-channel operation with ON/OFF ratios of 10^5 and subthreshold swings of 90 mV/decade. The formation of an EDL at the interface of the polymer electrolyte and $MoTe_2$ enables us to estimate the band gap energy of few-layer $MoTe_2$ to be ∼0.8 eV. The capacitance of the double layer is measured by a DC method to be ∼4 $\mu F/cm^2$. The extracted field-effect mobilities are 7 and 26 $cm^2/(V\,s)$ for electrons and holes, respectively, while a maximum sheet carrier density of 1.6×10^{13} cm^{-2} is achieved. Finally, taking advantage of the feasibility of the reconfigurable doping, stable p−n junction doping is demonstrated at 220 K.

RESULTS AND DISCUSSION

Prior to applying the electrolyte gate, the transfer and output characteristics of the $MoTe_2$ were measured (Figure 1). A cross-sectional schematic of the back-gated 2H-$MoTe_2$ device is provided in Figure 1a. An AFM image of the device immediately after source/drain fabrication is illustrated in Figure 1b, and a line scan indicates a flake thickness of 5.6 nm, corresponding to 8 monolayers. The surface roughness of the SiO_2 and 2H-$MoTe_2$ are 0.3 and 0.4 nm, respectively. The channel width and length are 1.4 and 1 μm, respectively. The room temperature transfer characteristics of the device are shown in Figure 1c at various source-drain voltages (V_{DS}). The device shows ambipolar behavior with a minimum current at the back gate voltage (V_{BG}) of −25 V. When V_{BG} increases from −25 to 60 V, the drain current (I_D) increases by more than 3 decades, indicating electron accumulation in the channel. When V_{BG} decreases from −25 to −60 V, I_D becomes dominated by holes, as evidenced by increasing I_D. Within the applied V_{BG} range, the ON/OFF ratio of the hole branch is less than two decades, and the electron branch is slightly more than three decades. The output characteristics of the device are shown in Figure 1d, where I_D is a nonlinear function of V_{DS} for both electron and hold branches. This suggests that transport is Schottky-barrier limited in the $MoTe_2$ FET. This also explains the relatively small current at $|V_{DS}| = 2$ V, which is only 300 nA/μm for the electron branch at $V_{BG} = 60$ V and 4 nA/μm for the hole branch at $V_{BG} = -60$ V.

Ion-gating is achieved by depositing PEO:$CsClO_4$ and a metal top gate (TG) onto the same FET presented in Figure 1. The channel can be doped n- or p-type simply by applying voltages of opposite polarity to the top gate. As illustrated by the transistor schematic in Figure 2a, when a positive top gate voltage (V_{TG}) is applied, Cs^+ ions are driven to the surface of the channel, which induce electrons in the $MoTe_2$, doping it n-type. The positive ions and the induced electrons

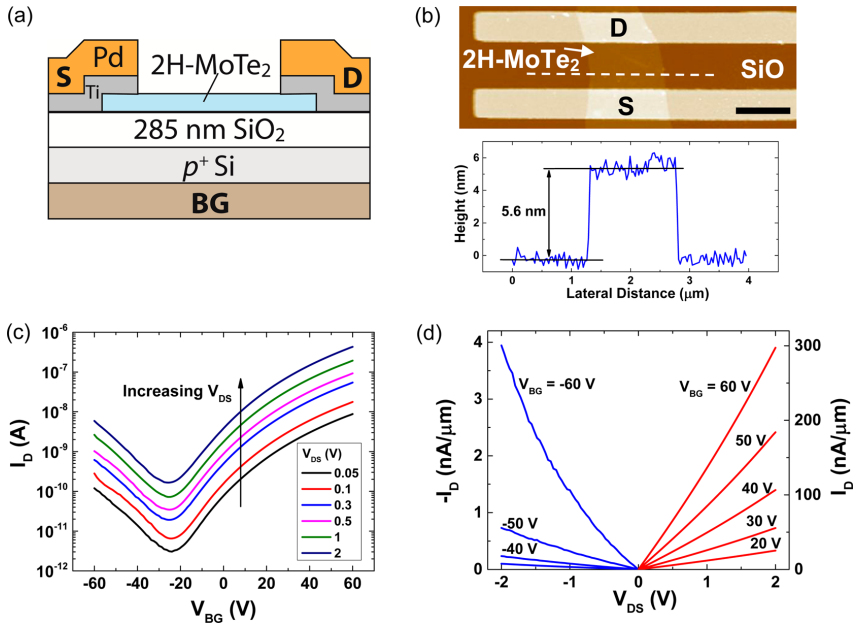

Figure 1. Room temperature current−voltage characteristics of a back-gated 2H-$MoTe_2$ field-effect transistor (FET). (a) Schematic cross section of the FET. (b) Top: AFM scan of the fabricated FET; scale bar, 1 μm. Bottom: AFM line scan corresponding to the white dashed line. (c) Transfer characteristics of the FET shown in (b) at various V_{DS}. (d) Common-source transistor characteristics of the electron (red curves) and hole (blue curves) conduction branches of the same device.

form an EDL, the thickness of which is typically ~1 nm.[44,46,47] Similarly, a p-type channel can be realized by applying a negative V_{TG} where ClO_4^- ions dope the channel and induce holes. The doping level depends on the capacitance of the EDL and the magnitude of the applied V_{TG}.

The transfer characteristics of the ion-gated FET are illustrated in Figure 2b. The source and back gate terminals were grounded. Considering the low mobility of ions in PEO at room temperature,[51] we use a slow sweep rate of 1 mV/s when measuring the ion-gated device at room temperature to provide sufficient time for the ions to respond to the applied field. We determined that 1 mV/s is sufficiently slow by decreasing the sweep rate until the double sweep was essentially hysteresis-free (see Supporting Information). To eliminate any effects from previous measurements, all device terminals were grounded for 5 min between measurements, providing the ions sufficient time to return to equilibrium.

With ion-gating, the ON/OFF ratio increases from a few orders of magnitude to greater than 5 decades for both electron and hole branches. At V_{DS} = 0.05 V, the ON current is ~1 μA for the electron branch at V_{TG} = 0.4 V, and 4 μA for the hole branch at V_{TG} = −1.6 V, while the OFF current is less than 10 pA. The subthreshold slopes (SS) are 100 and 87 mV/decade for the electron and hole branches, respectively. Multiple ion-gated devices were measured and all showed similar behavior. These SS swing values are smaller than those reported by Lezama and co-workers for an ionic liquid-gated $MoTe_2$ FET (140 mV/decade for electrons and 125 mV/decade for holes) and show significantly smaller hysteresis over a comparable voltage range and sweep rate.[27]

Compared to the back-gated device without the electrolyte (Figure 1), the ON current and the ON/OFF ratio in the ion-gated device are two decades larger for the electron branch and four decades larger for the hole branch at V_{DS} = 0.05 V. The strong current modulation with the top gate implies that the EDL was formed at the interface of the electrolyte and the $MoTe_2$ channel. Figure 2c,d shows the common source characteristics (I_D−V_{DS}) at various V_{TG} for the electron and hole branches, respectively. Drain current increases linearly with drain-source voltage and then gradually saturates. The saturation current is ~3.6 μA/μm at V_{TG} = 0.4 V for the electron branch and 7 μA/μm at V_{TG} = −1.6 V for the hole branch. The I_D−V_{DS} relation is similar to the Si MOSFET, where current is limited by thermal emission over an energy barrier at the source end of the channel. This can be expected in the top-gated devices due to the small (~1 nm) electrostatic length resulting from the ion doping.[33,44] The large induced sheet carrier density at the source/drain end increases the tunnel current in the Schottky barriers

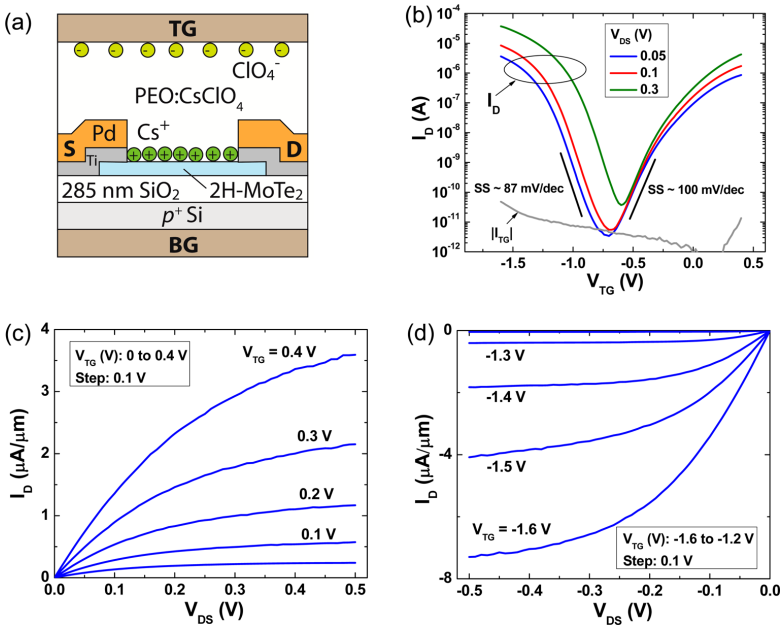

Figure 2. Room temperature current−voltage characteristics of a PEO:CsClO$_4$ solid polymer electrolyte-gated 2H-MoTe$_2$ FET. (a) Schematic device cross section. (b) FET transfer characteristics showing drain current *vs* top-gate voltage at various supply voltages. The gate leakage current (I_{TG}) is measured at the top gate. The two solid black lines show the subthreshold swings for the electron and hole branches, respectively. Common-source transistor characteristics are shown for the electron branch in (c) and the hole branch in (d).The back gate was grounded and the sweep rate was 1 mV/s.

resulting in nearly ohmic transport for both electrons and holes. Thus, transport inside the channel mainly limits the current in the top-gated $MoTe_2$ transistor. This is very different from the back-gated device of Figure 1, where the current is limited by thermionic emission through the Schottky barriers. To quantitatively capture the difference, it is instructive to compare the electrostatic length (λ) in the two systems, which describes the extension of the electric field lines from the source/drain contacts into the channel region.[52,53] In a planar structure, λ is quantified as $\lambda = (\varepsilon_{CH}\, t_{CH}\, t_{OX}/\varepsilon_{OX})^{1/2}$,[52,53] where ε_{CH} is 12 for the $MoTe_2$ channel,[54] and t_{CH} of the $MoTe_2$ is 5.6 nm as measured by AFM. For the electrostatic double layer the $t_{OX} = t_{EDL} \cong 1$ nm and $\varepsilon_{OX} = \varepsilon_{EDL} = 5$.[33,51] On formation of the EDL using the top gate, $\lambda = 3.7$ nm; however, using the electrostatic doping from the back-gated FET, $\lambda =$ 62 nm, with $\varepsilon_{OX} = 3.9$ and $t_{OX} = 285$ nm; this is more than 18 times larger than in the top-gated FET. As a result, we may expect thick Schottky barriers in the back-gated $MoTe_2$ transistors with 285 nm SiO_2, and thin barriers for easier electron tunneling in the top-gate devices with an EDL.

We also highlight the distinct difference between the transfer characteristics of the two systems in the subthreshold region of the electron branch. At the same positive V_{DS} values of 0.05, 0.1, and 0.3 V, the drain currents for the top-gated FET overlap in the subthreshold region (Figure 2b), while I_D increases exponentially as a function of V_{DS} in the back-gated device (Figure 1b). This difference may also be explained by the different transport mechanisms in the two devices. In the top-gated case, because the channel length of 1 μm is much larger than the natural length ($\lambda \sim 3$ nm), short-channel effects can be excluded, and thus the overlap is expected for V_{DS} larger than a few k_BT/q (~26 mV at room temperature),[55] where k_B is Boltzmann constant and T is absolute temperature. However, in the back-gated case, the current is mainly limited by back-to-back Schottky barriers, where V_{DS} mainly drops at the barriers instead of the channel region. When V_{DS} increases from 0.05 to 2 V, as shown in Figure 1c, the Schottky barrier height at the drain end becomes lower, and the Schottky barrier at the source end becomes thinner. Thus, larger I_D is expected with larger V_{DS} whether the device is in the subthreshold region or the ON region.

The strong ambipolar behavior shown in Figure 2b suggests that the Fermi level in the energy band diagram was shifted from the valence band edge to the conduction band edge when the gate voltage was swept from −1.6 to 0.4 V. The I_D-V_{TG} curve in Figure 2b is shown on a linear scale in Figure 3a. The V_{TG} of the OFF state ranges from −1.1 to −0.1 V, indicating the

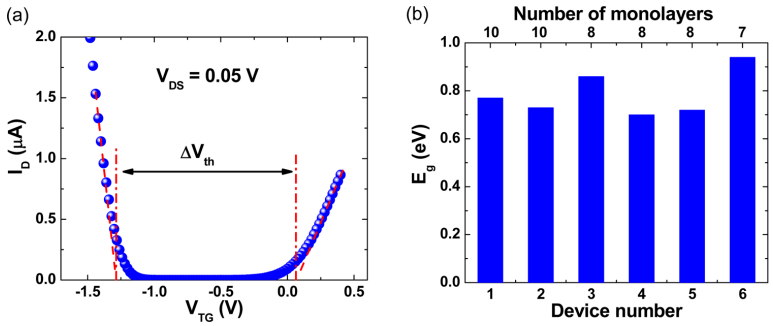

Figure 3. Quantitative determination of the band gap (E_g) of 2H-$MoTe_2$. (a) Linear scale plot of the I_D−V_{TG} transfer curve as shown in Figure 2b. The intersection points of the red dashed lines with the *x* axis indicate the threshold voltages, $V_{th,p}$ and $V_{th,n}$, of the hole and electron branches, respectively. (b) Computed band gap for six devices, with an average of 0.8 eV. The band gap for each device was calculated based on ΔV_{th} in (a).

band gap of the channel material. Following previous studies,[34,44] we estimate the band gap energy (E_g) of the 2H-$MoTe_2$ using the empirical formula $E_g = aq\Delta V_{th}$.[34] Here, q is the electronic charge and $\Delta V_{th} = \Delta V_{th,n} - \Delta V_{th,p}$, where $V_{th,n}$ and $V_{th,p}$ are the threshold voltages of the electron and hole branches, respectively. These values are highlighted by the dashed lines in Figure 3a. The parameter α is defined as $\alpha = SS_{60}/SS_M$, where SS_{60} is the subthreshold slope at the thermal limit (60 mV/decade at room temperature), SS_M is the measured subthreshold slope of the device. A SS_M of 94 mV/decade is extracted from the transfer characteristics in Figure 2b by averaging the electron and hole subthreshold swings, giving an α value of ∼0.64. With ΔV_{th} = 1.35 V extracted from Figure 3a, this yields $E_g \sim 0.86$ eV at room temperature. The E_g values for six devices are shown in Figure 3b. The $MoTe_2$ flake thicknesses of devices 1 to 6 are 7.0, 7.0, 5.6, 5.6, 5.6, and 5.0 nm, respectively (devices 3, 4, and 5 were fabricated on the same flake), corresponding to 10, 10, 8, 8, 8, and 7 monolayers. The extracted E_g ranges from 0.70 to 0.94 eV with an average of 0.8 eV, and this result agrees well with previous theoretical studies,[6,39−41] and a recent experimental report of $MoTe_2$ gated with an ionic liquid.[27] It has been reported that E_g increases weakly within 4−6 monolayers, and increases strongly below 3 monolayers (*i.e.*, ≤ 2 nm).[11,56,57] Considering our flake thickness, we expect the E_g reported here to be similar to that of the bulk $MoTe_2$ crystal. We noticed that E_g extracted from the device fabricated on a 5 nm thick $MoTe_2$ flake (7 monolayers) is 0.94 eV, which is slightly larger than those extracted from devices with 6 or 7 nm thick flakes. This may be a result of the quantum confinement effect; however, considering the fluctuations in E_g for devices built with flakes of similar thickness, more devices must be measured to confirm this conclusion.

As discussed above, one of the advantages of ion-gating is the strong gate coupling due to the large C_{EDL}, which can range from a few to tens of μF/cm^2. Here we determine C_{EDL} with a DC measurement. A map of I_D for various V_{TG} and V_{BG} is plotted on a logarithmic scale in Figure 4a. The data were measured by fixing V_{BG} at one value while sweeping V_{TG} with V_{DS} fixed at 0.05 V. For a given V_{BG}, the electron and hole conduction branches appear at the right and left sides of the conduction minimum respectively, where the minimum is indicated by the dark regions. The location of the minima in V_{TG} is a function of V_{BG}. Specifically, the conduction minimum shifts to more negative V_{TG} values as the V_{BG} becomes more positive. The extent of the shift along the V_{TG} axis is almost linearly proportional to the V_{BG} applied, as shown in the bottom plot of Figure 4a for different current levels for electron and hole branches. The triangles and the squares are experimental data and the solid lines represent a linear fit to each set of experimental data with the same current. The slopes of the solid lines (*i.e.*, $\Delta V_{BG}/\Delta V_{TG}$) are 370, 360, 305, and 316 from the left green curve to the right blue curve, giving an average of 338. For the double-gated device with a thin channel and thick back gate oxide, this ratio can be used to calculate the capacitance of the electric double layer (C_{EDL}) as $C_{EDL}/C_{OX} = -\Delta V_{BG}/\Delta V_{TG}$.[58,59] Using ε_{OX} = 3.9 and t_{OX} = 285 nm, C_{OX} is 0.0121 μF/cm^2, giving C_{EDL} of ∼4 μF/cm^2. Using the parallel-plate capacitor model and assuming the relative dielectric constant of the electrolyte is 5,[51] the thickness of the EDL (t_{EDL}) is estimated as 1 nm. The extracted C_{EDL} and t_{EDL} agrees well with previous studies.[33,35,47]

The C_{EDL} and the transfer characteristics can be used to extract the field-effect mobility, μ_{FE}, above threshold $\mu_{FE} = (1/C_{EDL})\partial\sigma/\partial V_{TG}$,[24] where σ is the conductivity of the channel, defined as $\sigma = (L/W)\, I_D/V_{DS}$ and L and W are the length and width of the channel, respectively. The dependence of σ on V_{TG} is shown in the inset of Figure 4b, and the extracted μ_{EF} is shown in the main panel. The maximum μ_{FE} is 7 cm^2/(V s) for electrons and

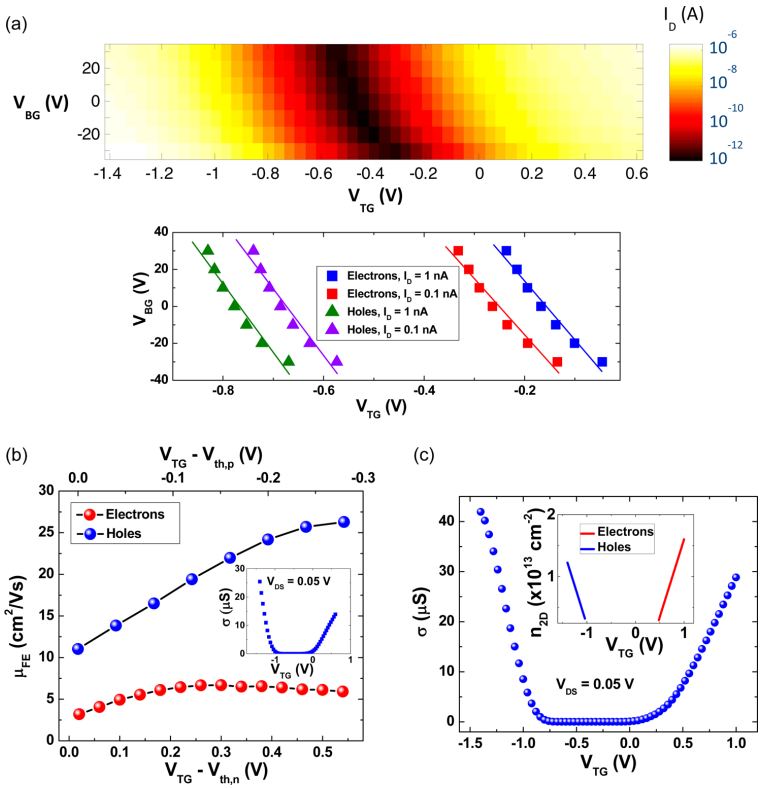

Figure 4. Quantitative determination of the electric double layer (EDL) capacitance, $MoTe_2$ channel field-effect mobility, and sheet carrier density. (a) Top: Drain current map at various top gate and back gate voltage plotted on a logarithmic scale for a supply voltage of 0.05 V and a sweep rate of 1.3 mV/s. Bottom: Linear fit (solid lines) of the experimental data (squares and triangles) at fixed drain current. (b) Field-effect mobility as a function of top gate voltage above threshold for electrons (red spheres) and holes (blue spheres) respectively. Inset: Channel conductivity as a function of top gate voltage measured at V_{DS} = 0.05 V and V_{BG} = 0. (c) Conductivity as a function of top gate voltage for another FET measured over a larger top gate voltage range. The inset shows the estimated sheet density as a function of top gate voltage for electrons (red curve) and holes (blue curve) above threshold.

26 $cm^2/(V\,s)$ for holes, similar to a recent study on few-layered 2H-$MoTe_2$ transistors gated with thermal SiO_2[24] and an ionic liquid.[27]

Figure 4c shows σ measured in another device with a relatively larger V_{TG} range from −1.4 to 1.0 V. Channel conductivity increases with $|V_{TG}|$ and reaches 29 μS at V_{TG} = 1.0 V for the electron branch and 42 μS at V_{TG} = −1.4 V for the hole branch. Assuming a constant C_{EDL} throughout the entire V_{TG} range, the sheet charge carrier density (n_{2D}) in the channel well above the threshold voltage may be estimated as, $n_{2D} = C_{EDL}|V_{TG} - V_{th}|/q$.[60] As reported in the inset of Figure 4c, the maximum doping level of the electron branch is 1.6×10^{13} cm^{-2} at V_{TG} = 1.0 V, and the hole branch is 1.2×10^{13} cm^{-2} at V_{TG} = −1.4 V.

The ion-gating technique makes it feasible to build 2D devices with different doping polarity and doping levels; however, as shown above, both the doping polarity and level depend on the applied external voltages and are sensitive to the top gate, drain/source, and back gate voltages. Moreover, slow sweep rates are required to drift the ions into place. What is needed is the ability to drive the ions to the surface of the $MoTe_2$ using an applied field, and "lock" them into place at the surface so that fast voltage sweep rates can be used to measure the drain current. This can be achieved by driving the ions to the surface of the $MoTe_2$ and quenching the device to a temperature lower than the glass transition temperature (T_g) of the solid polymer electrolyte (see Supporting Information, Figure S2). When temperature is less than T_g, the polymer chains are kinetically arrested and the polymer relaxation times become large. Because ion mobility is strongly coupled to polymer mobility, the ionic conductivity through the polymer becomes negligibly small (~10^{-12} S/cm).[61] Consequently, the EDL is locked

into position at the $MoTe_2$ interface, and the doping polarity and doping level become fixed and are no longer controlled by the top gate. However, top gate control is recovered after the sample is heated to room temperature, and the transfer characteristics become identical to those prior to quenching, demonstrating that no irreversible changes occurred to the device (see Supporting Information, Figure S5).

In addition to unipolar doping where either cations or anions are driven to the surface of $MoTe_2$, we use this technique to create p−n junction doping where both cations and anions are driven to the surface.[30] The specific case of the p−n junction doping is illustrated by the process flow in Figure 5a (A−D). In this device, we replaced the thick SiO_2 dielectric used above with 27 nm of Al_2O_3 grown by atomic layer deposition (ALD), because the thinner high-k dielectric offers better gate control over the channel. Also, the two-contact devices presented above were replaced with a four-terminal contact structure to allow the contact resistance to be extracted.

Both unipolar doping and p−n junction doping can be simultaneously achieved in separate regions of the device by the selection of terminal biases. Schematic A shows a four-contact device covered by PEO:$CsClO_4$ under thermal equilibrium at room temperature. No external voltage is applied and the ions are homogeneously distributed. Here, instead of using the top-gate bias to drive the ions, we can uniformly bias the top 4-terminals with respect to the back gate for unipolar doping or ground the back gate and apply a drain/source bias to form a p−n junction. In Schematic B, terminals 2 and 3 are biased at room temperature with positive voltage (+V) and negative voltage (−V) respectively, the back gate is grounded, and terminals 1 and 4 are floated. Under these bias conditions, negative ions will accumulate near terminal 2 and positive ions near terminal 3. As a result, the channel region close to terminal 2 becomes p-type doped while the channel region close to terminal 3 becomes n-type doped. A p−n junction is expected between terminals 2 and 3. In Schematic C, the device is quenched to 220 K, which is 24 K below the T_g of the polymer. The bias condition in Schematic B is maintained during quenching until 220 K is reached.

An AFM image of the four-terminal device on Al_2O_3/Si is shown in Figure 5a-D, where the flake thickness is 6 nm and the channel width is ∼3.8 μm. The distance between terminals 1 and 4 is 2 μm, and terminals 2 and 3 are positioned such that the channel is divided into three regions of equivalent length (∼0.6 μm). Before depositing the electrolyte, we measured the room temperature $I-V$ and extracted a source resistance of 5.5 k$\Omega\cdot\mu$m using the four-probe method (see the Supporting Information for details). The source resistance is the contact resistance plus the series resistance originating from the interlayer transport.[62]

The device characteristics for the condition corresponding to Schematic A (*i.e.*, homogeneous ion distribution with no applied bias) are shown in Figure 5b. Here, the device temperature has been reduced to 220 K. The drain-to-source voltage was applied between terminals 1 and 4, with terminals 2 and 3 floating. The device shows ambipolar behavior with a linear I_D-V_{DS} relationship at low V_{DS} and saturating behavior at large V_{DS} for both electron and hole branches. The ON current is about 0.6 μA/μm for both electron and hole branches at V_{BG} of 4 and −6 V, respectively. The inset shows the transfer characteristic of the same device with electron and hole branches distributed almost symmetrically around V_{BG} of −1 V. These data suggest that the Fermi level lies close to the middle of the energy band gap at a back-gate bias of approximately −1 V.

The device characteristics obtained after the doping and quenching process described in Figure 5a are illustrated in Figure 5c. Here, 1.5 and −1.5 V are applied to terminals 2 and 3 during the quenching process, yielding p-type doping in the channel between terminals 1 and 2, and n-type doping between terminals 3 and 4 (Schematics B and C). The ON current in both n- and p-type channels exceeds 50 μA/μm, and the conductivity is more than two decades larger than the device without ion doping at a similar back gate voltage.

I_D as a function of V_{DS} in Figure 5d shows the $I-V$ characteristics of the four top-surface terminals for four combinations of terminals. The carrier transport from terminal 2 to 3 shows rectifying behavior, indicating a p−n junction in the channel between terminals 2 and 3 as anticipated from Figure 5a, Schematic C. The same behavior is also measured when V_{DS} was biased between the two most outer terminals, 1 and 4, as would be expected. Contact pairs 1−2, and 3−4 are ohmic because the ion doping increases the tunneling transparency of the Schottky contacts. The rectifying behavior shown in Figure 5d is therefore due to the formation of a p−n junction and not due to a Schottky barrier.

To simplify further discussion, we label the device with V_{DS} biased at terminals 1 and 4 as diode A, and the one with V_{DS} biased at terminals 2 and 3 as diode B. Figure 5e shows the I_D *versus* V_{DS} on a logarithmic scale for diodes A and B. The forward bias current increases rapidly with V_{DS}, giving a slope of 100 mV/decade when V_{DS} increases from 0.4 to 0.7 V. The theoretical limit for a diode limited by thermal transport is ln(10) k_BT/q. This yields 44 mV/decade at 220 K. The p−n junction current in bulk semiconductors is given by $I = I_0[\exp(qV/\eta k_BT) - 1]$,[55] where, I_0 is the reverse saturation current and η is the diode ideality factor. For $\eta = 1$, the current is diffusion current dominated, while for $\eta = 2$, the current is limited by recombination.[55] In our device, η is ∼2.3, suggesting that

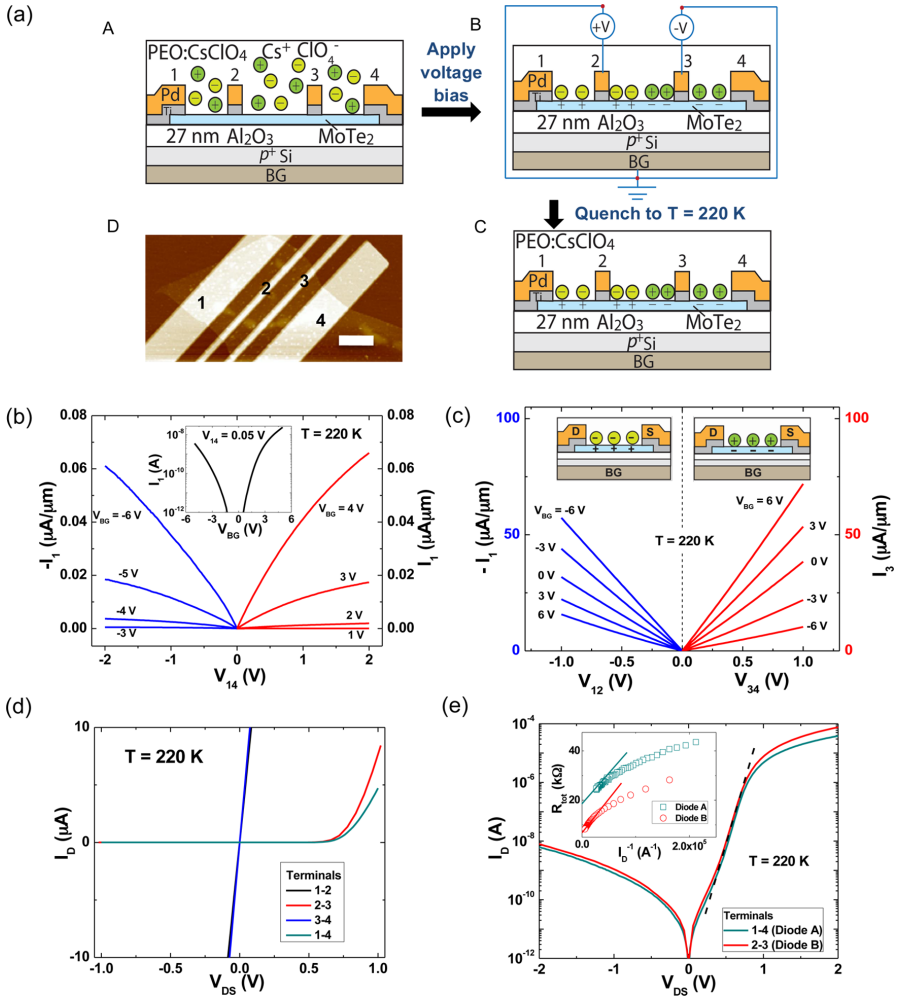

Figure 5. Unipolar doping and p−n junction formation using PEO:$CsClO_4$ solid polymer electrolyte at 220 K. (a) Mechanism for p−n junction formation. (A) In thermodynamic equilibrium the ions are homogeneously distributed. (B) Terminals 2 and 3 are connected to sources that set plus and minus DC voltages with respect to the back gate, with terminals 1 and 4 floating. Ions redistribute in the electric fields of the contacts to reach the steady state configuration shown. (C) The ions are locked into place by quenching the device to 220 K. (D) AFM scan of the device before depositing PEO:$CsClO_4$. Scale bar: 1 μm. (b) Common-source characteristics measured at 220 K without ion gating (*i.e.*, by locking in the homogeneous distribution as shown in (a), Schematic A. Inset: the corresponding transfer characteristics. (c) Common-source characteristics measured between terminals 1 and 2 and between 3 and 4 with the other terminals floating. (d) Current−voltage characteristics on the indicated terminal pairs with the unconnected pairs floating, note that 1−2 and 3−4 are ohmic. (e) Semilog plot of the p−n junction *I*−*V* characteristic. V_{DS} was applied between terminals 2 to 3 and 1 to 4, respectively. The dashed line indicates the ideality factor. Inset: Total differential resistance (R_{tot}) as a function of I_D^{-1}. The *y*-axis intercept indicated by the solid lines suggests the series resistance of the diode.

recombination is significant in the $MoTe_2$ p−n junction. The forward bias current is about 40 and 80 μA at V_{DS} of 2 V for diodes A and B, respectively. The reverse current increases gradually with $|V_{DS}|$ and reaches ~2.6 nA/μm at V_{DS} = −2 V, which is significantly larger compared to previous reports for monolayer WSe_2 (less than 0.05 nA/μm at the same V_{DS} of −2 V).[10] This may be partially due to the smaller band gap of $MoTe_2$ compared to monolayer WSe_2. Pronounced roll-off of I_D was observed when V_{DS} increases beyond 0.8 V due to the series resistance in the diode. Several methods can be used to extract the series resistance.[63] Here, we use the Werner method,[63,64] where, at large forward bias condition ($I \gg I_0$), the

$I-V$ relation for a diode including series resistance (R_S) $I = I_0[\exp[q(V - IR_S)/\eta k_B T] - 1]$ can be rewritten as $R_{tot} = k_B T/q\eta I^{-1} + R_S$. Here, R_{tot} is the differential resistance of a diode defined as $R_{tot} = dV/dI$, V is the drive voltage applied across the diode and I is the current of the diode. The y-axis intercept of the $R_{tot}-I^{-1}$ plot (inset of Figure 5e) suggests R_S, which is 18 and 7 kΩ for diodes A and B, respectively.

CONCLUSION

In summary, an electrostatic gating method using a solid polymer electrolyte, PEO:$CsClO_4$, on 2H-$MoTe_2$ is demonstrated for the first time. The electrolyte enables efficient reconfiguration of the device between n-channel and p-channel operation with n- and p-doping levels up to 1.6×10^{13} and 1.2×10^{13} cm^{-2} at room temperature. Such high doping levels are promising for the future demonstration of tunnel field-effect transistors (TFETs), and the study of spin-splitting and superconducting TMDs. The band gap energy of $MoTe_2$ (7−10 monolayers) is quantitatively estimated to be ∼0.8 eV, in good agreement with theoretical predictions. The field-effective mobility is extracted as 7 and 26 $cm^2/(V\ s)$ for electrons and holes at room temperature, respectively, which is comparable to other TMDs such as MoS_2 and WSe_2. By quenching the device to 220 K, stable unipolar and p−n junction doping is realized. The ideality factor of the junction is 2.3, suggesting that the p−n junction is recombination dominated.

METHODS

2H-$MoTe_2$ was mechanically exfoliated from either powder or crystal using the Scotch tape method. $MoTe_2$ from powdered exfoliation (99.9% American Elements) was used to construct the 2-terminal devices, while $MoTe_2$ exfoliated from the bulk crystal (2d Semiconductors, Inc.) was used for the 4-terminal devices. The flakes were transferred onto a highly p-doped Si substrate with 285 nm of thermal SiO_2. The flake thickness, measured by atomic force microscopy (AFM), ranged from 5−7 nm, or 7−10 monolayers assuming a monolayer thickness of 0.7 nm.[39] Source and drain contacts of Ti (1 nm)/Pd (60 nm) were deposited by electron-beam lithography and electron-beam evaporation, followed by lift-off in acetone at room temperature.

To prepare the ion gate, PEO (molecular weight 95 000 g/mol, Polymer Standards Service) and $CsClO_4$ (99.999%, Sigma-Aldrich) were dissolved in anhydrous acetonitrile (Sigma-Aldrich) with a solution concentration of 1 wt % and a PEO ether oxygen to Cs^+ molar ratio of 76:1. The solution was drop-cast onto the back-gated $MoTe_2$ devices under ambient conditions, followed by a 3 min anneal at 90 °C on a hot plate in air. The thickness of the cast electrolyte was ∼1 μm, measured by AFM. To prepare the top metal gate, 50 nm of Pd was evaporated onto the solid PEO:$CsClO_4$ film using a shadow mask and electron-beam evaporation. An optical image of the top-gated device is provided in the Supporting Information.

Electrical characterization was performed using a Cascade Microtech PLC50 Cryogenic vacuum probe station at $\sim 10^{-5}$ Torr. Because PEO-based electrolytes can absorb as much as 10 wt % water under ambient conditions,[65] the sample was annealed under vacuum at 350 K for 3 min. To facilitate the removal of water by increasing the polymer mobility, the annealing temperature was chosen to be ∼20 degrees larger than the melting temperature (T_m) of the PEO:$CsClO_4$. The T_m (58 °C) and T_g (−29 °C) of the polymer electrolyte were measured by differential scanning calorimetry, and the data are provided in the Supporting Information. After annealing, the heater was turned off and the temperature decreased to room temperature over 4 h.

Conflict of Interest: The authors declare no competing financial interest.

Supporting Information Available: Optical image of the top-gated device; DSC measurement of PEO:$CsClO_4$ melting and glass transition temperatures; transfer characteristics of the top-gated device at varying sweep rate; room temperature electrical characteristics of the back-gated FET; transfer characteristics of the electrolyte-gated FET before and after quenching. This material is available free of charge *via* the Internet at http://pubs.acs.org.

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ARTICLE

Monolayer Solid-State Electrolyte for Electric Double Layer Gating of Graphene Field-Effect Transistors

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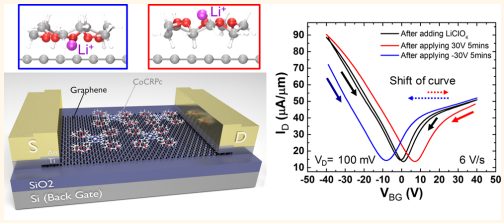
Supporting Information

ABSTRACT: The electrostatic gating of graphene field-effect transistors is demonstrated using a monolayer electrolyte. The electrolyte, cobalt crown ether phthalocyanine (CoCrPc) and $LiClO_4$, is deposited as a monolayer on the graphene channel, essentially creating an additional two-dimensional layer on top of graphene. The crown ethers on the CoCrPc solvate lithium ions and the ion location is modulated by a backgate without requiring liquid solvent. Ions dope the channel by inducing image charges; the doping level (*i.e.*, induced charge density) can be modulated by the backgate bias with the extent of the surface potential change being controlled by the magnitude and polarity of the backgate bias. With a crown ether to Li^+ ratio of 5:1, programming tests for which the backgate is held at $-V_{BG}$ shift the Dirac point by ~15 V, corresponding to a sheet carrier density on the order of 10^{12} cm^{-2}. This charge carrier density agrees with the packing density of monolayer CoCrPc on graphene that would be expected with one Li^+ for every five crown ethers (at the maximum possible Li^+ concentration, 10^{13} cm^{-2} is predicted). The crown ethers provide two stable states for the Li^+: one near the graphene channel (low-resistance state) and one ~5 Å away from the channel (high-resistance state). Initial state retention measurements indicate that the two states can be maintained for at least 30 min (maximum time monitored), which is 10^6 times longer than polymer-based electrolytes at room temperature, with at least a 250 Ω μm difference between the channel resistance in the high- and low-resistance states.



KEYWORDS: *ion gating, electric double layer, two-dimensional, electrolyte, field-effect transistor, graphene, phthalocyanine*

Two-dimensional (2D) crystals, including graphene and transition metal dichalcogenides (TMDs), are layered materials that are a single atom (*e.g.*, graphene) or molecule thick. The ultrathin body and electrical properties of 2D crystals[1,2] have motivated potential applications in field-effect transistors (FETs)[3,4] and electroluminescent devices;[5] however, for 2D materials to be used in these devices, doping methods are needed. The most common doping strategies for 2D crystals are charge transfer and electrostatic doping with ions. Charge transfer doping relies on the transfer of electrons resulting from the molecular physisoption or chemisorption of dopants on 2D crystals. For example, WSe_2 can be p-type doped by the adsorption of NO_2 and subsequent transfer of one electron from WSe_2 to NO_2.[6] Similarly, potassium[7] and benzyl viologen[8] can transfer one electron to MoS_2 and generate n-type doping in MoS_2. One aspect of this method is that after functionalizing the 2D crystal the doping density is permanent and cannot be modulated during device operation.

In contrast to charge transfer doping, electrostatic doping/gating with ions permits adjustable doping densities and doping types without charge transfer between the 2D crystal and the dopant. For example, reconfigurable ambipolar doping/gating has been demonstrated using electrolytes in many 2D materials including graphene, $MoTe_2$, WSe_2, WS_2, and black phosphorus.[4,9−11] Herein we will refer to ion gating as the process of using a gate to dynamically control the movement of ions, whereas ion doping will be used to refer to the condition where ions are stabilized on a surface in the absence of a gate bias. The electric double layer (EDL) that forms at the interface between the electrolyte and the semiconductor induces image charges in the channel and provides high gate capacitance (*e.g.*, 30 $\mu F/cm^2$ at 1 Hz between an ionic liquid and ZnO[12]) and high charge carrier density (*e.g.*, ~10^{14} cm^{-2} for both electrons and holes in

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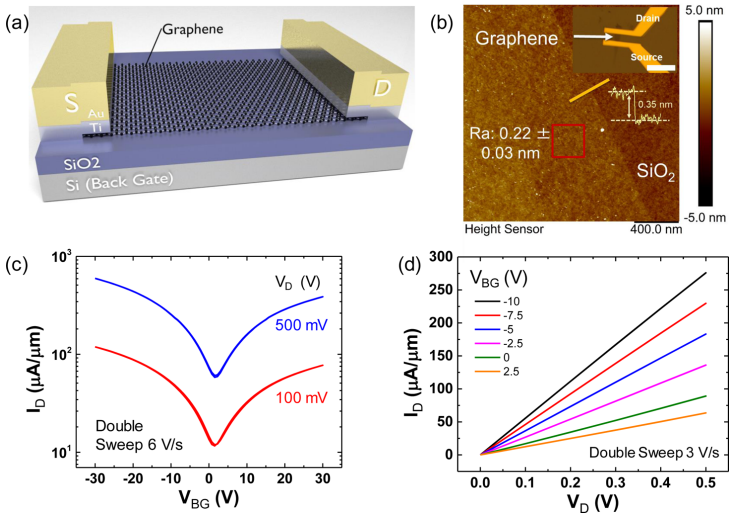

Figure 1. Room-temperature current and voltage characteristics of bare GFETs (before adding CoCrPc and $LiClO_4$). (a) Schematic of the GFET device. (b) AFM of device D1 after a CO_2 anneal on a 2 × 2 μm^2 area. R_a is the arithmetic average of the surface roughness averaged over 10, 0.3 × 0.3 μm^2 areas in the scanned image (one of the 10 areas is shown as a red box), and error bars represent one standard deviation from the mean. A line scan of the graphene step edge shows a height corresponding to a single layer. Inset shows an optical image of device D1. Scale bar is 10 μm. (c) Double sweep transfer characteristics of device D1 for V_D = 100 mV and 500 mV. (d) Output characteristics of device D1 at a backgate voltage (V_{BG}) from 2.5 to −10 V. All I−V measurements are made under N_2 in a dark chamber.

graphene[13]). While ionic gating is an effective tool for exploring new regimes of transport in 2D materials, there are limitations. Polymer electrolytes are solids that can be deposited as thin films that are typically tens of nanometers thick at their limit. To push the ion transport distance to the ultimate limit, it is of interest to explore device operation with electrolytes that are a single molecule thick; however, currently available solid electrolytes are not suitable candidates for a monolayer electrolyte because their intrinsic surface roughness is on the order of nanometers. In addition to scaling, ionic doping for devices should be achieved without a liquid solvent. While this has been demonstrated using solid-state, ion-containing polymers,[4,14,15] the room-temperature doping is volatile, and low temperatures (*e.g.*, <240 K) are required to "lock" the EDL into position. Thus, the development of a monolayer electrolyte with the ability to adjust the doping density *via* field control and to retain the doping in the absence of an applied gate bias at room temperature would be valuable for the development of 2D electronics.

Among 2D materials, graphene has unique electric properties such as ultrahigh intrinsic carrier mobility and room-temperature ballistic transport properties.[1] Doping of graphene-based electronics requires carrier density modulation that does not compromise the electric properties. Functionalizing the graphene surface with adsorbates that noncovalently interact with graphene is a promising approach because it will not degrade the electrical properties of graphene.[16] In this work, the surface of a graphene channel is functionalized by the physical adsorption of cobalt crown ether phthalocyanine (CoCrPc) molecules. Crown ethers (CEs) are cyclic molecules with the chemical formula $(CH_2CH_2O)_n$ that form a ring, where the size of the ring increases with increasing monomer repeat units, *n*. CE molecules can solvate a variety of metal cations[17] and selectively transport ions.[18] For the CE/Li^+ complex used in this work, for which n = 5, all of the O atoms within CE will reside on the same plane, making it possible to form a 2D structure.[19] A previous report using density functional theory (DFT) revealed that a crown ether/Li^+ (CE-Li^+) complex adsorbed on graphene can increase the binding strength between the absorbed ions and graphene and offers control of charge density and work function modulation.[20] DFT calculations show that the Li^+ is located inside the cavity of CEs with n = 4 and 5, and there are two energetically favorable contact configurations for the CE/graphene or Li^+/CE/graphene system. Recently, new DFT calculations suggest that location of Li^+ with respect to the CE as well as the conformation of the CE itself can be modulated by an electric field applied normal to the plane of the molecule.[21] On the basis of the DFT calculations, reconfigurable doping can be achieved using an applied electric field to push/pull the Li^+ relative to the graphene surface.

For the CE/ion system to function as a 2D dopant, the CEs must align parallel to the 2D crystal substrate so that the direction of ion transport is normal to the surface of the 2D crystal. To ensure that the CEs are lying flat on the graphene channel, they are covalently bonded to a cobalt phthalocyanine molecule, which provides the π−π interactions that promote in-plane physisorption of the molecule. Yoshimoto *et al.* reported the deposition of monolayer 15-crown-5-ether-substituted cobalt(II) phthalocyanine (CoCrPc) molecules on Au electrodes in a highly ordered array.[22,23] Recently, we reported a method for the solution-phase deposition of monolayer CoCrPc on freshly cleaved, highly ordered pyrolytic graphite (HOPG).[24] Monolayer CoCrPc forms an ordered array with a packing density of 1 molecule/16 nm^2 when annealed at 180 °C for 30 min.

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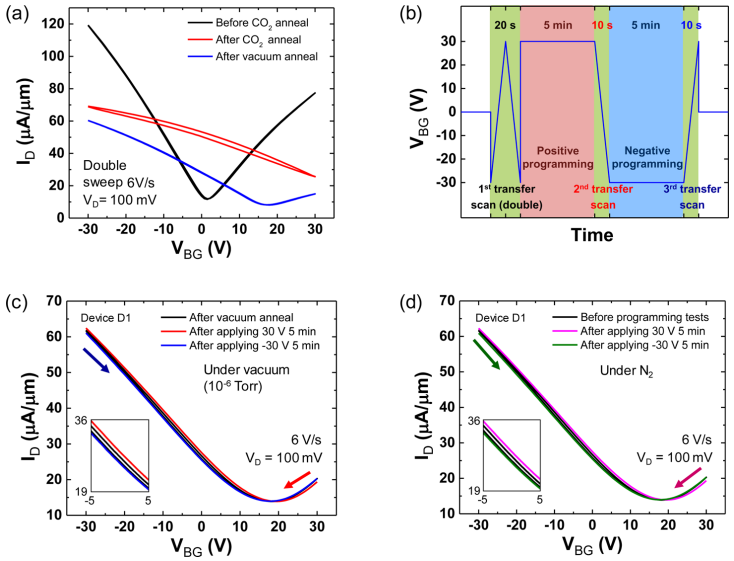

Figure 2. Transfer characteristics and programming tests of bare GFETs after CO_2 treatment followed by vacuum anneal. (a) Transfer curves for device D1 before and after CO_2 anneal and after vacuum anneal. (b) Sequence of a complete programming cycle, consisting of one positive programming test, one negative programming test, and three transfer scans. (c) Transfer curves after one programming cycle on device D1 under vacuum. Inset shows an enlarged view for $-5 < V_{BG} < 5$ V. Arrows indicate the direction of the scan. (d) Transfer curves after one programming cycle on device D1 under nitrogen showing identical behavior as under vacuum. Inset shows an enlarged view for $-5 < V_{BG} < 5$ V.

The combination of CoCrPc and Li^+ is a promising monolayer electrolyte because it can form an ordered monolayer on HOPG and cations are expected to pass through the CE cavities in response to an applied field, thereby modulating the location of the ions relative to the graphene surface. In this study, we demonstrate the ion gating of graphene FETs (GFETs) using a monolayer of CoCrPc and $LiClO_4$ without liquid solvent. A series of programming tests were used to determine the effectiveness of the monolayer electrolyte as a dopant. The Dirac point shifts toward positive/negative V_{BG} after programming tests of the same polarity, indicating that the doping is reconfigurable. The magnitude of the Dirac point shift indicates charge carrier densities of ~3 × 10^{12} cm^{-2} for a CE to Li^+ ratio of 5:1, which is 5 times lower than the theoretical maximum of 1:1. In addition, retention tests showed that the drain current after programming can be retained even in the absence of gate bias for at least 30 min (maximum time monitored). This experimental demonstration of a monolayer electrolyte suggests the potential for applications including electric double layer nanoionic memory and as a reconfigurable ion gate for semiconductors at the limit of scaling.

RESULTS AND DISCUSSION

Prior to depositing the monolayer electrolyte, the current and voltage characteristics of the bare graphene FETs were measured. A device schematic is provided in Figure 1a, and an optical image of a two-terminal device is shown in the inset of Figure 1b. The separation of the metal contacts is 3 μm in all devices, and the width of the graphene channel varies from 0.6 to 3 μm depending on the size of the flake. Most of the devices are single layer (see the atomic force microscope image in Figure 1b and the Supporting Information Figures S1 and S2). The room-temperature transfer characteristics are shown in Figure 1c at two source−drain voltages (V_D). The device shows ambipolar behavior with a minimum conduction current at a back gate voltage (V_{BG}) of 2 V. Within the measurement window, the On−Off ratio is approximately 10 for the p branch and 6 for the n branch. The output characteristics (Figure 1d) show that I_D depends linearly on V_D for both the electron and hole branches, indicating ohmic contact at both source and drain terminals. All the devices fabricated in this study show similar electrical behavior, with the Dirac point located within 5 V of V_{BG} = 0 V and linear I_D−V_D behavior.

Because electrostatic ion gating relies on the formation of an electric double layer at the interface between the electrolyte and the device channel, it is important to ensure that the channel surface is clean before depositing the monolayer electrolyte. An AFM scan of the graphene channel after device fabrication (Figure S1) shows a surface roughness of ~0.56 nm, with features that are likely the result of the e-beam resist residue. Residue will limit the proximity of the ions to the surface, and therefore the strength of EDL, and can disrupt the formation of an ordered monolayer of CoCrPc. To reduce the amount of residue on the surface, the devices were annealed for 30 min at 500 °C in CO_2, a method first reported by Gong *et al.*[25] After using the same procedure on our devices, the graphene surface roughness was reduced to ~0.22 nm with a step height of 0.35 nm corresponding to a single layer of graphene (Figure 1b). The Raman spectra (Figure S3) showed no D peak and no signature of graphene oxide, indicating that the CO_2 anneal

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does not adversely affect the physical or chemical structure of the graphene channel.

To determine the effect of the CO_2 on the electrical properties of the devices, transfer measurements of the bare graphene FETs were repeated after the anneal. Annealed devices show a strong p-type shift of the surface potential, as indicated by a right shift of the Dirac point of more than 30 V, decreasing carrier mobility, decreasing ON current by a factor of 2, and increasing hysteresis (Figure 2a). A detailed discussion of the effect of the CO_2 anneal is provided in the Supporting Information. One potential cause of these effects is the high-temperature annealing of 500 °C, which has been studied previously for graphene.[26] For example, charge transfer from the SiO_2 substrate can lead to the accumulation of excess positive charges in graphene, which increases with increasing temperature from 200 to 400 °C; depending on other factors, an increase in carrier density can decrease carrier mobility.[26] In addition, high-temperature annealing can increase contact resistance and decrease current. Finally, the p-type shift and increase in hysteresis may also be explained by the absorption of H_2O and O_2.[27,28] Therefore, to remove adsorbates that could potentially cause the p-type shift, the samples were annealed for 10 h under vacuum ($\sim 10^{-6}$ Torr) at 127 °C. Prolonged vacuum annealing is reported to be an effective method to reduce the p-type shift of surface potential and hysteresis caused by H_2O and O_2 adsorbed on graphene.[28−30] After vacuum annealing, the Dirac point shifted back into the measurement window and the hysteresis vanished, as shown in Figure 2a. However, the Dirac point did not return to the same position (~0 V) as before the CO_2 anneal, indicating that either not all of the adsorbates were removed or there are additional factors responsible for the p-type shift of surface potential. Because the Dirac point shifts back into the measurement window after vacuum annealing, and because our characterization of the monolayer electrolyte requires monitoring the Dirac point location, these devices remain suitable for this investigation.

As discussed in the introduction, the position of the Li^+ ions with respect to the graphene surface is controlled using a backgate voltage applied normal to the plane of the monolayer electrolyte. The proximity of the ions near the graphene surface can be monitored by measuring the location of the Dirac point *via* transfer characteristics; a shift in the Dirac point indicates the change in surface potential. Furthermore, if a Dirac point shift is detected by transfer measurements, it means that the doping persists at least as long as the time scale of the transfer measurement. To track the Dirac point shift, the programming tests outlined in Figure 2b were applied. A positive(negative) backgate voltage of 30(−30) V is applied for 5 min. It is to be noted that neither the ±30 V programming bias or the 5 min programming time was optimized; these were simply chosen as initial values. One complete programming tests cycle was conducted in the following sequence. First, a double sweep transfer curve was taken before the programming tests to determine the original Dirac point location (black curve). Next, a positive programming bias was applied (V_{BG} = 30 V for 5 min) to push the Li^+ away from the graphene surface, and a single sweep transfer curve (from positive to negative V_{BG}) was taken immediately after the test to record the Dirac point shift (red curve). Last, a negative programming bias was applied (V_{BG} = −30 V for 5 min) to pull Li^+ close to the graphene surface, and a single sweep transfer curve (from negative to positive V_{BG}) was taken immediately after the test to record the Dirac point shift (blue curve). The transfer curve taken before the programming tests was a double sweep to measure the hysteresis, while the transfer curve taken after each programming test was a single sweep with the starting point in accordance with the polarity of previous programming voltage. For example, after the positive programming test, the transfer curve is measured from positive to negative voltage. In this way the reverse programming of the device is minimized during the transfer measurement. In addition, to reduce the potential contribution of ion motion during the measurements, the sweep rate has to be sufficiently fast so that the ion-induced doping density is relatively stable during the measurements. In this study the sweep rate is chosen as 6 V/s for all the transfer measurements during programming tests. To maintain the measured current accuracy at the chosen sweep rate, the scanning voltage step (resolution) is set at 0.75 V. These configurations are all for the purpose of a more accurate measurement of the Dirac point location immediately following each programming test.

After the vacuum anneal, a series of programming tests were conducted on bare graphene FETs (*i.e.*, without the monolayer electrolyte) that served as the first set of control experiments to which the measurements with the monolayer electrolyte were compared. Figure 2c shows the transfer characteristics taken after vacuum anneal under vacuum in one programming cycle on device D1. The Dirac point shifted right (left) by 1.5 V after positive (negative) programming. The shift after negative programming is the difference in Dirac point location between the red and blue curves. The same Dirac point shifts (±1.5 V) are observed after purging the probe station chamber with N_2 up to atmospheric pressure and repeating the measurement (Figure 2d). The shift of the Dirac point during programming tests on bare graphene FETs is likely caused by charge trapping and detrapping at the graphene/SiO_2 interface,[31] which leads to charge transfer and a capacitive gating effect between graphene and SiO_2.[32] We can estimate the trapped charge density from the Dirac point shift. The shift is caused by the applied backgate voltage, which is dropped over 90 nm of SiO_2; therefore, the charge density increase, ΔQ, can be calculated by $\Delta Q = C_{ox}\Delta V_{Dirac}$, where C_{ox} is the capacitance of the SiO_2 (backgate capacitance) and ΔV_{Dirac} is the shift of the Dirac point. The charge density, n, is calculated by $n = Q/e \approx 3.6 \times 10^{11}/cm^2$, which is close to the graphene intrinsic carrier density at 300 K ($n_{in} \approx 10^{11}/cm^2$).[33] For the reasons discussed previously, the minimal voltage step in these measurements or the smallest sensible change of Dirac point voltage is 0.75 V. However, this does not prevent us from identifying the polarity of the surface potential change and estimating the charge density induced by the monolayer electrolyte, which as discussed later in the study, is an order of magnitude larger than trapped charge density.

Dirac point shifts of 1.5 V or less were observed over multiple bare graphene devices during programming tests (see Supporting Information Figure S7), and the magnitude of the shift is summarized in Table S1. The average trapped charge density after positive (negative) programming is about 2.8 ± 0.9 and 3.1 ± 0.8 × 10^{11} cm^{-2}, respectively. The charge density is averaged over four devices with two measurements on each device, and the error represents one standard deviation from the mean. These data provide a baseline for the induced trapped charge density in the backgated programming tests, which was later subtracted to obtain the ion-induced charge carrier density in those devices functionalized with the monolayer electrolyte.

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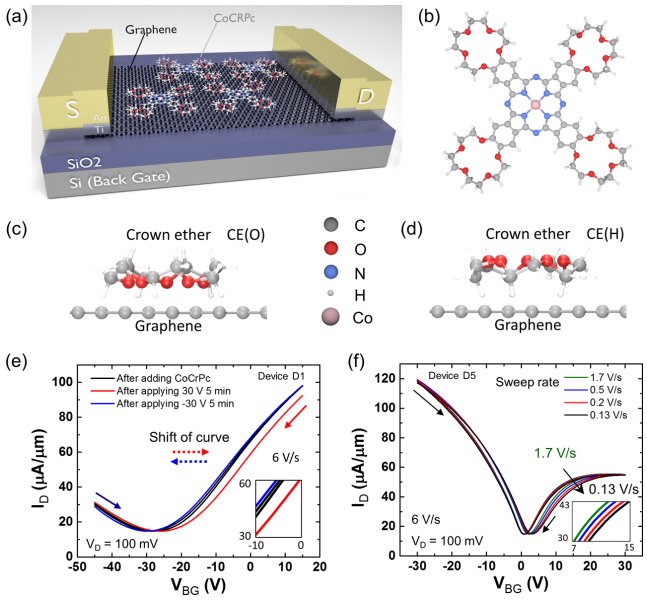

Figure 3. Electrical device characteristics of GFETs after depositing CoCrPc. (a) Schematic of the device after depositing a monolayer of CoCrPc. (b) Top view of CoCrPc. (c and d) Side view of CEs over graphene with two configurations: (c) CE(O) with the O atoms close to the graphene surface and (d) CE(H) with H atoms close to the graphene surface. (e) Transfer curves after one programming cycle on device D1, showing the right shift of the Dirac point after the positive programming test and left shift after the following negative programming test. Inset shows an enlarged view for $-10 < V_{BG} < 0$ V. Arrows indicate the direction of the scan. (f) Double sweep transfer scans (from negative to positive V_{BG} and back) with a slow sweep rate from 1.7 to 0.13 V/s on device D5. Inset shows an enlarged view for $7 < V_{BG} < 15$ V during back sweep.

The control measurements on bare graphene FETs established the magnitude of the Dirac point shift that can be expected in the absence of the monolayer electrolyte. Next, a monolayer of CoCrPc was deposited on the same sample, and the programming measurements were repeated (Figure 3a). Note that this system does not yet include ions, and as such, it can also be regarded as another control measurement to determine the extent to which the CoCrPc alone affects the surface charging. Figure 3e shows the transfer characteristics of device D1 after adding CoCrPc and completing one programming tests cycle. Notice first that the Dirac point before any programming (shown in black) shifted left for ~40 V, compared with the bare graphene FETs. After the positive programming test, the transfer curve shifted right by 3 V (red), and after the negative programming test the transfer curve shifted left by 3.75 V (blue), close to its original position (black). Compared to the bare graphene FETs, the Dirac point shift during the programming test increased after adding CoCrPc, indicating that the CoCrPc can change the graphene surface potential under applied V_{BG}. These data can be explained by considering the dipole effect and bistable states of the four CEs within the CoCrPc. As discussed in the introduction, Wang *et al.* used DFT to show that CE and graphene exhibit two different contact configurations:[20] (1) CE(O) with the O atoms close to the graphene surface, as shown in Figure 3c, and (2) CE(H) with H atoms close to but O atoms away from the graphene surface, as shown in Figure 3d. According to their DFT calculations, the chemical interaction between the CE and the graphene would cause charge transfer and charge redistribution in the CE/graphene system, which would form electric dipoles at the interface and eventually lead to the change of work function of CoCrPc and carrier density in graphene. In the programming tests, positive programming voltage would attract O atoms, which are more electronegative, resulting in a CE(O) contact configuration at the interface and a p-type shift of surface potential in graphene. On the contrary, negative programming voltage would push O atoms away, forming the CE(H) contact configuration and n-type shift of surface potential inside graphene. The transfer curve after negative programming (blue) overlaps with the transfer curve before programming (black), suggesting that the CEs are likely in the CE(H) contact configuration after being deposited on graphene, causing n-type doping inside graphene. However, this n-type doping effect is not as strong as the change of surface potential observed after depositing CoCrPc (before programming), indicating that other factors are responsible for the surface potential change. Further investigation is needed to understand this effect, but this does not prevent us from studying the ion gating effect induced by the monolayer electrolyte, which is the focus of this study. The increase of the Dirac point shifts during the programming tests are observed over multiple devices (see Figure S8), and the magnitude of the shifts is summarized in Table S2. Subtracting the trapped charge density described above, the average charge carrier density for the p- and n-type shift after positive and negative programming is 4.1 ± 2.6 and $4.7 \pm 1.6 \times 10^{11}$ cm^{-2}, respectively. The charge carrier density is averaged over six

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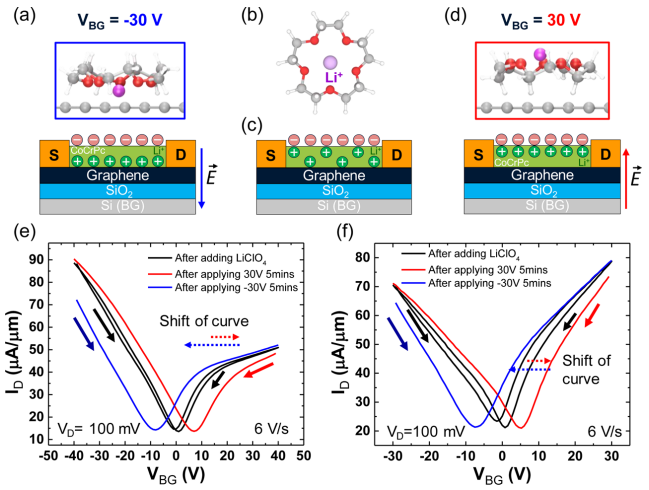

Figure 4. Electrical device characteristics of graphene FETs after depositing CoCrPc and $LiClO_4$. (a and d) Side view of the device and the monolayer electrolyte under applied backgate voltages. Based on DFT calculations,[20] there are two contact configurations for the Li^+, CE, and graphene complex: CE/Li^+/graphene (a) and Li^+/CE/graphene (d). (b) Top view of the monolayer electrolyte within one crown based on DFT calculations. (e) Side view schematic of the device after monolayer electrolyte deposition before any programming. Li^+ is randomly configured at either one of the two contact configurations. (e and f) Transfer curve after one programming cycle on devices D5 (e) and D9 (f) showing right shift of the Dirac point after positive programming and a larger left shift after negative programming, consistent with the location of Li^+. Arrows indicate the direction of the scan.

devices, and the error represents one standard deviation from the mean.

In an ionic system without bistable states, decreasing the sweep rate should decrease hysteresis in the double sweep transfer scans because ions have more time to respond to the applied electric field and reach their stable state. However, this trend is the opposite for a system with two stable states because provided with more time, ions can reach equilibrium at either one of the two stable states. The DFT calculations show that the CoCrPc has two stable states, and therefore hysteresis should be observed as the sweep rate is decreased. In programming tests with a sweep rate of 6 V/s, the Dirac point shift between the forward and reverse scans is 0.75 V. Figure 3f shows double-sweep transfer characteristics taken from −30 to 30 V at sweep rates varying from 1.7 to 0.13 V/s on device D5. As expected, the hysteresis increases with decreasing sweep rate. The difference in the Dirac points increases to ∼2 V at 1.7 V/s and ∼3 V at 0.13 V/s. Note that this trend of increased hysteresis with decreased sweep rate may also be observed for electron trapping at a certain sweep rate range. However, the increased Dirac point shifts in the programming tests after adding CoCrPc suggest that the effect of CoCrPc on changing surface potential of graphene is stronger; hence the observed Dirac point shift increase is more likely caused by the dipole of the CoCrPc.

In addition to increasing hysteresis, the slower sweep rate is accompanied by a shift of the transfer curve to more positive biases on the reverse scan for the part at $V_{BG} > 0$ V (Figure 3f inset). It should be noted that decreasing the sweep rate by a factor of 10 increases the measurement time by a factor of 10. The right shift is consistent with the effect that is observed after the positive programming test shown in Figure 3e. Together, these results indicate that increased programming time can shift the surface potential of graphene more p-type, suggesting that the response time of the CoCrPc to the applied bias is relatively slow (*i.e.*, time scale of seconds). However, the response time in the current device geometry does not represent the minimum response of the monolayer electrolyte system, because the time is related to the magnitude of the applied electric field.[21] Currently, programming is achieved by backgating through 90 nm of SiO_2 and graphene, so the actual electric field reaching the electrolyte is smaller than it would be for a thin top-gated device, and therefore the response time is longer. The same shift was not observed at $V_{BG} < 0$ V, suggesting that in the CE(H) configuration (Figure 3d), increasing programming time cannot further shift graphene surface potential n-type. This also agrees with the DFT calculations, which showed that the p-type charge density increase from the CE(O) configuration is stronger than the n-type charge density increase from CE(H).[20] In summary, even without the ions, the CoCrPc molecules can change the surface potential of graphene with an average charge carrier density of about 4.1 (4.7) × 10^{11} cm^{-2} for the p (n)-type shift after positive (negative) programming, respectively.

The monolayer electrolyte was prepared by drop-casting $LiClO_4$ from solution onto the CoCrPc-coated surface with a Li^+:CE molar ratio of 1:5, following by annealing. The Li^+ binds to electron-rich O atoms in the CE, and its precise location within the crown depends on the conformation of CE. On the basis of DFT calculations,[20] all of the O atoms within CE are on the same plane for 15-crown-5 ethers used in our study, with Li^+ at the center of the crowns (Figure 4b). DFT calculations also show that, similar to the CE/graphene interaction, there are also two contact configurations for the Li^+, CE, and graphene complex: CE/Li^+/graphene, where Li^+ is close to the graphene surface (Figure 4a), and Li^+/CE/graphene, where Li^+

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is away from the graphene surface (Figure 4d). Although the counterion, ClO_4^-, was not included in the DFT calculations, considering the charge distribution in this system, it is likely that the counterion will be located near the cobalt atom of the CoCrPc (additional discussion in the Supporting Information).

The transfer curves after one programming test cycle are shown in Figure 4e and f. After the positive programming test, the Dirac point shifted right by 8(7.5) V for device D5(D9). This effect is similar to what was previously observed when devices only have CoCrPc on top but no $LiClO_4$; however the magnitude of the Dirac point shift is about 2.5 times larger after adding $LiClO_4$ (Figure 5). A more interesting observation is

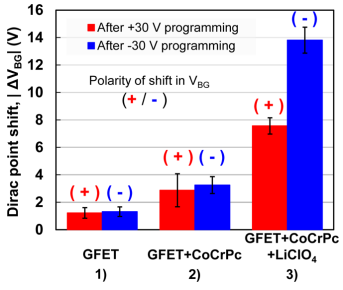

Figure 5. Dirac point shifts after ±30 V programming tests for (1) GFET (i = 4, m = 2), (2) GFET + CoCrPc (i = 6, m = 1), and (3) GFET+ monolayer electrolyte (CoCrPc + $LiClO_4$) (i = 2, m = 2), where i is the number of devices and m is the number of measurements on each device. Error bars indicate one standard deviation from the mean. The (±) signs on the plot indicate the polarity of the shift in V_{BG}.

that after the negative programming test, the transfer curve shifted further left (blue) than its original position (black), with a Dirac point left shift of 15.0(12.75) V for device D5(D9). The magnitude of the shift increased by more than 4 times compared with devices only having CoCrPc (Figure 5). On the basis of DFT calculations, Li^+ within the crowns of the CoCrPc molecules can be moved under applied positive(negative) backgate voltage to switch between two contact configurations (Figure 4a,d), shifting the surface potential of graphene more $p(n)$ type, which would cause the shift of the Dirac point after the programming tests. The magnitude of the shift for devices with both CoCrPc and $LiClO_4$ is increased compared with devices with only CoCrPc but no $LiClO_4$, because the Li^+ can move closer to (further away from) the graphene surface than O atoms in CEs (Figure 4a,d), and the Li^+ can interact more strongly with graphene to induce electrons (n-type doping). Without the participation of the counterion, ClO_4^- (which as discussed in the Supporting Information is expected to reside near the cobalt atom in CoCrPc and away from graphene surface), changing the distance between Li^+ and graphene would not induce any p-type doping (holes) inside graphene, only n-type. The p-type shift after positive programming (red curve) is likely explained as follows. Before programming, Li^+ is randomly and evenly configured at either one of the two contact configurations (Figure 4c). The positive programming with $+V_{BG}$ will push the remaining Li^+ away from graphene surface into the Li^+/CE/graphene configuration (Figure 4d), thus shifting the graphene surface potential more p-type. Figure 4e and f show that the n-type left shift (red to blue curve) is larger than the p-type right shift (black to red curve). This is expected because only a fraction of the Li^+ ions move during positive programming (Figure 4c to Figure 4d), while the majority of the Li^+ must move during negative programming (Figure 4d to 4a). DFT calculations also suggested that transforming the contact configuration from Li^+/CE/graphene to CE/Li^+/graphene would cause more n-type doping of graphene.[20] The increased magnitude of the Dirac point shift for both positive and negative programming tests after adding $LiClO_4$, along with the DFT calculations, presents a consistent picture that Li^+ is mobile within the monolayer solid-state electrolyte and can dope graphene FETs by modulating V_{BG}.

When ions are added to the CoCrPc, the average charge carrier density for the p- and n-type shift after positive and negative programming (after subtracting the trapped charge density) is about 1.5 ± 0.2 and 3.0 ± 0.2 × 10^{12} cm^{-2}, respectively. The carrier density is averaged over two devices with two measurements on each device, and the error represents one standard deviation from the mean. The measured carrier density is in agreement with the packing density of monolayer CoCrPc on graphene from our previous measurements. As mentioned above, the $LiClO_4$:CoCrPc molar ratio used in this study is 4:5, corresponding to a Li^+:CE ratio of 1:5. Using scanning tunneling microscopy, we previously determined the packing density of monolayer CoCrPc on graphene to be 0.0625 molecule/nm^2,[2,24] which for a 1:5 Li^+:CE ratio corresponds to a density of 5 × 10^{12} cm^{-2}. Assuming each Li^+ induces one image charge (electron) in the channel, the sheet carrier density in the channel would also be 5 × 10^{12} cm^{-2}. The average charge carrier density we estimated is ~3 × 10^{12} cm^{-2}, which is about 80% of what can be expected. Theoretically, each crown can accommodate one Li^+, meaning that by increasing the salt concentration to a Li^+:CE ratio of 1:1, a carrier density as high as 2.5 × 10^{13} cm^{-2} is feasible.

To confirm that the Dirac point shift is caused by moving Li^+ within the CoCrPc, another control experiment was conducted where $LiClO_4$ was deposited directly onto bare graphene FETs without any CoCrPc. For consistency, a concentration of $LiClO_4$ equivalent to that of the CoCrPc:$LiClO_4$ system was deposited. As shown in the Supporting Information, Figure S6, pure $LiClO_4$ n-type dopes the device, shifting the Dirac point to the left by more than 40 V. If the cations and anions were homogeneously distributed on the surface, no net doping would be observed. Therefore, the strong, n-type doping suggests that Li^+ is near the surface, while ClO_4^- ions are further away. This picture is consistent with anions surrounded by tightly bound water molecules that would screen the field. Additional experiments are required to understand the mechanism, but the observation is reproducible on multiple measurements over multiple devices.

While all the devices for which $LiClO_4$ was deposited on CoCrPc showed a left shift of the Dirac point (before programming tests), the magnitude of the shift varied from device to device. Comparing all eight devices, we found that they can be categorized into two types: type 1 devices show a left shift in the Dirac point of less than 10 V, while type 2 devices left shift more than 25 V. The transfer characteristics are shown in Supporting Information Figure S6. We also found that type 2 devices (with a larger shift of the Dirac point after adding $LiClO_4$) also exhibit a larger shift after adding CoCrPc (>55 V). Those categorized as type 1 show a smaller shift (~30 V) after adding CoCrPc. The magnitudes of the Dirac point shifts are compared for type 1 and type 2 devices in Figure 6.

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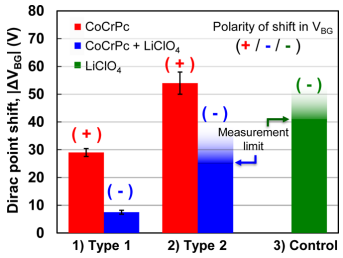

Figure 6. Comparison of Dirac point shift prior to programming after depositing CoCrPc, CoCrPc+$LiClO_4$, and $LiClO_4$ only. The three columns are (1) type 1 devices for which the Dirac point shift is less than 30 V (8 V) after depositing CoCrPc ($LiClO_4$) (i = 2), (2) type 2 devices for which the Dirac point shift is larger than 50 V (25 V) after depositing CoCrPc ($LiClO_4$) (i = 6), and (3) a control experiment of adding $LiClO_4$ directly to graphene without CoCrPc (i = 2), where i is the number of devices. The ($\pm$) sign indicates the polarity of the shift in V_{BG}. The error bar shows one standard deviation from the mean. For type 2 and the control experiment, the Dirac point shifts out of the measurement window after adding $LiClO_4$. The arrows indicate the measurement limit, and the faded bar reflects the fact that the Dirac point shifted beyond the measurement window to a value that cannot be determined.

The difference of the Dirac point shifts in the type 1 and 2 devices cannot be attributed to a difference in channel thickness because most devices are monolayer graphene (Figures S2 and S3 provide AFM scans of single-layer type 1 and type 2 devices). Instead, the two distinct device characteristics in types 1 and 2 could possibly reflect varying degrees of homogeneity of the monolayer electrolyte on top of the graphene channel, such as pinholes, aggregates, and disordered CoCrPc. As discussed in the introduction, the CoCrPc deposition method used in this study is the same method demonstrated previously for depositing a monolayer CoCrPc on freshly cleaved HOPG.[24] Although HOPG and exfoliated graphene share the same surface bonding structure, achieving a homogeneous monolayer of CoCrPc on exfoliated graphene flakes is more challenging. One reason is that the monolayer tends to be less homogeneous than HOPG near step edges; in the graphene FETs, there are more edges per unit area of graphene compared to HOPG, and so more of the monolayer may be disorganized. In addition, patterned source/drain metal contacts create an additional interface at the surface of graphene, and it is unclear how the CoCrPc molecule will arrange near the edge of a metal contact. Lastly, even though a CO_2 clean was used, it is possible that some electron-beam lithography residue is still present that will prevent a homogeneous deposition of CoCrPc. When the CoCrPc is inhomogeneously deposited on the graphene channel, it may cause a larger left shift of the Dirac point such as what is observed for type 2 devices.

In addition, for these type 2 devices, if the inhomogeneity includes pinholes in CoCrPc, some of the $LiClO_4$ would reach the graphene surface directly through these pinholes. We learned from control experiments (Figure 7, Figure S6) that depositing ions directly onto the graphene surface will cause a large left shift of the Dirac point. When the density of the pinholes is above a critical threshold, the $LiClO_4$ in the pinholes will dominate the Dirac point shift, which would lead to a bimodal distribution of Dirac point shifts among multiple devices, agreeing with the observation of two types of devices. The challenges in achieving monolayer CoCrPc on the fabricated graphene FET limit the available devices that can be measured after deposition of the monolayer electrolyte.

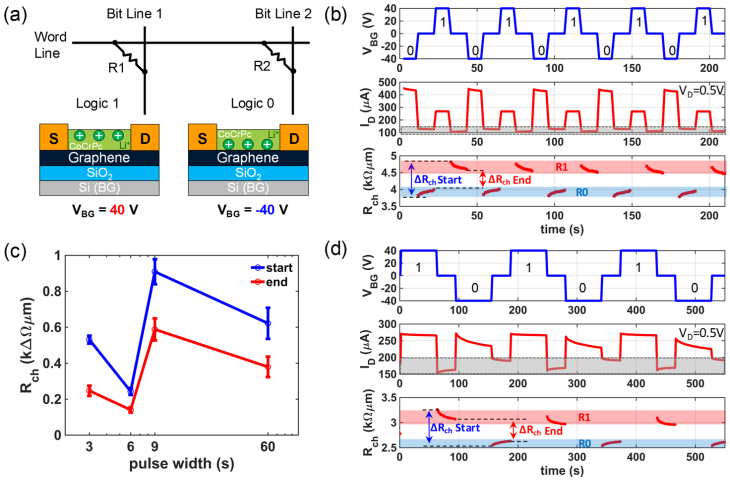

Figure 7. V_{BG} step tests with different step width. (a) Illustration for program (1) and erase (0) using the backgate voltage (V_{BG}). (b) Step test with 9 s step width. Third row is R_{ch} during the reading time after each program/erase, calculated from I_D in the shaded area in the second row. ΔR_{ch} in blue is the difference between R_{ch} right after the program/erase step, and ΔR_{ch} in red is the difference between R_{ch} just before the next program/erase step. (c) ΔR_{ch} right after the program/erase step (start) and ΔR_{ch} just before the next program/erase step (end), with a step width of 3/6/9/60 s. ΔR_{ch} is averaged over five step cycles (three for the 60 s step width), and the error bar shows one standard deviation away from the mean. (d) Step test with 60 s of step width. Third row is R_{ch} during the reading time after each program/erase, calculated from I_D in the shaded area in the second row.

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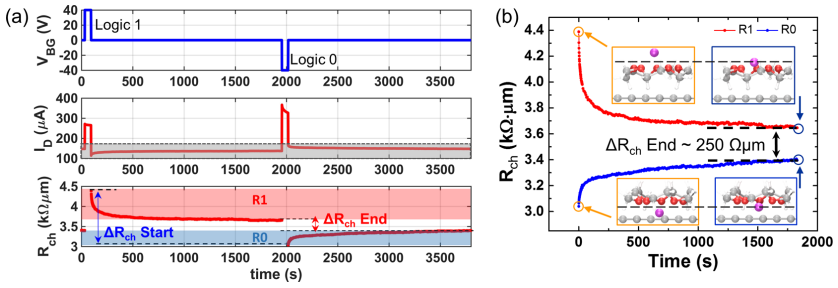

Figure 8. Retention measurements and memory window. (a) Retention test with 60 s step width and 30 min of monitoring time. The third row is a zoomed-in view of the drain current from the shaded area in the second row. (b) Drain current (I_D) as a function of time after removing backgate voltage (t = 0). The difference of I_D is the memory window. Inset cartoons showed Li^+ further and closer to graphene than stable states immediately after removing V_{BG} (yellow box) and after returning to a stable state (dark blue box).

The programming tests described above indicate that the monolayer electrolyte is exhibiting some memory effect (*i.e.*, the Dirac point location shifted after programming, and the shift was retained even after removing the programming bias.) To further explore the memory effect, backgate step tests were made with fixed drain voltage (V_D = 0.5 V) while monitoring the drain current, I_D. In step tests we "write" to the device by applying a ±40 V backgate voltage, which we define as program/erase (or logic 1/0), for a certain amount of time (*i.e.*, the step width). On the basis of DFT calculations, and similar to the previous programming steps discussed above, program (logic 1) should move the Li^+ away from graphene surface, giving rise to a Li^+/CE/graphene contact configuration. In contrast, erase (logic 0) should move the Li^+ toward the graphene surface to create the CE/Li^+/graphene contact configuration. The erase step induces more electrons in graphene because Li^+ is closer to the graphene surface than in the program step, and thus the graphene channel resistance during the erase step (R0) will be smaller than during the program step (R1) (Figure 7a). If the Li^+ retains its location within the monolayer electrolyte after removing the program/erase voltage, then the channel resistance will be retained at two distinct states (R1/R0). The "read" step is then completed by measuring the channel current (I_D) after the program/erase step at the same V_D in the absence of backgate bias (V_{BG} = 0 V). The cycle is shown in Figure 7b, and the sequence of one test cycle is as follows: (1) program/erase the device for X seconds (where X = 3/6/9 is the step width), (2) read the device for (20 − X) seconds, (3) erase/program the device for X seconds, (4) read the device for (20 − X) seconds. In this way one test cycle period is fixed at 40 s. The cycle was repeated consecutively for five times. Note that the ±40 V program/erase voltage, 3/6/9 s step width, and 40 s period were chosen simply as a starting point; these values are not optimized and therefore do not reflect any intrinsic limitation of the system. In experiments, I_D was monitored continuously. The channel resistance (R_{ch}) is calculated by $R_{ch} = V_D/I_D$. The memory window, ΔR_{ch}, is defined as the difference between channel resistance after the program step (R1, logic 1 state) and after the erase step (R0, logic 0 state).

I_D as a function of time is shown in Figure 7b during five cycles with a step width of 9 s. The third row in the figure is R_{ch} after each program/erase step (during these times no V_{BG} is applied, so we are "reading" the device). During five consecutive step cycles we "read" two distinct values of R_{ch} after the program/erase steps: R1 after the program step is ∼4.6 kΩ μm (red shade), and R2 after each erase step is ∼3.9 kΩ μm (blue shade). It is observed that the memory window (ΔR_{ch}) gradually decreased with time. R1 immediately after each program step is ∼4.8 ± 0.05 kΩ μm, and R2 immediately after each erase step is ∼3.8 ± 0.02 kΩ μm, giving a maximum memory window of 1.0 ± 0.05 kΩ μm at the moment after the program/erase step (ΔR_{ch} "start" shown in blue). ΔR_{ch} decreased with time until just before the start of the next program/erase step when it has its minimal value of 0.5 ± 0.07 kΩ μm (ΔR_{ch} "end" shown in red). Data are averaged over five step cycles, and error represents one standard deviation from the mean. The two distinct values of R_{ch} after the program/erase step correspond to two logic states (1/0). During five consecutive step cycles the corresponding R_{ch} for each logic state are repeatable and consistent. Although the memory window decreased during the "read" period, R_{ch} maintained at least 400 Ω μm of difference, suggesting that the memory effect is nonvolatile on the time scale of the measurement.

To investigate the relation between memory window and step width, we repeated the step tests with step widths of 3 s, 6 s (not shown here), 9 s (Figure 7b), and 60 s (Figure 7d). For 3, 6, and 9 s step width tests one test cycle period is 40 s. For the 60 s step width test, the period is 180 s, the "read" time is 30 s each, and the cycle was repeated three times (Figure 7d). Experiments with different step widths of 3/6/9/60 s suggest that the size of the memory window is related to the program/erase time, and 9 s of program/erase time has the largest memory window (∼910/590 Ω μm for ΔR_{ch} start/end in Figure 7c). Data are averaged over five step cycles (three for a 60 s step width), and the error bar shows one standard deviation from the mean.

The nonvolatility of the device was further investigated with a retention test. A 60 s program/erase step was applied; then the backgate was grounded and I_D was monitored for 30 min (Figure 8a). R_{ch} remained at two distinct states even 30 min after removing the program/erase bias. The memory window immediately after the step is about 1400 Ω μm and 30 min later remains larger than 250 Ω μm (Figure 8b). The decrease of the memory window is likely because the program(erase) bias pushed(pulled) Li^+ further(closer) to the graphene compared to the stable state calculated in DFT. For example, as shown in Figure 8b (blue curve), immediately after removing the erase bias, the Li^+ was closer to graphene than its stable state (yellow inset box), inducing more image charges resulting in lower

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channel resistance (~3030 Ω μm). Without the bias to hold its location, Li^+ gradually returned to its stable state (dark blue inset box) and the channel resistance increased to ~3400 Ω μm. A similar effect likely caused the R_{ch} decrease after program bias. If Li^+ is further away from its stable position after the program bias than after the erase bias, this could explain why the change of R_{ch} is also larger after program bias (Figure 8b red curve, ~750 Ω μm) than after erase bias (Figure 8b blue curve, ~370 Ω μm). The relaxation time of the monolayer electrolyte is on the time scale of 10^3 s, which is approximately 10^6 times longer than the retention time of conventional solid polymer electrolytes, such as PEO:$LiClO_4$, and ionic liquids, such as DEME-TFSI [*N,N*-diethyl-*N*-(2-methoxyethyl)-*N*-methylammonium bis(trifluoromethylsulfonyl)imide], that have relaxation times of a few milliseconds at room temperature (ref 12 for DEME-TFSI and unpublished data for PEO:$LiClO_4$).

For the current mechanism of operation, the size of the memory window is directly related to the On−Off ratio of the FET. Due to the absence of a band gap and the semimetallic behavior in graphene, the On−Off ratio for graphene FETs is only about 10. While the memory window of the current devices is limited by the intrinsic property of graphene, this is not a fundamental limit. The same device mechanism described in this study is applicable to a variety of other 2D crystals, including semiconductors, such as MoS_2. With an On−Off ratio about 10^7 times larger than graphene,[3] the memory window should be significantly increased. For this study, graphene was selected as an elemental channel material to provide a simple framework for both experiments and first-principles simulations. DFT studies of the Li^+/CE/graphene system are used to interpret the experimental results and to understand the operating mechanisms in the monolayer electrolyte system. Experiments reveal that bistability can be achieved. The fact that I_D remains at two distinct states after program/erase steps suggests that the position of the Li^+ could be programmed and maintained within the monolayer electrolyte. These data provide a basis for explorations of this concept in other 2D materials.

One advantage of the proposed monolayer electrolyte concept is its potential for lower operating voltage and faster response time − attributes that are predicted by DFT calculations.[21] The calculations predict that a vertical electric field of 0.15 V/Å will lower the energy barrier to Li^+ diffusion from 0.29 eV to 0.20 eV, enabling transport from one state to another with a switching speed on the time scale of nanoseconds. However, the minimal response time cannot be quantified for the backgated devices in this study because the switching time between the bistable states is related to the ion diffusion energy barrier, which depends on the strength of the applied field.[21] The strength of the field that reaches the electrolyte *via* backgating through a thick dielectric layer is smaller than that for a thin top-gated device, and the exact field strength is difficult to estimate because some fraction of the field will be screened by the graphene channel. Future work includes fabricating a top-gated device geometry for which the response time can be quantitatively correlated to the applied field.

CONCLUSION

The ionic gating of graphene FETs using a monolayer, solid-state electrolyte has been demonstrated. The doping was achieved by moving ions within a one-molecule-thick electrolyte that does not contain any liquid solvent. Unlike charge transfer doping methods, which do not provide doping modulation or reconfigurability, this monolayer solid-state electrolyte dopant is reconfigurable, and the charge carrier density can be modulated by more than 1 order of magnitude using an applied electric field. Sheet charge carrier density changes on the order of 10^{12} cm^{-2} are measured, and on the basis of the packing density of the monolayer electrolyte, 10^{13} cm^{-2} is predicted by increasing the ion concentration. The monolayer electrolyte-doped FET also shows a memory effect. The drain current remains at two distinct states even after removing the applied field, suggesting that the position of Li^+ could be programmed and maintained within the monolayer electrolyte. Retention tests showed that the retention time is greater than 30 min (maximum time measured), and the relaxation time of the electric double layer is more than 10^6 times larger than all reported polymer electrolytes, such as PEO:$LiClO_4$. The same device mechanism could be used with semiconducting 2D crystals to increase the memory window. This feature indicates that the monolayer electrolyte is also potentially useful in developing memory devices, if the switching speed is sufficiently fast.

METHODS

Devices were fabricated on a degenerately doped p-type Si substrate (resistivity 0.001−0.005 ohm-cm) with 90 nm of thermally grown SiO_2 (Graphene Supermarket). The substrate was precleaned by acetone, 2-propanol, and deionized water, then baked at 180 °C for 2 min to dehydrate the surface. Graphene flakes were mechanically exfoliated from HOPG and then transferred to the SiO_2/Si substrate using the Scotch tape method. Thin graphene flakes were first selected by optical microscopy and then confirmed with atomic force microscopy (AFM, Bruker Dimension Icon) in ScanAsyst mode using silicon nitride ScanAsyst Air tips. AFM data show the flakes are mostly single-layer graphene (0.3−0.4 nm). Source and drain contacts were patterned by electron-beam lithography. A 300 nm thick undercut layer of methyl methacrylate-8.5-EL9 (MMA-8.5-EL9, MicroChem) was spin-coated, followed by a soft bake at 170 °C for 2 min. Then, a 100 nm thick, poly(methyl methacrylate)-950-C2 (PMMA-950-C2, MicroChem) was spin-coated, followed by a soft bake at 170 °C for 3 min. After exposure, the sample was developed in methyl isobutyl ketone/methyl ethyl ketone/isopropyl alcohol (MIBK:MEK:IPA) solution in a volume ratio of 50:3:150 at room temperature for 40 s, followed by an isopropyl alcohol rinse. Metal contacts consisting of Ti (5 nm) and Au (150 nm) were deposited by electron beam evaporation (base pressure <2 × 10^{-6} mbar). Lift-off was performed in hot acetone (70 °C) for 1 h, followed by mr-Rem 400 remover for 5 min (Micro Resist Technology GmbH). The sample was then rinsed with isopropyl alcohol followed by deionized water.

To reduce the PMMA resist residue on the graphene FET channel, an anneal in a CO_2 environment was performed.[25] A tube furnace was connected to CO_2 (99.99%) and N_2 (99.999%) gases. The sample was loaded into a quartz sample boat and then transferred to the tube furnace at room temperature. The tube was purged with N_2 for 15 min at a flow rate of 300 sccm. This ensured that the tube was dry and free of other gases that may react with the sample surface. Following the N_2 purge, the tube was then purged with CO_2 for 30 min at 100 sccm. After 30 min, the flow rate of CO_2 was reduced to 10 sccm; then the furnace was heated to the target temperature of 500 °C at a rate of 20 °C/min. The furnace was then maintained at 500 °C and 10 sccm CO_2 for 30 min to etch the resist residue. To terminate the resist etch step, the CO_2 was replaced by a 300 sccm N_2 purge, while the furnace cooled to room temperature. The sample was then removed into the ambient for several minutes before loading into an Ar-filled glovebox. AFM inside the glovebox was used to image the surface. Raman

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spectroscopy on a separate set of samples was used to confirm that the graphene was not oxidized or made defective by the CO_2 anneal.

A vacuum anneal was conducted using a Cascade Microtech PLC50 Cryogenic vacuum probe station at 127 °C (400 K) under ~10^{-6} Torr. After 10 h of annealing, the heater was turned off and the probe station returned to room temperature within 24 h.

Monolayer CoCrPc was deposited using our previously developed method.[24] The CoCrPc solution was prepared by dissolving 1 mg of CoCrPc in a 100 mL mixture of anhydrous benzene/ethanol (9:1 v/v, Sigma-Aldrich: 99.8% anhydrous benzene, 99.5% anhydrous ethanol) and sonicated for 60 min at 40 kHz (Branson 2510 sonicator). An initial deposition of 125 μL of CoCrPc solution (10 mg/L) was drop cast onto graphene FETs (substrate area ~1 × 1 cm) in an Ar-filled glovebox using a micropipet with a drop volume of 25 μL. To achieve the optimal coverage of CoCrPc on the wafer, a second deposition of 100 μL was applied after the previous drops were evaporated and the sample surface appeared dry. A total amount of 225 μL of CoCrPc solution is used. After drop casting the sample was transferred onto a hot plate and annealed at 180 °C for 30 min.

To prepare the monolayer electrolyte, 140 μL of $LiClO_4$ dissolved in ethanol (Sigma-Aldrich: 99.5% anhydrous ethanol) with a solution concentration of 1 mg/L was drop cast onto CoCrPc-coated graphene FETs in an Ar-filled glovebox using a micropipet. After deposition the $LiClO_4$:CoCrPc ratio is 4:5, corresponding to a ratio of 1:5 Li^+:Crowns (4 crowns per CoCrPc molecule). The sample was transferred onto a hot plate and annealed at 180 °C for 30 min before removing from the glovebox for electrical measurements.

Electrical measurements immediately after vacuum anneal were performed on a Cascade Microtech PLC50 Cryogenic vacuum probe station under ~10^{-6} Torr at room temperature using an Agilent B1500A semiconductor parameter analyzer. The rest of the electrical measurements were made on a Cascade Microtech Summit 11000 probe station in a dark environment at room temperature using the same semiconductor parameter analyzer. During the measurements the probe station was under a constant flow of N_2 to minimize water and O_2 absorption in the monolayer electrolyte.

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acsnano.6b08505.

Raman spectra of graphene; AFM images and optical images of devices before and after CO_2 annealing; transfer characteristics of the devices after depositing CoCrPc and then $LiClO_4$ and of a control device (without CoCrPc) before and after adding $LiClO_4$; transfer characteristics on multiple devices during programing tests, including data on bare GFET and GFET+CoCrPc (PDF)

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Notes

The authors declare no competing financial interest.

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