EFFECT OF PLATINUM OXIDATION AND REDUCTION ON SINGLE ELECTRON TRANSISTORS FABRICATED BY ATOMIC LAYER DEPOSITION

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by

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Dedicated:

To my mom and dad for homeschooling me and teaching me the values of thoroughness, perseverance, and integrity, which have proven invaluable beyond price.

To my wonderful wife, Kaylee, for endlessly supporting and encouraging me, and enduring three semesters of long-distance marriage so I could pursue graduate studies.

To my Lord and Savior, Jesus Christ, for blessing me beyond what I could ask for or imagine, and for making the world full of mysteries to explore.

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CHAPTER 1:

PERSPECTIVE AND MOTIVATION

Gordon Moore predicted in 1965 that transistor speed and density would approximately double every eighteen months [1] and this prediction has proved remarkably accurate. It has fueled the ubiquity of personal computers and mobile devices, which have revolutionized daily life. However, clock speeds have been stalled around 3 GHz due to power dissipation for almost a decade, and while computer memory and the sheer number of transistors per processor has continued to grow exponentially, with physical transistor gate lengths now at 20 nanometers, the difficulty and cost of achieving further scaling is also growing exponentially [2]. Complementary metal oxide semiconductor (CMOS) transistors, which have been the industry workhorse for decades, have scaled well but on the nanometer scale suffer from severe short channel effects such as channel length modulation and drain induced barrier lower. Thus “beyond CMOS” devices and computing schemes are drawing increasing attention.

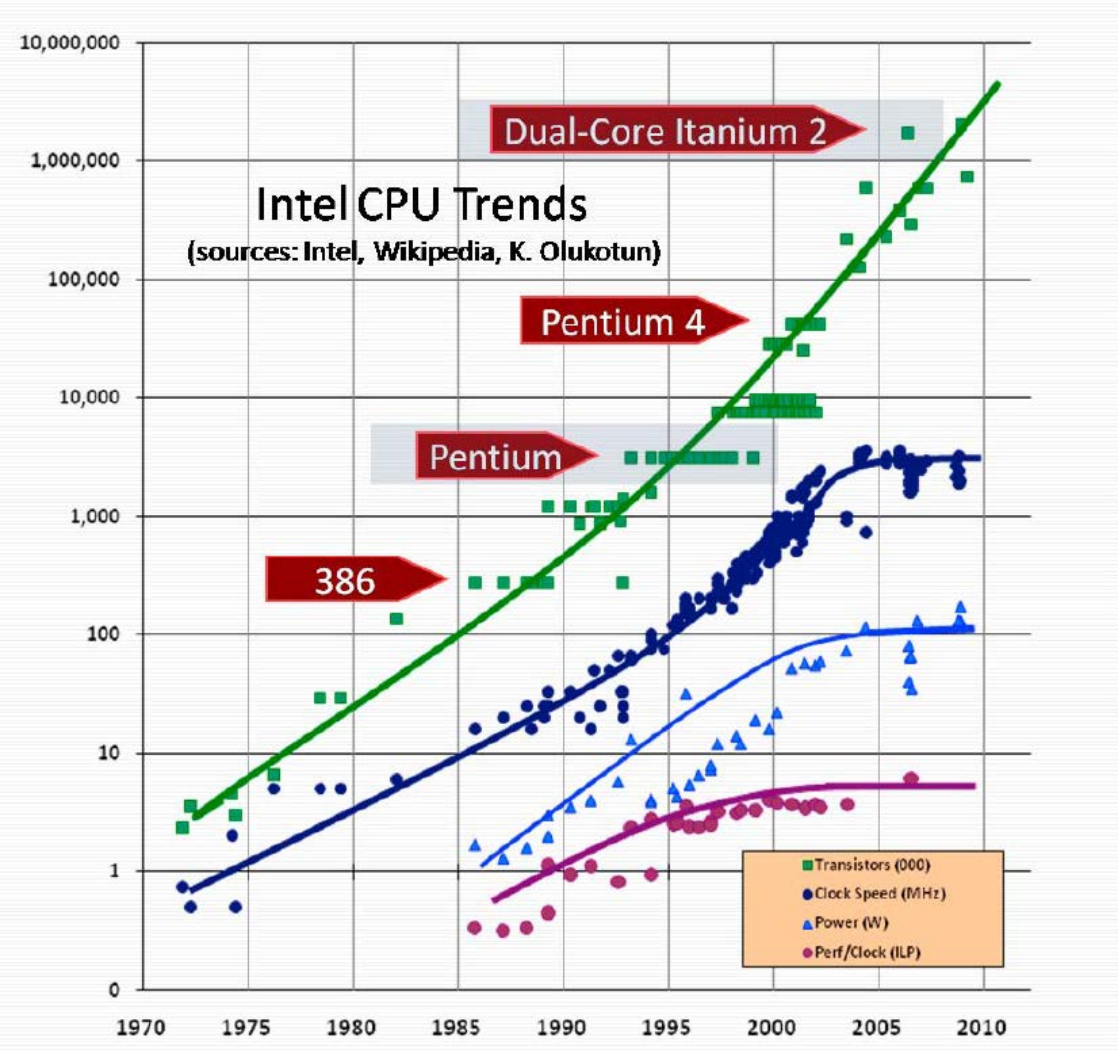

Figure 1.1 Scaling trends of number of transistors, clock speed, power, and performance [2].

Of these beyond CMOS computing schemes, molecular quantum dot cellular automata (QCA) is perhaps the most extreme case of scaling. This form of computing encodes 1's and 0's as the electron occupancy of quantum dots in specially designed molecules [3]. QCA consists of an arrangement of cells with each cell containing four quantum dots and two electrons. Due to the repulsive force between the electrons, for a symmetric arrangement of the quantum dots in a cell, there are two stable energy

states where the electrons are as far apart as possible. These states encode the binary data, and logic functions can be implemented by arranging cells appropriately [4].

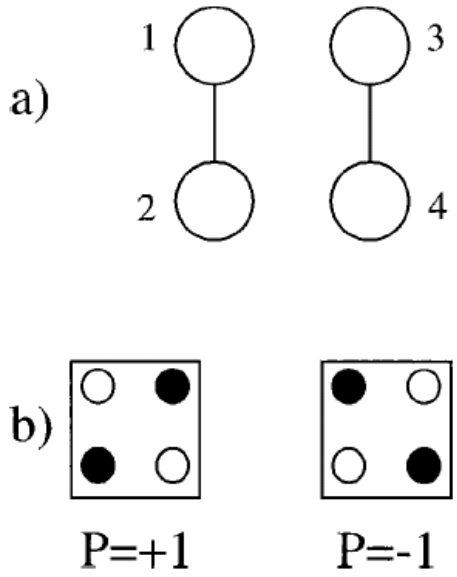

Figure 1.2 A QCA cell: a) Open circles represent quantum dots with lines representing coupling between dots, and b) shows the two polarization representing binary data where the filled circles are electron occupied quantum dots [5].

One obvious challenge to QCA is detecting the computed result because it is encoded in the positions of *single* electrons. This can be achieved by the use of single electron transistors (SETs), which are the most sensitive electrometers demonstrated to date [6]. Both QCA and SETs rely on electron-electron interactions which are typically negligible in bulk metals at room temperature but become more noticeable for nanoscale structures on the order of ~10 nm. Consequently, the performance of both devices improves as they are scaled down. Furthermore, in the remaining years of

CMOS scaling that will require very thin high-k dielectrics, SETs may be used to characterize the defects and interface states of these materials.

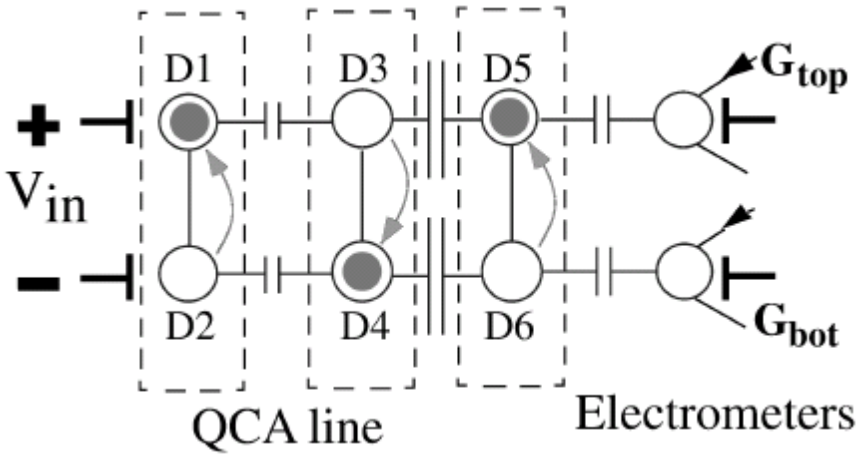

Figure 1.3 Illustration showing the input electrodes, QCA cells, and SET electrometers [4].

CHAPTER 2:

SET THEORY

Single electron transistors (SETs) are like other transistors in that they are three terminal devices with a gate used to modulate current between the source and drain. In an SET, separated from the source and drain by tunneling barriers is a conductive "island". The gate is capacitively coupled to the island and can modulate its potential. Due to the island's small size and hence small capacitance, individual electrons entering or leaving the island can result in a measureable change in the electrostatic energy of the island.

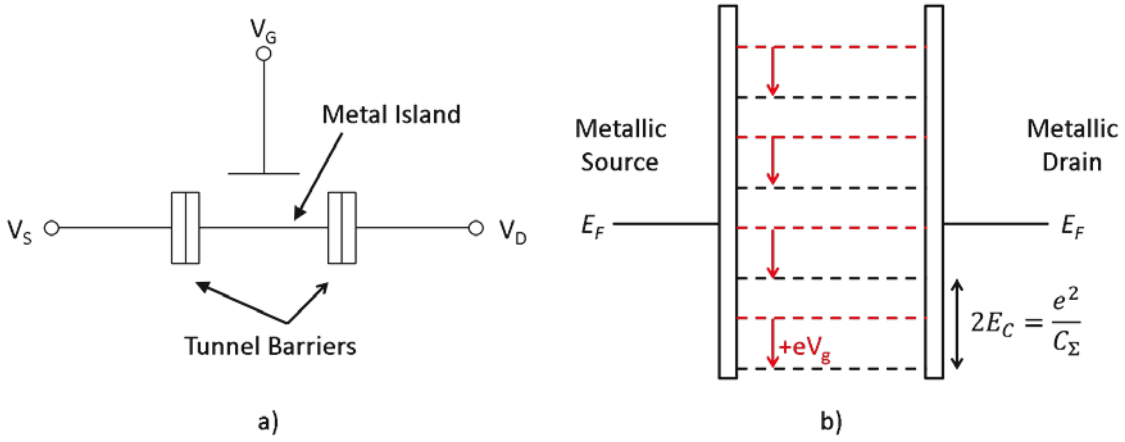

Figure 2.1 a) Schematic showing SET source, drain, gate, and island. b) Band diagram of an SET. The levels in the island are due to Coulomb interaction between electrons and these levels can be shifted by the gate voltage.

To describe the electrostatics of the SET, it is easiest to first consider the single electron box, which is an SET with the source and drain both tied to ground (see Figure 2.2). In this configuration, electrons can tunnel from the source/drain to the island when it is energetically favorable. Using Kirchhoff's Voltage Law and the definition of capacitance $C = Q/V$, it can be shown that the island potential is

$$V_i = \frac{C_g V_g}{C_g + C_j + C_0} + \frac{Q}{C_g + C_j + C_0} \quad (2.1).$$

where

$$Q = q_j - q_g = -Ne \quad (2.2)$$

is the quantized charge on the island, q_g is the charge induced by the voltage from the gate to the island, q_j is the charge induced by the voltage from the island to the grounded source/drain, N is the number of electrons on the island, C_0 is the self-capacitance of the island, and e is the elementary charge.

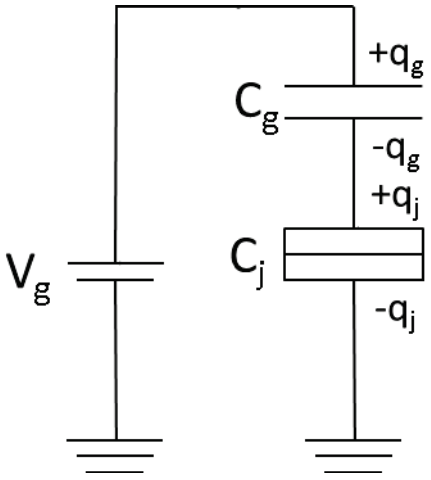

Figure 2.2 Single electron box.

Therefore, the electrostatic energy of the island is

$$E = \int_0^Q -V_i dQ' = \frac{Q^2}{2\left(C_g + C_j + C_0\right)} + \frac{C_g V_g Q}{C_g + C_j + C_0}$$

$$= E_C \left(N^2 - 2N \left(\frac{C_g V_g}{e} \right) \right) \tag{2.3}$$

$$E_c = \frac{e^2}{2\left(C_g + C_j + C_0\right)} \tag{2.4}$$

where E_c is called the charging energy of the island and is the energy that would be required to add the first excess electron to the island with V_g = 0 V. The self-capacitance is typically so small compared to the capacitance of the tunnel junction and the gate that it is negligible, and it will be dropped in the following analysis. It is worth noting, however, that for a given island size, the self-capacitance sets an upper limit on the charging energy.

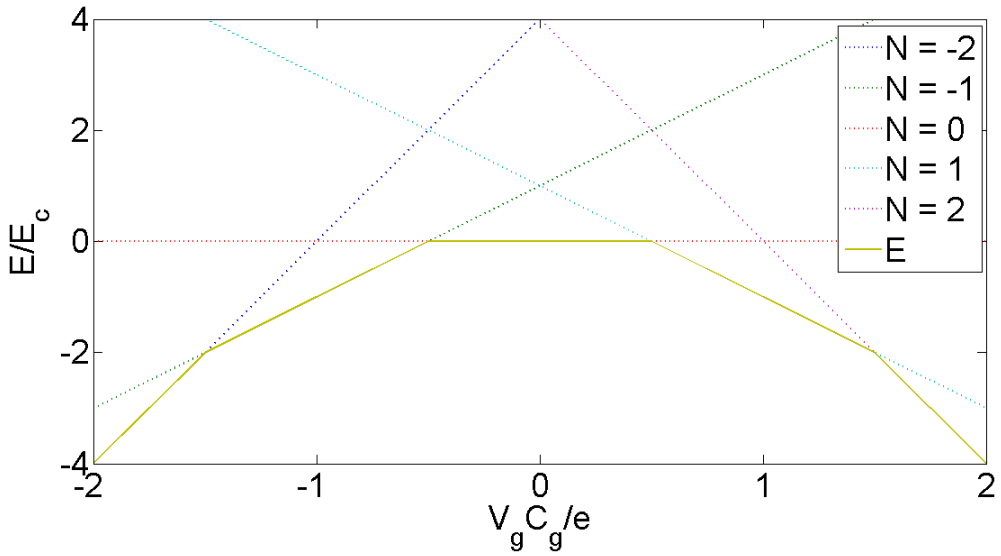

Figure 2.3 Electrostatic energy of the island in a single electron box for fixed N (dotted lines) as a function of gate voltage. When N is not fixed (i.e. electrons are allowed to tunnel), the system follows the solid curve of minimum energy.

For $kT << E_c$, the system seeks the lowest available energy state by populating or depopulating the island, depending on V_g. Figure 2.3 is a plot of (2.3) and shows dashed lines for various fixed N (i.e. fixed number of electrons on the island) while the system follows the solid curve of minimum energy when N is allowed to change (i.e. electrons are allowed to tunnel). More frequently, the free energy is plotted, which is the energy that is only dependent on the number of electrons. The free energy can be calculated from the electrostatic energy by completing the square in (2.3) and ignoring the term solely dependent on V_g:

$$E_f = E_c\left(N - C_g V_g/e\right)^2 \tag{2.5}$$

For the free energy, (2.5) describes a set of parabolas as shown in Figure 2.4.

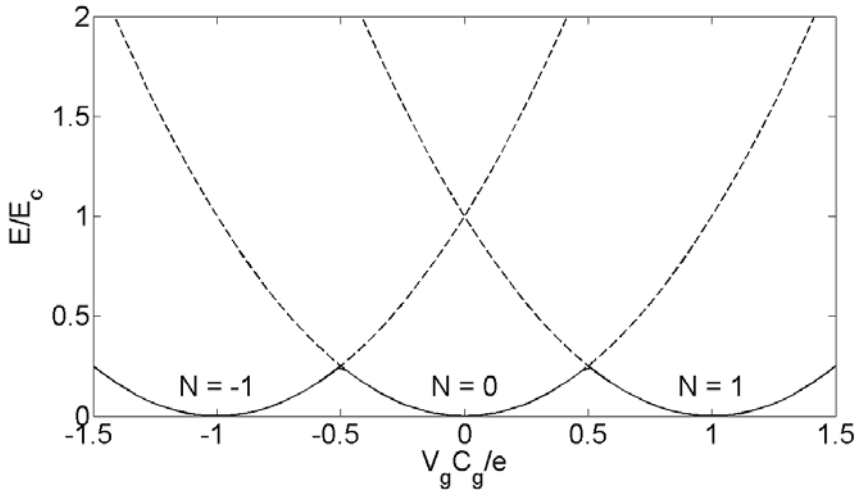

Figure 2.4 Free energy of a single electron box. Each dashed parabola is the free energy for a fixed number of electrons on the island while the solid line is the free energy of an actual single electron box since charge can tunnel to the island.

The most significant characteristic of the single electron box is the degenerate energy points at the kinks in the solid curve of Figure 2.3 and at the lowest intersections of the parabolas in Figure 2.4. At these points where $V_g C_g/e = (N + 1/2)$ the island can have either N or N+1 electrons, whereas at all other values of V_g it is only energetically favorable for the island to have some fixed, integer number of electrons.

Now consider an SET: the electrostatic energy for the SET is the work required to get the SET into that charge configuration N for a given V_g and V_{ds}. When the source and drain are biased, the amount of work needed depends on whether the electrons come from the source or from the drain electrode (since they are separated by an energy equal to eV_{ds}). Due to this, two electrostatic energies need to be considered for an SET (see Figure 2.5), and these energies have equations similar to (2.3), developed for the

single electron box [7]. If the source is grounded and the drain is biased, the island voltage is given by

$$V_i = \frac{1}{C_g+C_s+C_d}\left(C_g V_g + C_d V_{ds} - Q\right) \quad (2.6)$$

where C_g, C_s, C_d are the capacitances of the island to the gate, source and drain respectively, and V_{ds} is the voltage of the drain relative to the grounded source. For charge coming from the source, the electrostatic energy is given by

$$E_s = E_c\left(N^2 - \frac{2N}{e}\left(C_g V_g + C_d V_{ds}\right)\right) \quad (2.7)$$

$$E_c = \frac{e^2}{2\left(C_g+C_d+C_s\right)} \quad (2.8).$$

Electrons coming from the drain require the same amount of work as those coming from the source plus eV_{ds} per electron to compensate for the drain bias.

$$E_d = E_s + eV_{ds}N = E_c\left(N^2 - \frac{2N}{e}\left(C_g V_g + C_d V_{ds}\right)\right) + eV_{ds}N \quad (2.9)$$

Solving (2.7) and (2.9) for the degeneracy points (i.e. where E(N) = E(N+1)) gives two sets of lines, along which having N or N+1 electrons is equally favorable for the source or drain respectively. For electrons from the source:

$$V_{ds} = \frac{\left(N+\frac{1}{2}\right)e - C_g V_g}{C_d} \quad (2.10).$$

And for electrons from the drain:

$$V_{ds} = \frac{C_g V_g - \left(N+\frac{1}{2}\right)e}{C_g+C_s} \quad (2.11).$$

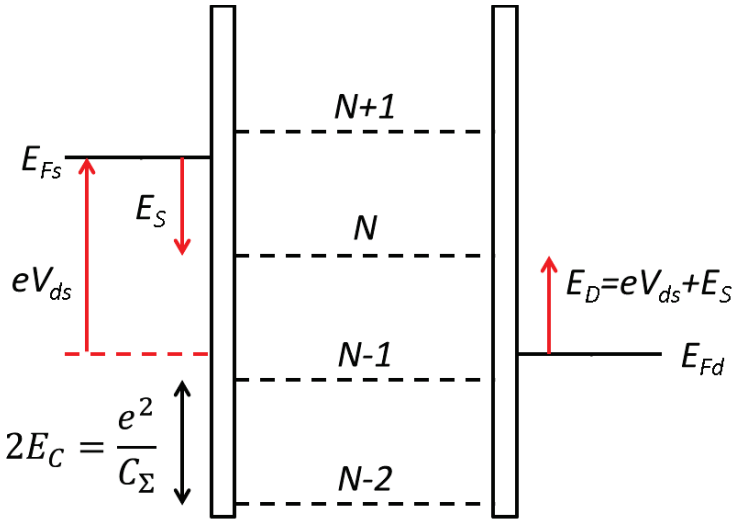

Figure 2.5 Energy level of an SET under bias. The black dashed lines show the Fermi level of the island for a given number of electrons on the island. E_{Fs} and E_{Fd} are the Fermi levels of the source and drain respectively. The dashed red line is the drain Fermi level for reference. E_S and E_D are the electrostatic energies for electrons coming from the source and drain respectively.

Adjacent parallel lines defined by (2.10) define regions of V_{ds} and V_g where the source favors N electrons. Equation (2.11) defines similar regions for the drain. The overlap of these regions forms diamonds (the current of which will be derived later) as can be seen in Figure 2.6, which is referred to as a “charge diagram”.

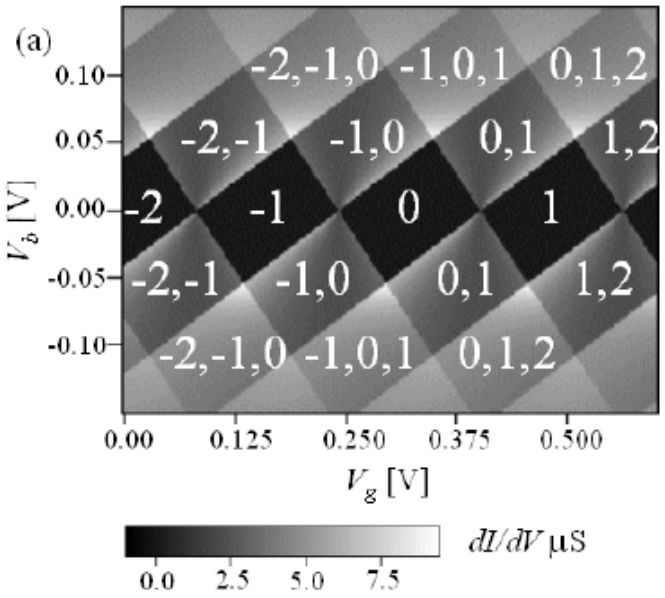

Figure 2.6 Coulomb blockade regions defined by (2.10) and (2.11). V_b in the figure equates to V_{ds} in the text. The numbers in each diamond designate the allowed number of electrons in that region [8]. The offset in V_g is due to background charge.

For example, inside the diamond marked "0" in Figure 2.6, both E_S and E_D are minimized for N=0, no excess electrons on the island. Since the island can have 0 excess electrons and only 0 excess electrons, no current can pass through the island and this region is known as Coulomb blockade because current flow is blocked. Diamonds notated with more than one number indicate regions where the blockade has been lifted and current flows because the source and drain "disagree" on the number of electrons that should be on the island. For example, the higher diamond marked "-1, 0, 1" in Figure 2.6 corresponds to a region where E_S is minimized when N=1 electron but E_D is minimized when N = -1 electron. In this case, the island can have anywhere from -1 to

1 excess electrons and current can be conducted by up to 2 electrons at a time from the source to the drain.

One important criterion for single electron transistors is that electrons are localized on the island so that charge is quantized. This can be satisfied as long as the uncertainty in energy from the Heisenberg uncertainty principle is smaller than the charging energy. Assuming the uncertainty in the time measurement is comparable to the RC-time constant of the SET gives the condition

$$2E_c\tau_{RC} = \frac{e^2}{C}\frac{C}{G} > \Delta E\Delta t > \frac{h}{2} \Rightarrow G < \frac{2e^2}{h} \approx 77\ \mu S \qquad (2.12)$$

where G=1/R is the conductance of the tunnel junction. This condition guarantees that the charge on the island is quantized.

To fully and quantitatively describe the SET, the current for each bias point must be described. At T=0 K, the tunnel rate for a simple tunnel barrier is simply related to the current by $\Gamma = I/e\ = V/Re = \Delta E/Re^2$ where ΔE is the change in energy from one side of the tunnel barrier to the other and R is the junction resistance [9]. At T>0 K, this is modified by the probability of an electron having energy E on one side of the barrier and there being a state $E + \Delta E$ available on the other side of the barrier. Therefore, the tunneling rate becomes

$$\Gamma = -\frac{\Delta E}{Re^2}\int_{-\infty}^{\infty} f(E)\big(1 - f(E + \Delta E)\big)dE = -\frac{\Delta E}{Re^2}\frac{1}{1-e^{\Delta E/kT}} \qquad (2.13)$$

where f(E) is the Fermi distribution.

For SETs, ΔE is the difference in electrostatic energy for different charge states, depending on whether the electron came from the source or drain.

$$\Delta E(N) = E_{s,d}(N \pm 1) - E_{s,d}(N) \tag{2.14}$$

This implies that the tunneling rate is a function of N, the number of electrons on the island before the tunneling event, and that for each state N there are four possible tunneling events that need to be considered in an SET: to the source ($\Gamma_{-s}(\Delta E_{-s})$), from the source ($\Gamma_{+s}(\Delta E_{+s})$), to the drain ($\Gamma_{-d}(\Delta E_{-d})$), and from the drain ($\Gamma_{+d}(\Delta E_{+d})$), where

$$\Delta E_{-s}(N) = E_s(N-1) - E_s(N) \tag{2.15}$$

$$\Delta E_{+s}(N) = E_s(N+1) - E_s(N) \tag{2.16}$$

$$\Delta E_{-d}(N) = E_d(N-1) - E_d(N) \tag{2.17}$$

$$\Delta E_{+d}(N) = E_d(N+1) - E_d(N) \tag{2.18}$$

Thus for each bias point, the four tunneling rates must be calculated.

Furthermore, for each bias point the current will be constant (i.e. a stationary state since current is the average flow of electrons) and there will be a stationary probability p_N of finding the SET in each charge state N. Since this probability p_N is stationary, the tunneling rates that result in the state N (i.e. tunnel events where the initial state is N±1 and the final state is N) are balanced out by tunneling rates that result in the states N±1 (i.e. where the initial state is N and the final state is N±1):

$$\frac{dp_N}{dt} = 0 = -\big(\Gamma_{-s}(N) + \Gamma_{+s}(N) + \Gamma_{-d}(N) + \Gamma_{+d}(N)\big)p_N + \big(\Gamma_{-s}(N+1) + \Gamma_{-d}(N+1)\big)p_{N+1} + \big(\Gamma_{+s}(N-1) + \Gamma_{+d}(N-1)\big)p_{N-1}. \quad (2.19)$$

Since all the tunneling rates are known, this reduces to a linear algebra problem that depends on the number of electrons involved. Once the stationary probabilities for each state have been found, the current through each tunnel junction is given by

$$I = e\sum_N\big(\Gamma_{+s}(N) - \Gamma_{-s}(N)\big)p_N = e\sum_N\big(\Gamma_{-d}(N) - \Gamma_{+d}(N)\big)p_N \quad (2.20)$$

To conclude this chapter, a few practical concerns are worth noting. Since the total island capacitance $C_d + C_s + C_g$ is inversely proportional to the size of the island, it follows that scaling down the SET increases the charging energy E_C. This is beneficial because one of the assumptions made in deriving the single electron behavior described by the equations above was that $kT \ll E_C$. Thus a larger charging energy allows the SET to operate at higher temperatures. However, due to fabrication limitations, most SETs are still tested at liquid Helium temperatures to observe single electron behavior. To make a room temperature SET requires an island on the scale of 5 nm, at which size energy quantization can become significant depending on the density of states at the Fermi level [9]. However, this work will only consider single electron behavior in the classical limit.

Since the conductance of an SET is due to tunneling, it is extremely sensitive to the thickness of the dielectric barrier. SETs are mesoscopic devices so one of the

greatest challenges in their fabrication is ensuring both that the conductance is not so small that it is immeasurable and that the electrons are localized (satisfying equation (2.12)). The most popular SET fabrication technique for metal-metal oxide based devices has been the Dolan bridge [10], which achieves a small capacitance by using two evaporations through a lithographic mask at different angles and *in situ* oxidation to create the dielectric barrier between the metal layers. In this work, atomic layer deposition is used to form the tunnel barriers due to it's ideally monolayer control of thickness.

CHAPTER 3:

OVERVIEW OF FABRICATION TECHNIQUES

The two principal techniques employed in fabrication in this work are atomic layer deposition (ALD) and electron beam lithography (EBL). Given that SETs can operate at higher temperatures when scaled down and that the tunnel barriers must be very consistent in thickness but also very thin (~ 1nm thick), each of these techniques allows fine control of the most critical dimensions of an SET: EBL over the lateral dimensions of the SET and ALD over the barrier thickness. A brief overview of each technique will be given.

Atomic layer deposition is a self-limiting form of chemical vapor deposition (CVD). CVD uses gaseous precursors which react with each other on or near the heated substrate to form a continuous film, and numerous varieties of CVD have been developed (e.g. plasma assisted, low pressure, hot wire, metal organic, etc.) [11]. However, CVD is ill-suited to the production of extremely thin layers because the deposition rate is typically on the scale of 1 nm/sec, which makes deposition of nanoscale films difficult. ALD addresses this limitation by separating the precursors so that the only available reactions sites are on the substrate. Most commonly the precursors have been separated in time by pulsing one precursor and purging the

reaction chamber before introducing the next precursor, but spatially separated precursors have also been investigated to achieve faster deposition while retaining ALD's advantage of monolayer thickness control [12].

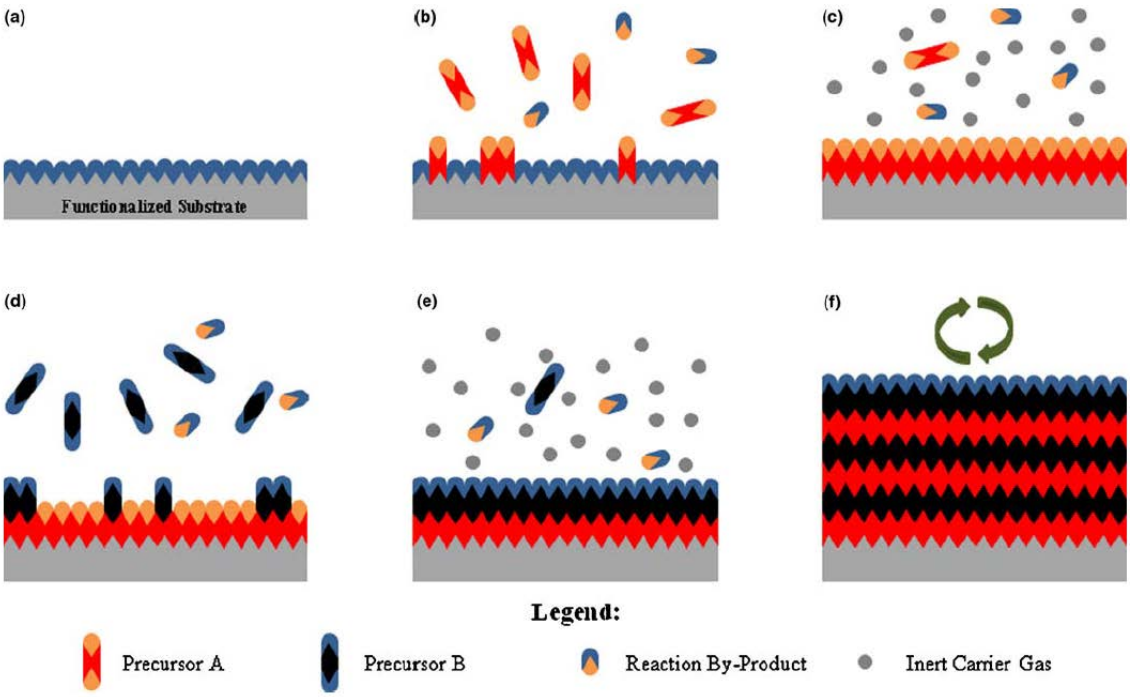

Figure 3.1 ALD process. (a) The prepared substrate. (b) Precursor A is pulsed into reaction chamber and reacts with the sample surface. (c) Further reactions of Precursor A with the surface are self-limited because Precursor A cannot react with itself. Reaction products are purged from the chamber by the carrier gas. (d) Precursor B reacting with surface. (e) Self-limiting and purging of Precursor B reactants. (f) Repeating the cycle provides monolayer control of thickness ideally [13].

Figure 3.1 shows the ideal ALD process. The first precursor is pulsed into the chamber and reacts with the surface. This reaction is self-limited because the first precursor cannot react with itself or any surface site with which it has already reacted. Next the unreacted first precursor and reaction products are purged out of the reaction

chamber using a carrier gas. After the first purge, the second precursor is pulsed into the chamber and reacts with the new surface sites created by the first precursor. Like the first precursor, it is self-limited and after the surface reaction is completed, any remaining precursor is purged out with the reaction products. This process is repeated leading to cyclic growth that ideally results in one monolayer per cycle.

In reality, however, ALD usually achieves less than one monolayer per cycle, especially during the initial cycles if the substrate is relatively inert. Moreover, the film is usually not uniform during the first few cycles but rather forms expanding islands around nucleation sites that eventually join to form a continuous film as more layers are added. Nucleation and uniform deposition have proven particularly problematic for 2D materials that have no dangling bonds or surface hydroxyl groups where nucleation can start [14]. But even aluminum oxide on silicon, which is an almost ideal ALD process that has been extensively studied, has been shown to form islands during the first 5 cycles which merge into a continuous layer after 10 total cycles [15].

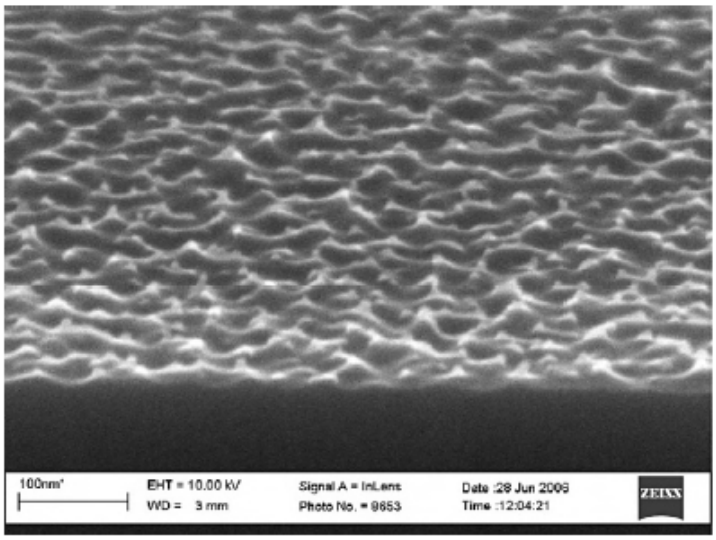

Figure 3.2 SEM image showing the island formation of Al_2O_3 on hydrogen-passivated silicon after 2 cycles of ALD, as revealed by plasma defect etching [15].

It should also be mentioned that ALD films are frequently annealed after deposition using rapid thermal annealing, but for different reasons depending on the application. One of ALD's first applications was replacing SiO_2 CMOS gate dielectrics with high-k dielectrics such as HfO_2 and Al_2O_3 so that gate leakage could be reduced by increasing the gate oxide thickness. For this purpose, it is important that interface defects and fixed charges be minimized to provide a consistent threshold voltage, and it has been found that rapid thermal annealing helps achieve this end [16]. It is believed that this is due to dangling bonds being eliminated at higher temperatures. Annealing can also change the microstructure and band structure [17]. For thin film transistors with ALD ZnO channels, it has also been found that annealing stabilizes the threshold voltage and reduces the hydrogen content of the film [18].

The second fabrication technique used was electron beam lithography (EBL). Much like ultraviolet lithography, EBL is used to form nanoscale patters and structures by selectively depositing energy in a spun-cast resist layer, changing the solubility of the resist in a developer. EBL deposits the energy using a finely focused beam of high-energy electrons whereas ultraviolet lithography uses photons. Figure 3.3 shows a number of typical EBL processes. In this work, only positive resist and lift-off were used.

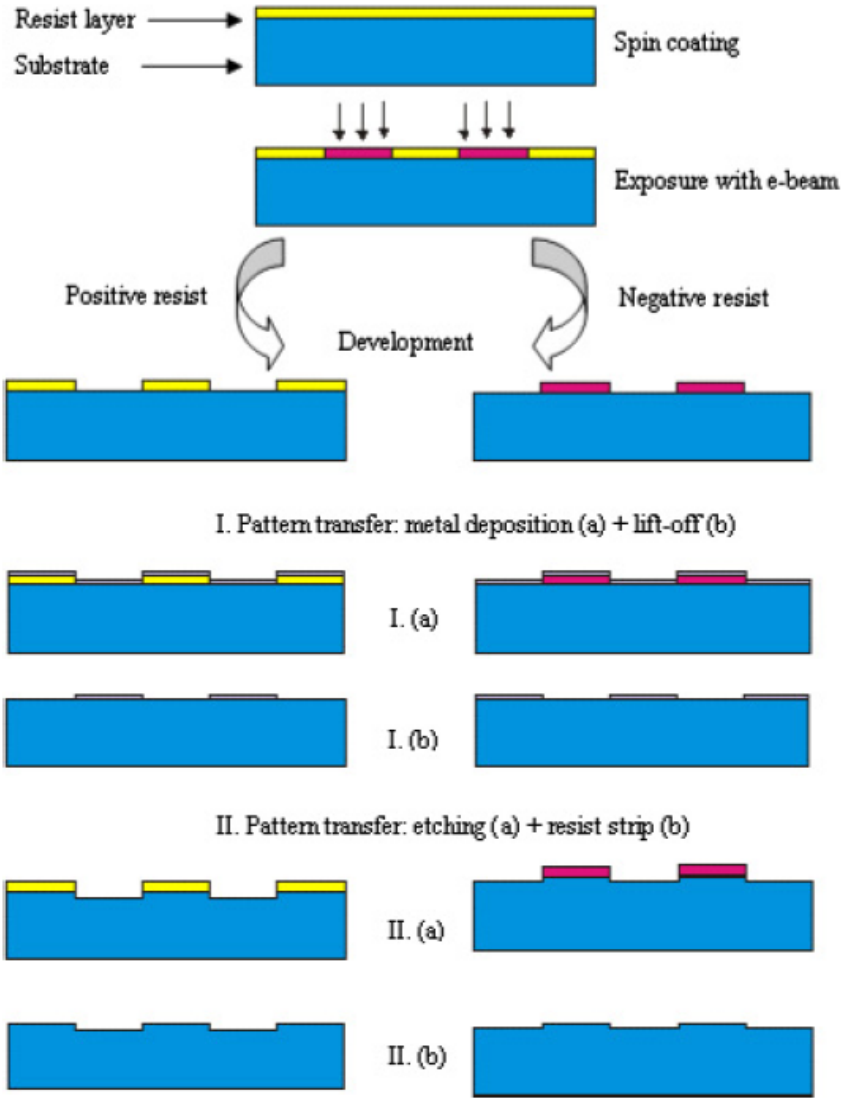

Figure 3.3 Typical EBL processes [19].

A number of factors affect the minimum feature size achievable by EBL: accelerating voltage, aperture, dose, the resist stack, development, the beam focus, and, to a limited extent, the substrate. A higher accelerating voltage leads to less forward scattering in the resist, resulting in steeper sidewalls, less undercut in the resist, and less backscattering from the substrate, which can improve resolution. Less undercut also decreases the chances of the resist collapsing (see Figure 3.4). Less backscattering has the advantage of decreasing the proximity effect, which is the enlargement of densely spaced features due to overexposure by backscattered or secondary electrons. Thus a higher accelerating voltage is generally preferred.

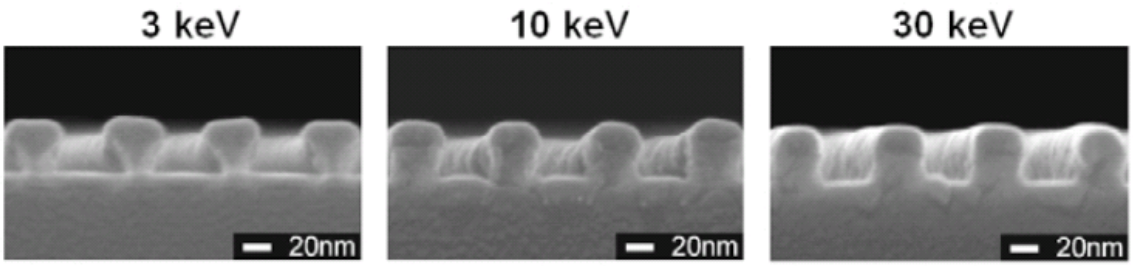

Figure 3.4 Grating of lines in PMMA showing the effect of different accelerating voltages [20]

The relationship between dose (usually measured in $\mu C/cm^2$ since the energy of the electrons is fixed), development time, and resist is usually optimized experimentally by a dose test, which finds a combination of dose and development that yields acceptable features. Lowering the dose can result in smaller features due to fewer scattered electrons but risks incomplete development. Longer development times can ensure that the resist is completely developed, but risks enlarged features.

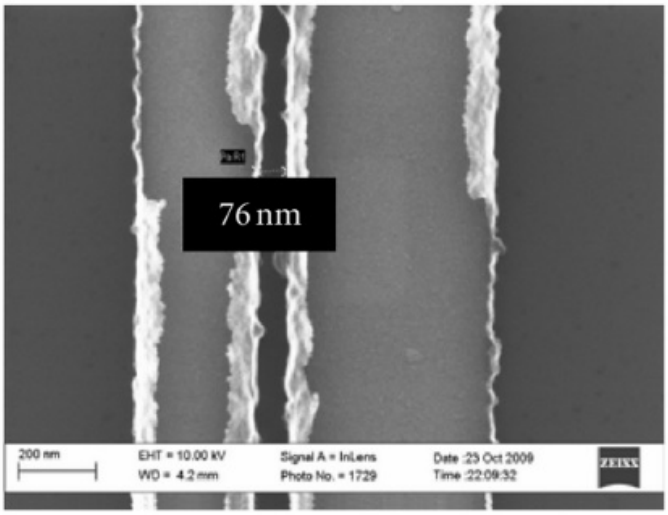

Figure 3.5 Scanning electron micrograph of “rabbit ears”. The long, vertical pieces of metal on the edge of the lines are formed when a continuous layer of metal is formed over the resist in contrast to what is shown in Figure 3.3 [21].

In this work, pattern transfer was accomplished by using liftoff with positive resist. After the resist is developed, metal is deposited uniformly on the sample by electron beam evaporation. This is followed by resist removal using a solvent. As the resist is removed, metal on top of the resist is likewise removed leaving only the metal that was formerly in the resist trenches (see Figure 3.3 for liftoff with positive resist). Liftoff is a simple and inexpensive technique (as compared to dry etching for example), but does suffer from a number of problems that can include adhesion problems, redepositing of metal particles during the liftoff process, and “rabbit ears” (Figure 3.5) which are tall, vertical pieces of metal at the edges of features caused by vertical or tapered resist sidewalls. Either poly(methyl methacrylate) or poly(methyl glutarimide)

was used as the positive resist in this work as these resists are both able to achieve a reentrant profile which mitigates the “rabbit ears” problem.

CHAPTER 4:

FABRICATION OF SINGLE ELECTRON TRANSISTORS

All devices were fabricated on silicon wafers having a surface of 500 nm of thermally grown SiO_2. Optical lithography with liftoff was used to define a layer of Ti/Pt (5/20 nm respectively). Another optical lithography step defined sixteen 20-pin Ti/Au (5/200 nm respectively) pad frames on each of the samples, which were approximately 1 cm^2. These pad frames were used to probe the SETs and bond the sample to a chip carrier for low temperature testing.

Before the EBL process, each sample was cleaned with acetone, isopropyl alcohol (IPA), and 5 minutes of direct oxygen plasma. EBL was used with liftoff to pattern the source, drain, and gate of the SETs using evaporated Pt (25 nm thick). Either poly(methyl methacrylate) (PMMA) or poly(methyl glutarimide) (PMGI) was used as the resist. For the PMMA process, a double stack of PMMA and methyl methacrylate (MMA, the monomer/copolymer of PMMA) was used (roughly 120 nm and 300 nm thick respectively). The MMA was exposed to 1.5 J/cm^2 of ultraviolet radiation (220 nm) before spinning on the PMMA to ensure development and a reentrant profile to ease liftoff [22]. The MMA layer was baked for 3 minutes at 170°C, and then the PMMA layer was spun on and baked for 2 minutes at 170°C. The EBL was done using a Vistec EBPG

5200 set at 100 kV, and the dose was set at 1000 μC/cm^2. The PMMA/MMA stack was then developed in an IPA, methyl isobutyl ketone (MIBK), methyl ethyl ketone (MEK) mixture (3:1:1.5% IPA:MIBK:MEK) for 30 seconds [23].

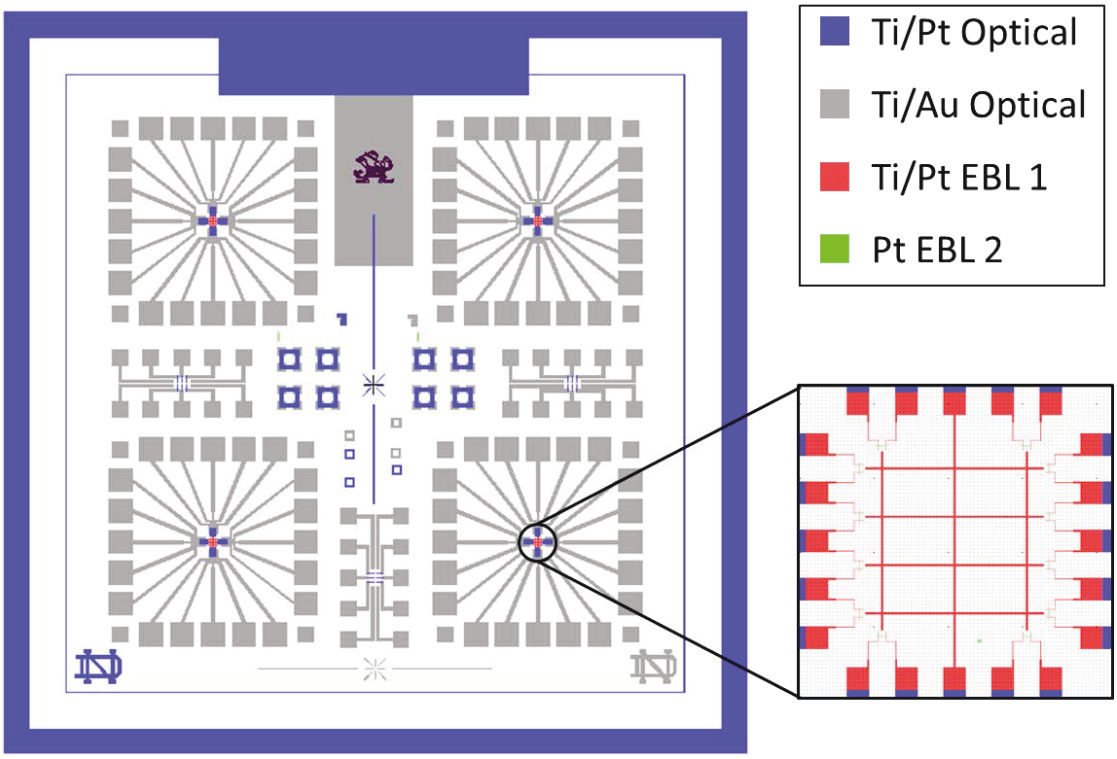

Figure 4.1 Four 20-pin pad frames from the optical lithography mask data. This pattern was repeated four times for each sample for a total of 16 pad frames per sample. The zoomed in portion shows the EBL layers.

PMGI was used as a single layer (roughly 125 nm thick) because it has been found to have excellent contrast, which enables it to have higher resolution than PMMA when developed at room temperature [24]. PMGI required a higher dose than PMMA (approximately 13 mC/cm^2) and was developed in Xylenes for 5 minutes with ultrasonic agitation at 100 Hz. After development, both the PMMA and PMGI processes proceeded

to a direct oxygen plasma descum step (10 sec) to clear the resist trenches of any residue.

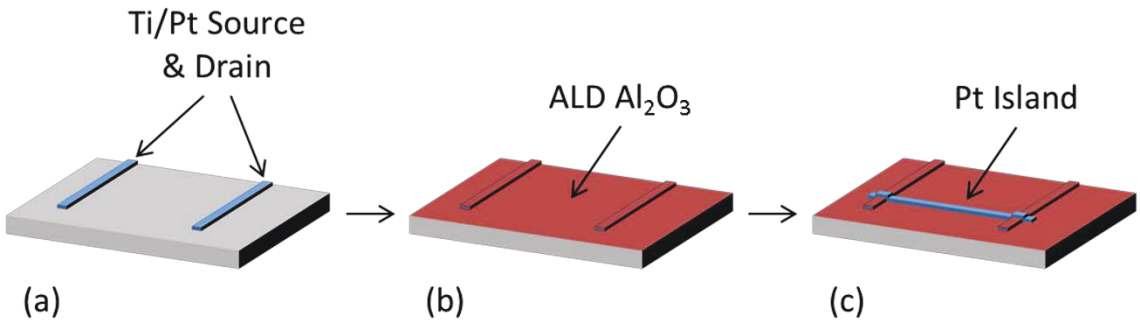

Figure 4.2 Fabrication process: (a) the Ti/Pt source and drain are deposited using EBL and liftoff, (b) the sample is coated with 9 cycles of Al_2O_3 using ALD, and (c) the Pt island is formed by EBL and liftoff (gate not shown).

The first metal layer deposited was the 25-nm thick Pt source, drain, and gate on a 5-nmTi adhesion layer. Deposition was carried out in an Oerlikon evaporator with a base pressure $<1\times10^{-6}$ Torr. The metal film was lifted off in mr-REM 400 resist remover (Micro Resist Technology) heated on a hotplate set at 90°C. After liftoff initiated, the sample was subjected to 2 seconds of ultrasonic agitation to aid liftoff; the ultrasonic time was kept short due to observed adhesions problems. An oxygen plasma clean was used to remove any resist left after liftoff.

Next, 9 cycles of Al_2O_3 (1 nm) were deposited at 200°C in a Cambridge Nanotech Savannah ALD system using either H_2O or O_3 (45 msec pulse), and trimethyl aluminum (TMA, 45 msec pulse) with a 5 sec purge time between each step. The ozone was generated by a LG-7 CD laboratory ozone generator and the concentration was

approximately 5% by weight. The growth rate, as observed in transmission electron microscopy images, is approximately 1.1 nm/cycle which agrees well with the growth rates recorded in literature for Al_2O_3 grown on Pt [25], but is generally higher than that reported for deposition on hydrogen-passivated silicon [26]. Nine cycles were selected as that number consistently provided a measurable conductance that also satisfied equation (2.12), the requirement on conductance to localize electrons to the island. The carrier/purge gas was nitrogen and the pressure was held at 200 mTorr.

Another oxygen plasma clean was applied after ALD as this was found to assist adhesion of the second layer. The second metal layer formed the SET island and followed the same procedure of EBL, metal evaporation, and liftoff as the first layer except that the Ti adhesion layer was omitted to form a symmetric metal-insulator-metal (MIM) tunnel barrier of Pt-Al_2O_3-Pt. The island layer was 30-nm thick Pt. After fabrication, various annealing and forming treatments were explored, which will be described in the next chapter.

CHAPTER 5:

RESULTS AND DISCUSSION

The conductance of the devices was initially measured using a lock-in amplifier and a current preamp at room temperature. Analyzing data from devices previously fabricated by graduate student Louisa Schneider [27], it was found that devices fabricated with water as the oxidative species in the ALD process showed a strikingly different conductance than devices fabricated with ozone for the same number of cycles. In general, as prepared water-based devices were approximately three orders of magnitude more conductive than ozone-based devices, with water-based devices typically having a conductance of ~9 μS while ozone-based devices had a conductance of ~2 nS. Furthermore, across multiple devices fabricated on the same chip, water-based devices showed a much larger spread in conductance than ozone-based devices as can be seen in Figure 5.1.

Both types of devices showed a large increase of more than two orders of magnitude in conductance when they were annealed in Ar at 375°C for three minutes in a Rapid Thermal Anneal (RTP) system. This was a desirable result for ozone-based devices, resulting in conductance of about 5 μS, but resulted in short-circuited tunnel junctions for water-based devices (~ 1 mS, which is approximately the conductance of

the metal nanowires without a tunnel barrier present). Looking at the standard deviation in conductance for each type of device also illustrates how annealing changes them. The spread in conductance for ozone-based devices is almost unchanged by annealing while the spread decreases noticeably for the water-based devices since the conductance is now limited by the resistance of the source and drain wires instead of the tunnel barriers.

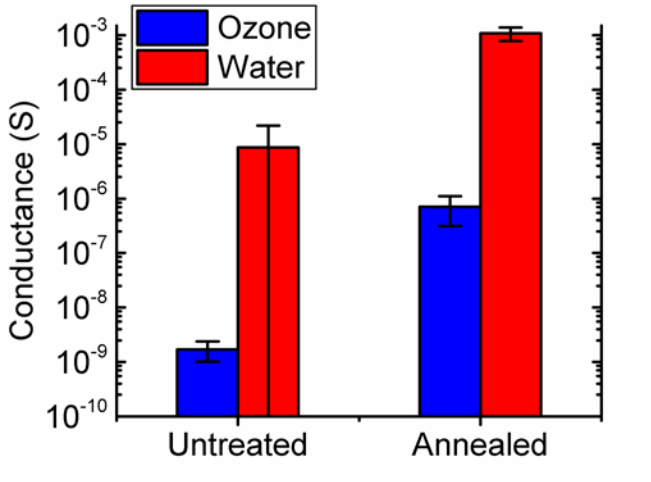

Figure 5.1 Average conductance and standard deviation at room temperature over at least 20 devices before and after annealing at 375°C in Ar for 3 minutes.

At $kT<<E_C$, an ideal MIM SET would show constant differential conductance $G_{ds} = dI_{ds}/dV_{ds}$ as a function of source-drain bias V_{ds} outside the region of Coulomb blockade (i.e. where $V_{ds}>>E_C/e$). But testing of untreated devices at approximately 5 K in a cryocooler, using a lock-in amplifier and current preamp, showed nonlinear I-V behavior outside of the Coulomb blockade region as can be seen by G_{ds} increasing as a function of V_{ds} in Figure 5.2. However, this nonlinear behavior was significantly less noticeable in

annealed devices as can be seen in comparisons to simulations (Figure 5.2-Figure 5.3). Also of interest, the width of the Coulomb blockade region in V_{ds}, which is proportional to the charging energy, did not change noticeably with annealing. A near constant charging energy means that the capacitances of the junctions were not noticeably changed by the anneal.

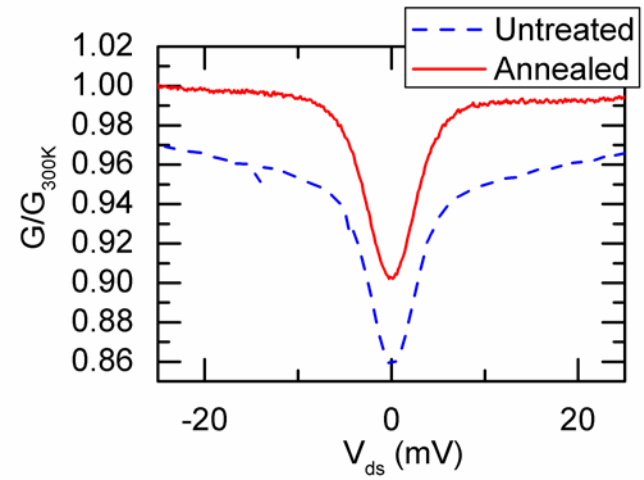

Figure 5.2 Differential conductance at T = 5 K of an ozone-based device as a function of source-drain voltage before and after anneal, normalized by room temperature conductance (G_{300K} = 5 nS for the untreated device, G_{300K} = 733 nS for the annealed device). The dip at V_{ds} = 0 mV is the Coulomb blockade, which is not fully formed at this temperature, and the width of this dip is proportional to the charging energy. Outside of the blockaded region, the untreated device shows more nonlinear behavior than the annealed device, which shows nearly constant differential conductance.

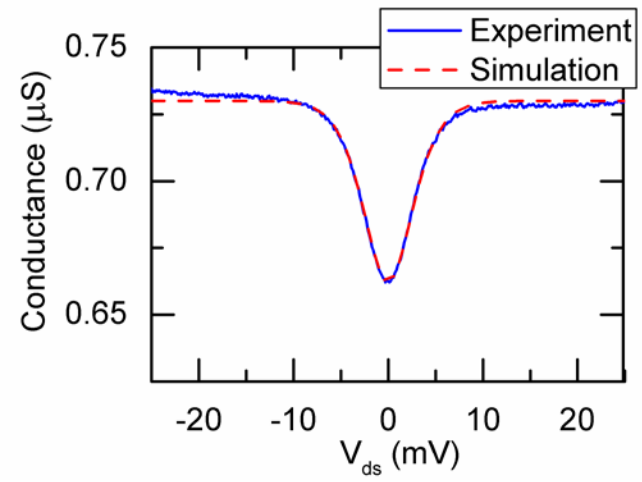

Figure 5.3 Differential conductance of an annealed, ozone-based device compared to a simulation using the master equation for SETs [28].

In order to determine the cause of these observations, transmission electron microscope (TEM) cross-sectional images were taken of the H_2O-grown ALD tunnel junctions before and after annealing in a FEI Titan TEM system (Figure 5.4). Structurally, both untreated and annealed junctions appeared very similar. However, EDX revealed that the bottom platinum layer near the Pt/Al_2O_3 interface had a higher oxygen content than the platinum of the top interface, as can be seen in Table 5.1 and, more significantly, that the oxygen content in the same position was much lower in an annealed sample (Table 2). This suggests that during the ALD process, a thin platinum surface oxide is formed on the bottom platinum layer.

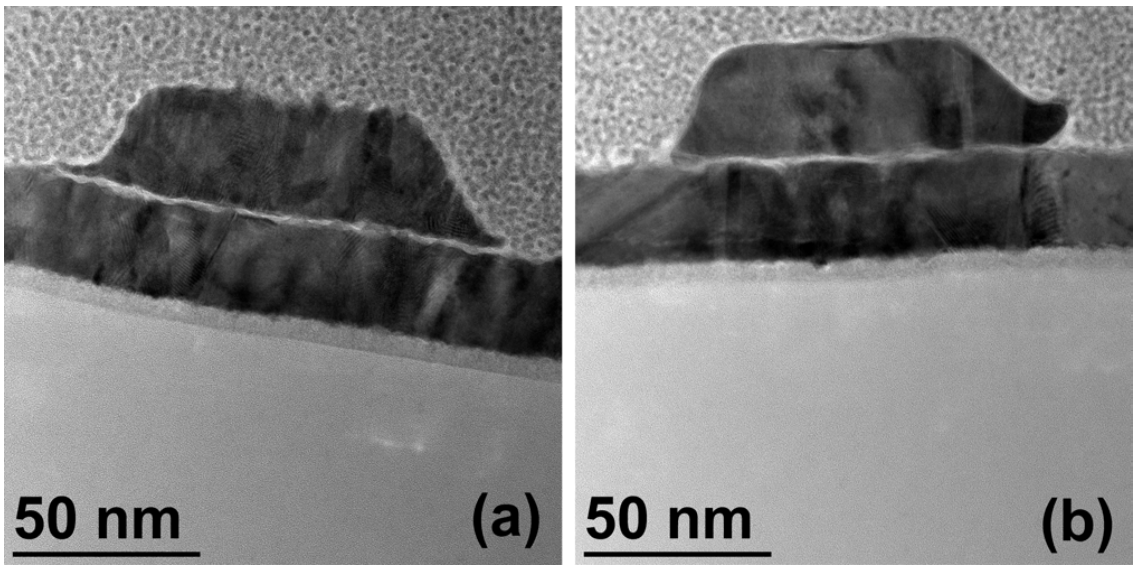

Figure 5.4 TEM image of water-based Al_2O_3 tunnel junctions (a) before and (b) after annealing.

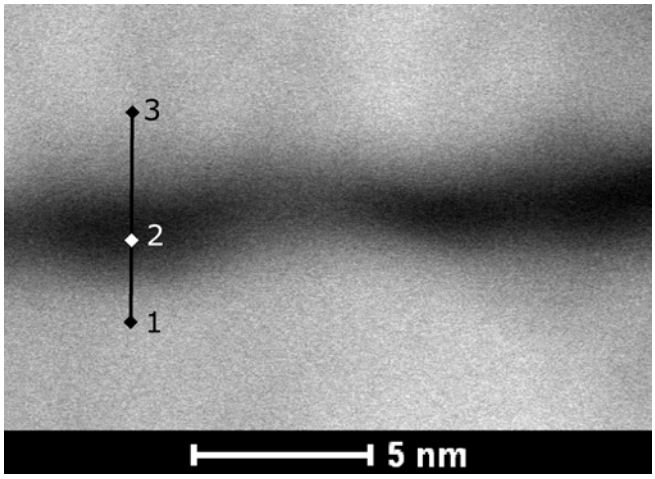

Figure 5.5 Scanning TEM image showing the positions of the EDX spectra used to generate the data in Table 1.

TABLE 5.1

ATOMIC PERCENTAGES BEFORE ANNEAL

Scan Position	1	2	3
Al	1.85	23.67	0
O	11.57	34.05	0
Pt	55.28	27.4	59.78
Cu	31.27	14.86	30.31

Note: scan position refers to those shown in Figure 5.5. Notice that position 2 shows an almost ideal Al/O ratio and also that position 1 in the bottom Pt layer shows a larger amount of O than position 3 in the top layer. The presence of copper is due to the grid supporting the sample, and platinum in position 2 is due to the electron beam not being perfectly confined to the very thin Al_2O_3 region.

TABLE 5.2

ATOMIC PERCENTAGES AFTER ANNEAL

Scan Position	1	2	3
Al	1.14	11.26	0
O	1.72	18.83	1.39
Pt	44.85	30.51	48.04
Cu	52.25	39.37	50.55

Note: Positions are similar to those shown in Figure 5.5 but on a different sample. Notice the decrease in oxygen content at position 1 compared to position 1 in Table 5.1.

While Pt is considered a noble metal without a surface oxide under most conditions, it has been well established in the literature that Pt has at least three different stable phases of oxide [29] and that a surface oxide can form under the right conditions [30]. Given that O_3 is a highly reactive oxidizing agent, the higher resistance of ozone-based devices is likely caused by the oxidation of the platinum surface.

Moreover, the most common platinum oxide, PtO_2, is unstable compared to other metal oxides [29]. It dissociates around 500°C at 1 atm of oxygen partial pressure and lower oxygen partial pressures reduce the decomposition temperature further as can be seen in the Ellingham diagram of Figure 5.6 [31].

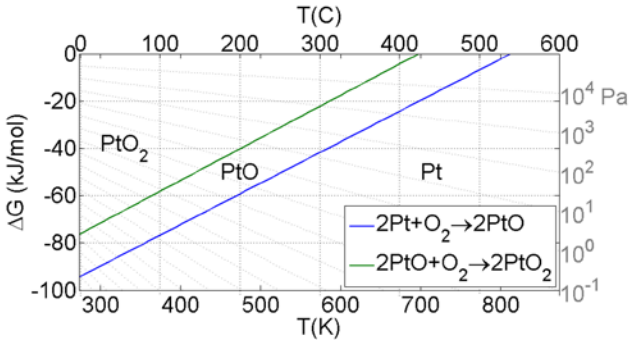

Figure 5.6 Ellingham diagram showing the change in Gibbs free energy per mole of oxygen as a function of temperature and pressure. These values were calculated using thermodynamic data from [32]. Lower oxygen partial pressures, shown in the nomographic scale on the right, reduce the decomposition temperature by changing the $\Delta G = 0$ kJ/mol line to the lines shown in grey with the pressures indicated.

These characteristics of PtO_2 suggest a theory as to why annealing greatly increased the conductance of ozone-based devices without changing the charging energy. PtO_2 was formed on the bottom Pt layer during the ALD process due to the O_3, but exposure to the high temperature and low oxygen partial pressure (since oxygen was displaced by argon) caused the PtO_2 to dissociate. This dissociation eliminated the resistive PtO_2 layer and increased the conductance. The insignificant change in charging energy can be explained by the fact that the capacitance due the PtO_2 is likely

significantly larger than that of the ALD layer since the parasitic layer is very thin and the dielectric constant of platinum oxide can be as high as 18 if it is nonstoichiometric [33].

The observed nonlinear behavior of differential conductance can therefore be explained by considering the contribution of the PtO_2 layer in the untreated devices. The sample, as prepared and before anneal, can be modeled by a series combination of the two Al_2O_3 tunnel barriers and two parasitic PtO_2 layers (Figure 5.7). The electrical conductivity of metal oxides typically exhibits thermally activated conductance [33] and nonlinear electric field dependence as was observed [34]. Once the PtO_2 decomposes, the parasitic oxide layer turns to metal, resulting in an approximately two orders of magnitude increase in conductance and the linear electric field response characteristic of MIM tunnel junctions. Such a large increase in conductance is due to the approximately exponential relationship between conductance and barrier thickness for tunnel barriers [35] (Figure 5.8).

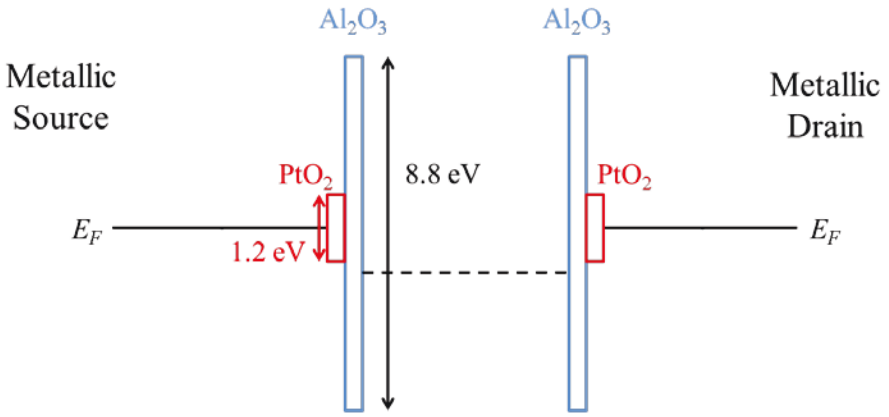

Figure 5.7 Band diagram of SET showing position of parasitic PtO_2 layers. PtO_2 barrier height estimate is from [33].

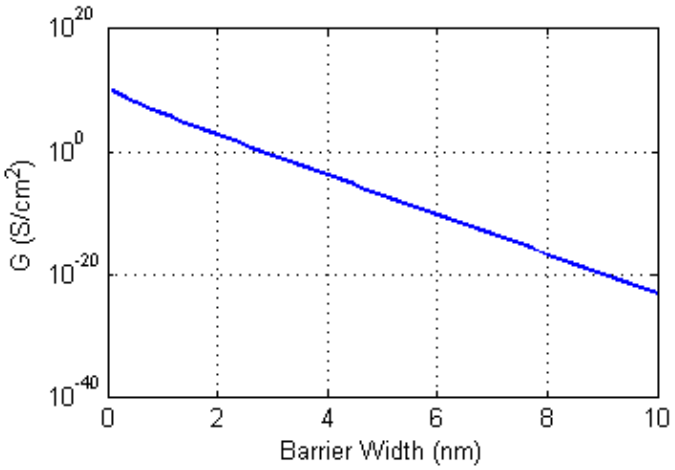

Figure 5.8 Conductance per unit area as a function of barrier width as given by the Simmons equation for zero bias across a uniform barrier [35]. The barrier height is 0.5 eV.

Likewise, the behavior of the water-based devices can be explained by native PtO_2 playing a major role in localizing the electrons to the island and by poor ALD nucleation when compared to ozone with the same number of deposition cycles. For the series combination suggested above, if conductance was limited by a layer of native PtO_2 in the as prepared water-based devices, then decomposition of the PtO_2 would result in a drastic increase in conductance, as is observed, and even the delocalization of electrons from the island. Furthermore, the smaller spread in conductance for ozone-based devices compared to water-based devices suggests that ozone-based devices have a more uniform ALD layer than water-based devices. This difference in conformity is attributed to the fact that H_2O is unable to oxidize the Pt surface as O_3 is able to [32] and that the ozone-induced formation of PtO_2 promotes ALD nucleation. This theory is supported by literature about nucleation on silicon [15] and ALD on similarly inert

substrates such as 2D transition metal dichalcogenides. McDonnell's study [14] of MoS_2 found that nucleation was either mediated by organic residue resulting in non-conformal ALD or depended on reactions between physisorbed precursors on the MoS_2 surface in a limited time window. Our results suggest a similar phenomenon for when H_2O is used on platinum, but that O_3 achieves more conformal ALD by oxidizing the platinum and providing a higher density of nucleation sites.

To test this theory about platinum oxide, another means of eliminating the parasitic oxide was investigated using devices I fabricated. Consider the reaction

$$PtO_2\ (s) + 2H_2\ (g) \rightarrow 2H_2O\ (l) + Pt\ (s)$$

where hydrogen is used to reduce platinum oxide. The change in Gibbs free energy for this reaction at room temperature is

$$\Delta G° = \Delta H° - T\Delta S° = -394\ kJ/mol \tag{5.1}$$

where ΔH° is the change in standard enthalpy, T is temperature, and ΔS° is the change in standard molar entropy using thermodynamic data from [32] and [36]. Since the change in Gibbs free energy is negative, this reaction is possible at room temperature but is not guaranteed to proceed at a measureable rate. Hydrogen is unable, however, to reduce the Al_2O_3 ALD barriers ($\Delta G° = +865\ kJ/mol$). To test this reaction, ozone-based devices were exposed to forming gas (5% H_2 in Ar) at low temperatures (~32°C) for 1 hour. The calculation above assumes a hydrogen partial pressure of 1 atm, but accounting for the lower hydrogen partial pressure in the forming gas only reduces the change in Gibbs free energy to -387 kJ/mol so the reaction is still possible.

After exposure to forming gas, the conductance increased by about a factor of 30 (0.5 nS to 15 nS), as would be expected if the theory about platinum oxide is correct. Furthermore, as a control experiment, a group of devices from the same wafer were exposed to Ar at the same temperature and for the same time, and no change in conductance was observed. Given the lower temperature, the smaller change in conductance for this process compared to the annealing process is likely due to a slower reaction rate and lower diffusion rate of the reaction by-products, but requires further investigation.

Other devices from the same sample were exposed to forming gas at higher temperatures and larger increases in conductance were observed, suggesting that forming gas at room temperature does not completely reduce the parasitic oxide (Figure 5.9). Even devices treated at 300°C may still have some parasitic oxide present because the conductance of the devices at the peak of Coulomb blockade oscillations was never observed to reach half of the conductance outside of Coulomb blockade, as would be expected for ideal devices. It was also observed that some devices ceased to show SET behavior upon annealing at higher temperatures. Device 13 showed Coulomb blockade after the second 20 minute treatment at 90°C as can be seen in Figure 5.10, but was an electrical short after the treatment at 300°C. The cause of this change may be that the conductance is approaching the quantum of conductance so that the electron is no longer localized to the island.

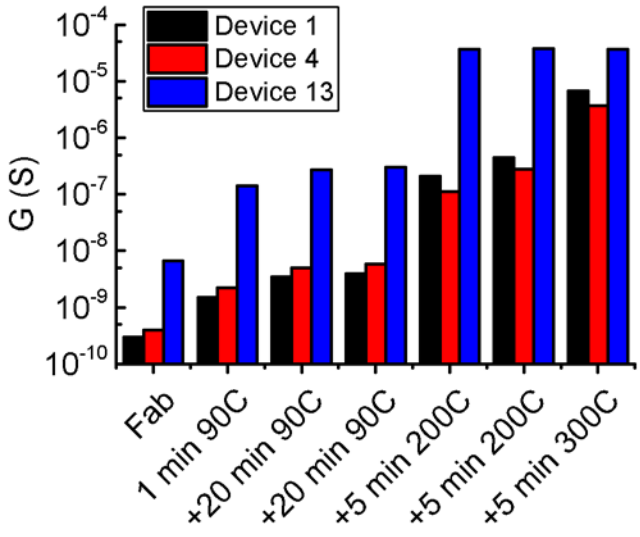

Figure 5.9 Increase in conductance with forming gas (5% H_2 in Ar). Each set of columns is for the same devices but measured after applying the treatment described.

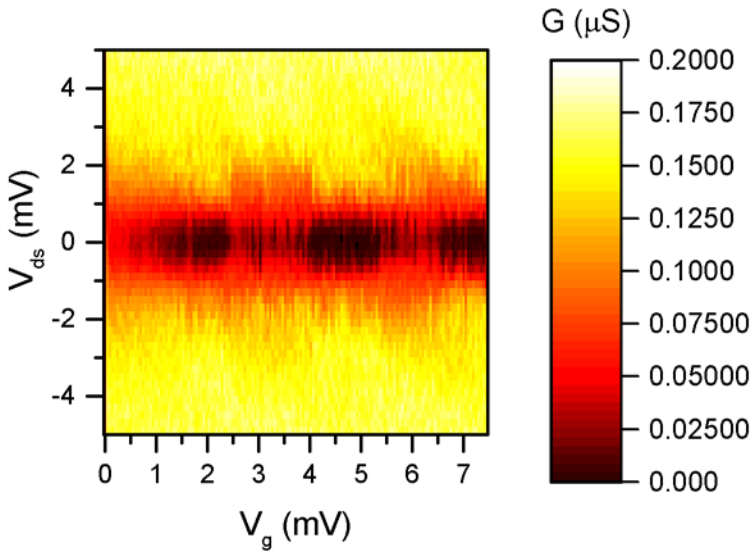

Figure 5.10 Device 13 tested at T = 0.5 K after the second 20-minute treatment at 90°C. The dark regions of low conductance are regions of Coulomb blockade. After this device was treated at 300°C, the Coulomb blockade disappeared possibly due to the barriers becoming shorts.

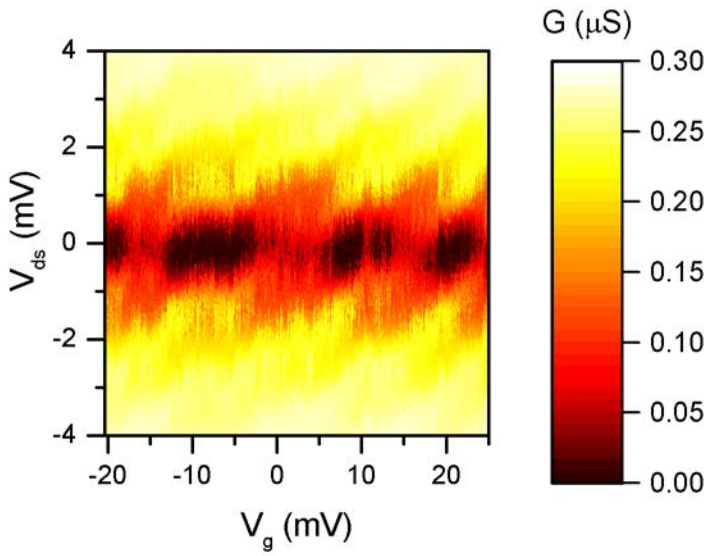

Figure 5.11 Charging diagram of device 1 after the 300°C 5 min treatment (T = 0.375 K).

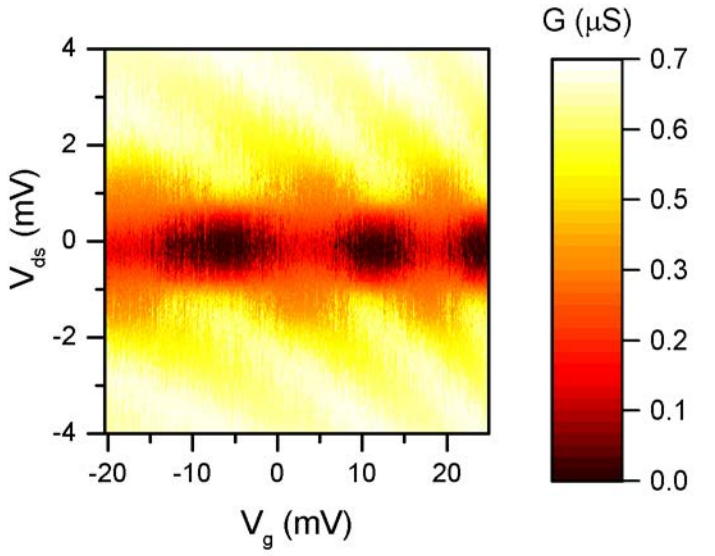

Figure 5.12 Charging diagram of device 4 after the 300°C 5 min treatment (T = 0.375 K).

Figure 5.11 and Figure 5.12 show the charging diagrams for devices 1 and 4 after the treatment at 300°C for 5 min. As can be seen in all the charging diagrams, the devices are noisy and the noise appears to be independent of V_g bias. This is most likely caused by traps within the tunnel barrier that are shielded from the gate by the metal of the source electrode and island. These traps are strongly coupled to the island due to their close proximity to the island, so that as the traps charge and discharge, the potential of the island is randomly shifted. These shifts in potential appear as noise in V_g in the charge diagrams. The periodicity of the Coulomb diamonds is also imperfect due to very slow movements of background charge in the Si substrate at low temperatures.

Another interesting observation was the time-dependent decrease in conductance after treatments in forming gas. Figure 5.13 shows the conductance at room temperature of a device over a 23-hour period after treatment in forming gas at 90°C for 20 minutes. As can be seen, the conductance drops by almost an order of magnitude. This can be explained by re-oxidation of the edge of the tunnel barrier. As mentioned earlier, treatment in forming gas at lower temperatures does not appear to completely reduce the parasitic oxide as further increases in conductance were observed when subsequently higher temperatures were used. The time-dependent drop in conductance suggests that when the devices are brought out of the RTP chamber into the oxygen-containing ambient, a thin ring of platinum around the edge of the tunnel barrier begins to re-oxidize and “pinch-off” the current tunneling through the barrier as shown in Figure 5.14. At higher temperatures, when most of the platinum oxide is

reduced, this effect is negligible because the majority of the tunnel barrier is free of the parasitic oxide.

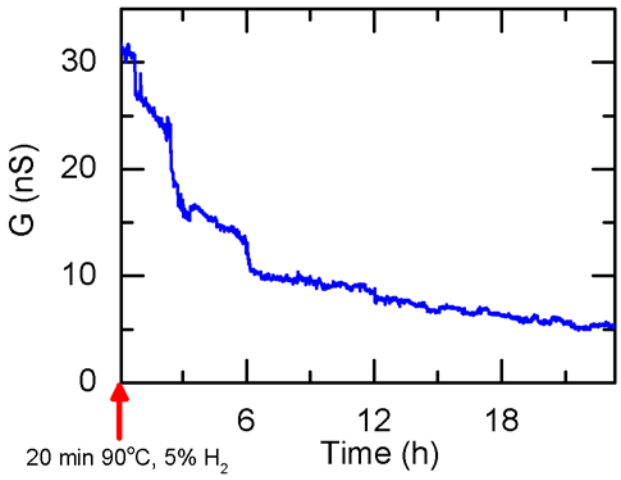

Figure 5.13 Conductance as a function of time after 20 minutes at 90°C in 5% H_2. This is believed to be caused by re-oxidation around the edge of the tunnel barrier.

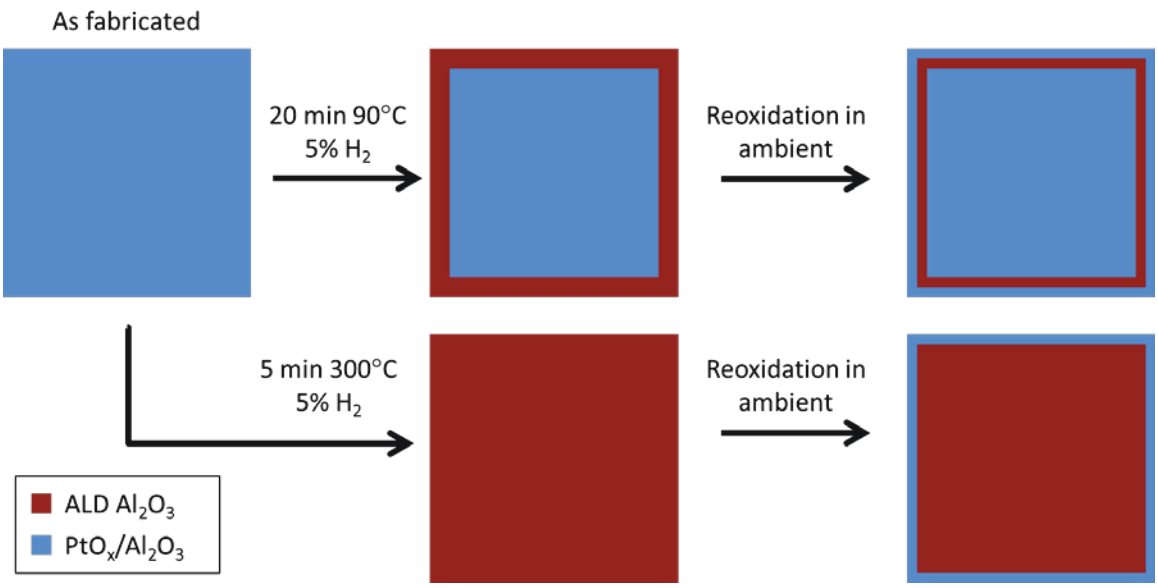

Figure 5.14 Top view of reduction and reoxidation of Pt-Al_2O_3-Pt tunnel barriers. In as fabricated devices, electrons must tunnel through both the Al_2O_3 and the PtO_x. This thicker tunnel barrier causes low conductance. Treatment with forming gas at 90°C only partially reduces the PtO_x but this provides a region where the electrons can tunnel through just the Al_2O_3 layer. When brought back out into the oxygen-containing ambient, this more conductive region shrinks as the edge of the tunneling region is re-oxidized. The same process happens when the devices are treated at 300°C but, since all the parasitic oxide is reduced in this case, the effect of re-oxidation is negligible.

CHAPTER 6:

FUTURE WORK AND CONCLUSIONS

Future work will concentrate on confirming the source of the noise and finding treatments to eliminate the traps within the barrier that are suspected to cause the noise. One possible weakness of the forming gas treatment used in this work is the low concentration of hydrogen. Higher concentrations may aid the reduction reaction so that more of the parasitic oxide can be reduced at lower temperatures. Another possible treatment is hydrogen plasma since the hydrogen radicals of the plasma make the reduction reaction more energetically favorable. A combination of annealing in forming gas and hydrogen plasma treatment has been found to yield the best noise performance for SETs fabricated using nickel and SiO_2, but it was also found that the plasma can damage the dielectric barrier [37].

Other tunnel dielectrics that may not oxidize the metal electrodes may also be investigated. SiO_2 deposited on Pt by ALD has been investigated but Pt-SiO_2-Pt capacitors with large areas were found to be electrically shorted until more than 100 cycles (about 10 nm) of SiO_2 was deposited. This suggests that SiO_2 growth is not completely uniform on Pt but it is unknown at this point what the density of pinhole defects is in the film. SiO_2 would have the added benefit of having a smaller dielectric

constant, which for equal dimensions would give a higher charging energy than Al_2O_3, but initial results and simulations suggest that for wires on the order of 20 nm wide, fringing fields may begin to dominate so that there is little advantage to using SiO_2 instead of Al_2O_3. Another dielectric that may be investigated is silicon nitride. Although its dielectric constant is similar to Al_2O_3, it can also be deposited by ALD and would not oxidize the metal electrodes since no oxygen is involved in the deposition process.

Other techniques are also being considered to characterize the tunnel barriers. All techniques employed so far have been unable to give an accurate picture of the uniformity of the tunnel barrier. TEM shows the cross section of the barrier but since there is some topography to the platinum surface and the image is viewed along this surface, it is difficult to determine if the barrier is uniform and how annealing and other treatments affect the barrier. One measurement that may be employed to measure the uniformity is scanning tunneling microscopy (STM). This technique employs tunneling from an atomically sharp tip to measure the local density of states and could be used to form an image of how conductive the barrier is on the nanometer scale. Tunneling spectroscopy may also be employed to determine the position and energy level of the traps that are believed to be causing noise in the SETs fabricated with ALD. Structures are currently being fabricated which would allow individual tunnel barriers to be tested. Tunneling spectroscopy uses the second derivative of current with respect to bias to determine the position and the energy level of the traps with respect to the Fermi level of the electrodes of individual tunnel barriers. This technique may aid in identifying the source of the noise-causing traps and in finding a way to eliminate them.

This work has demonstrated that MIM SETs can be fabricated by using ALD to form the tunnel barriers, but it has also shown that there are a number of challenges and disadvantages. Foremost among these is the oxidation of the metal electrodes. Compared to other metals, platinum is relatively inert, typically being included in the noble metals, yet it has been shown that the ALD process forms a parasitic surface oxide and that this lowers the tunneling current by more than two orders of magnitude from what it would be were the parasitic oxide not formed. A similar phenomenon has been observed for nickel using oxygen plasma as the oxidative species in the ALD process [38]. However, platinum does have the advantage of having an oxide that readily decomposes or reduces. Another challenge is that once the parasitic oxide has been eliminated, SETs fabricated with ALD have been found to be very noisy. As the principle interest in SETs is to sense small charge fluctuations, traps within the tunnel barriers that are strongly coupled to the island would obscure these measurements and must be eliminated.

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